SPICoder™ UR5HCSPI
Zero-Power™ Keyboard Encoder & Power Management IC for H/PCs

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HID & SYSTEM MANAGEMENT PRODUCTS, H/PC IC FAMILY

DESCRIPTION

The SPICoder™ UR5HCSPI keyboard encoder and power management IC is designed specifically for handheld PCs (H/PCs). The off-the-shelf UR5HCSPI will readily work with CPUs designed for Windows CE®, saving OEMs significant development time and money as well as minimizing time-to-market for the new generations of handheld products.

Three main design features of the UR5HCSPI make it the ideal companion for the new generation of Windows CE® -compatible, single-chip computers: low-power consumption; real estate-saving size; and special keyboard modes.

"Quasi" Zero-Power™ consumption (less than 2μA @ 3V), a must for H/PCs, provides the host system with both power management and I/O flexibility, with almost no battery drainage.

Finally, special keyboard modes and built-in power management features allow the SPICoder™ to operate in harmony with the power management modes of Windows CE®, resulting in more user flexibility and longer battery life.

The UR5HCSPI also offers programmable features for wake-up keys and general purpose I/O pins.

FEATURES

- SPI-compatible keyboard encoder and power management IC with other interfaces available
- Compatible with Windows CE® keyboard specification
- Zero-Power™ — typically consuming less than 2μA, between 3-5V
- Offers overall system power management capabilities
- Compatible with "system-on silicon" CPUs for H/PCs
- Special keyboard and power management modes for H/PCs, including programmable "wake-up" keys
- Scans, debounces, and encodes an 8 x 12 matrix and controls discrete switches and LED indicators
- Custom versions available

APPLICATIONS

- StrongARM™ Handheld PCs
- Windows CE® Platforms
- Web Phones
- Personal Digital Assistants (PDAs)
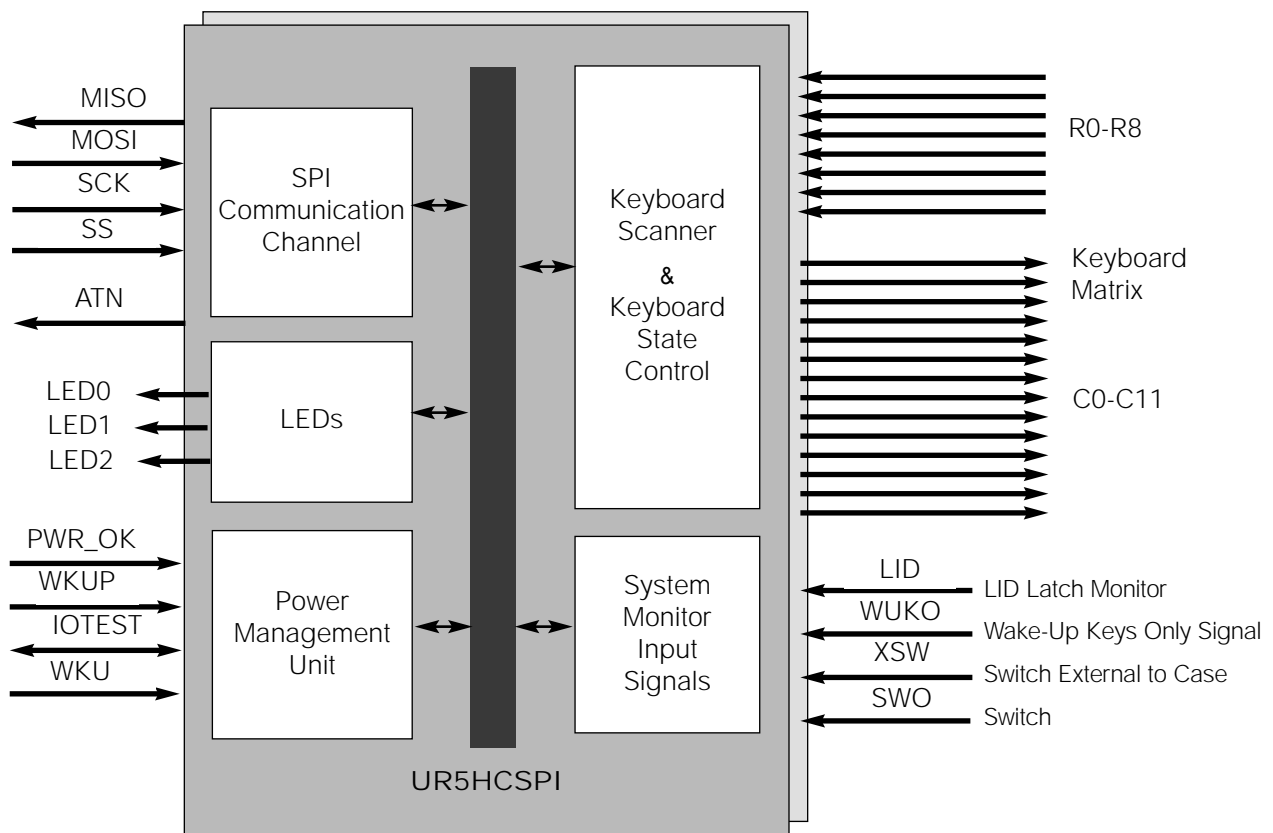- Wearable Computers
- Internet Appliance

PIN ASSIGNMENTS
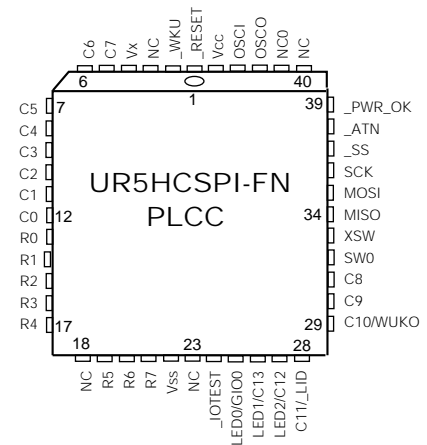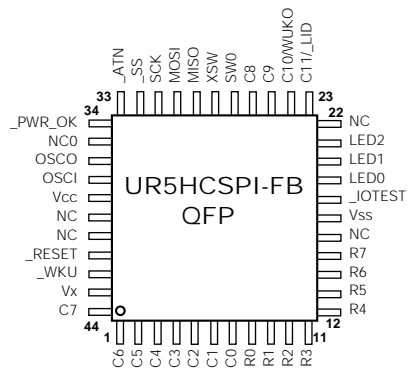
ORDERING CODE

Package Options	Pitch in mm's	TA=-20° C to +85° C
44-pin, Plastic PLCC	1.27 mm	UR5HCSPI-XX-FN
44-pin, Plastic QFP	0.8 mm	UR5HCSPI-XX-FB

Other Materials	Type	Order number
SPICoder™	Testing Board	ASY5-SPI-XXX

Note 1: XX=Optional Customization, XXX= Denotes Revision number

BLOCK DIAGRAM

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FUNCTIONAL DESCRIPTION

The UR5HCSPI consists functionally of five major sections (see the Functional Diagram on page 2). These are the Keyboard Scanner and State control, the Programmable I/O, the SPI Communication Channel, the System Monitor and the Power Management unit. All sections communicate with each other and operate concurrently.

PIN DEFINITIONS

Mnemonic	PLCC	QFP	Type	Name and Function
VCC	44	38		**Power Supply:** 3-5V
VSS	22	17	I	**Ground**
VX	4	43	I	Tie to VCC
OSCI	43	37	I	**Oscillator input**
OSCO	42	36	O	**Oscillator output**
_RESET	1	41	I	**Reset:** apply 0V to provide orderly start-up
MISO	34	29	O	**SPI Interface Signals**
MOSI	35	30	I	
SCK	36	31	I	
_SS	37	32	I	Slave Select: If not used tie to VSS
_IOTEST	24	18	O	**Wake-Up Control Signals**
_WKU	2	42	I	
R0-R4	13-17	8-12	I	**Row Data Inputs**
R5-R7	19-21	13-15	I	Port provides internal pull-up resistors
C0-C5	12-7	7-2	O	**Column Select Outputs:**
C6-C7	6-5	1,44	O	
C8-C9	31-30	26-25	O	
				Multi-function pins
C10/WUKO	29	24	I/O	C10 & "Wake-Up Keys Only" imput
C11/_LID	28	23	I/O	C11 & Lid latch detect input
				Miscellaneous functions
LED2	27	21	I/O	LED2 output
LED1	26	20	I/O	LED1 output
LED0	25	19	I/O	LED0 output
XSW	33	28	I	External discrete switch
SWO	32	27	I	Discrete switch
				Power Management Pins
_ATN	38	33	O	CPU Attention Output
_PWR_OK	39	34	I	Power OK Input
NC	3,18 23,40	39-40 16,22		**No Connects**: these pins are unused
NC0	41	35		NC0 should be tied to VSS or GND

Note 1: An underscore before a pin mnemonic denotes an active low signal.

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PIN DESCRIPTIONS

VCC and VSS

VCC and VSS are the power supply and ground pins. The UR5HCSPI will operate from a 3-5 Volt power supply. To prevent noise problems, provide bypass capacitors and place them as close as possible to the IC with the power supply. VX, where available, should be tied to Vcc.

OSCI and OSCO

OSCI and OSCO provide the input and output connections for the on-chip oscillator. The oscillator can be driven by any of the following circuits:
- Crystal
- Ceramic Resonator
- External Clock Signal
The frequency of the on-chip oscillator is 2 MHz.

_RESET

A logic zero on the _RESET pin will force the UR5HCSPI into a known start-up state. The reset signal can be supplied by any of the following circuits:
- RC
- Voltage monitor
- Master system reset

MOSI, MISO, SCK, _SS, _ATN

These five signals implement the SPI interface. The device acts as a slave on the SPI bus. The _SS (Slave Select) pin should be tied to ground if not used by the SPI master. The _ATN pin is asserted low each time the UR5HCSPI has a packet ready for delivery. For a more detailed description, refer to the SPI Communication Channel section on page 9.

_IOTEST and _WKU

"Input Output Test" and "Wake Up" pins control the stop mode exit of the device. The designer can connect any number of active low signals to these two pins through a 17K resistor, in order to force the device to exit the stop mode. A sample circuit is shown on page 15 of this document.

All the signals are "wire-anded." When any one of these signals is not active, it should be floating (i.e., these signals should be driven from "open-collector" or "open-drain" outputs). Other configurations are possible; contact Semtech.

R0-R 7

The R0-R7 pins are connected to the rows of the scanned matrix. Each pin provides an internal pull-up resistor, eliminating the need for external components.

C0-C9

C0 to C9 are bi-directional pins connected to the columns of the scanned matrix. When a column is selected, the pin outputs an active low signal. When the column is de-selected, the pin turns into high-impedance.

C10/WUKO

The C10/WUKO pin acts alternatively as column scan output and as an input. As an input, the pin detects the "Wake-Up Keys Only" signal, typically provided by the host CPU to indicate that the user has turned the unit off. When the device detects an active high state on this pin, it feeds this information into the "Keyboard State Control" unit, in order to disable the keyboard and enable the programmed wake-up keys.

C11/_LID

The C11/_LID pin acts in a similar manner to the C10/WUKO. This pin is typically connected to the LID latch through a 150K resistor, in order to detect physical closing of the device cover. When the pin detects an active low state in this input, it feeds this information into the "Keyboard State Control" unit, in order to disable keys inside the case and enable only switches located physically on the outer body of the H/PC unit.

LED0, LED1 and LED2

These three pins provide an active low drive for LED indicators. The programming of these pins is explained in the LEDs section on page 8 of this document.

PIN DESCRIPTIONS, (CON'T)

XSW

The XSW pin is dedicated to an external switch. This pin is handled differently than the rest of the switch matrix and is intended to be connected to a switch physically located on the outside of the unit.

SW0

The SW0 pin is a dedicated input pin for a switch.

PWR_OK

The PWR_OK is an active low pin that monitors the battery status of the unit. When the UR5HCSPI detects a transition from high to low on this pin, it will immediately enter the STOP mode, turn the LED off and remain in this state until the batteries of the unit are replaced and the signal is deasserted.

THE WINDOWS CE® KEYBOARD

The following illustration shows a typical implementation of a Windows CE® keyboard.

Windows CE® does not support the following keyboard keys typically found on desktop and laptop keyboards:
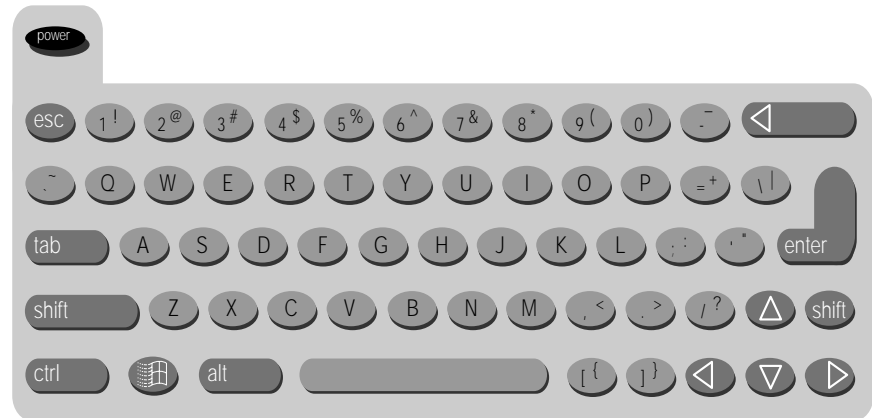
- ■ INSERT
- ■ SCROLL LOCK
- ■ PAUSE
- ■ NUM LOCK
- ■ Function Keys (F1-F12)
- ■ PRINT SCREEN

If the keyboard implements the Windows key, the following key combinations are supported in the Windows CE® environment:

Key Combination	Result
Windows	Open Start Menu
Windows+K	Open Keyboard Tool
Windows+I	Open Stylus Tool
Windows+C	Open Control Panel
Windows+E	Explore the H/PC
Windows+R	Display the Run Dialog Box
Windows+H	Open Windows CE® Help
Ctrl+Windows+A	Select all on desktop

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"GHOST" KEYS

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is sensed as being pressed. This is known as the "ghost" or "phantom" key problem.
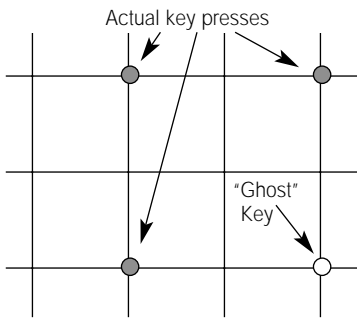

Figure 1: "Ghost" or "Phantom" Key Problem

Although the problem cannot be totally eliminated without using external hardware, there are methods to neutralize its negative effects for most practical applications. Keys that are intended to be used in combinations should be placed in the same row or column of the matrix, whenever possible. Shift Keys (Shift, Alt, Ctrl, Window) should not reside in the same row (or column) as any other keys. The UR5HCSPI has built-in mechanisms to detect the presence of "ghost" keys.

KEYBOARD SCANNER

The encoder scans a keyboard organized as an 8 row by 12 column matrix for a maximum of 96 keys. Smaller size matrixes can also be accommodated by simply leaving unused pins open. The UR5HCSPI provides internal pull-ups for the Row input pins. When active, the encoder selects one of the column lines (C0-C13) every 512 µS and then reads the row data lines (R0-R7). A key closure is detected as a zero in the corresponding position of the matrix.

A complete scan cycle for the entire keyboard takes approximately 9.2 mS. Each key found pressed is debounced for a period of 20 mS. Once the key is verified, the corresponding key code(s) are loaded into the transmit buffer of the SPI communication channel.

N-KEY ROLLOVER

In this mode, the code(s) corresponding to each key press are transmitted to the host system as soon as that key is debounced, independent of the release of other keys.

When a key is released, the corresponding break code is transmitted to the host system. There is no limitation to the number of keys that can be held pressed at the same time. However, two or more key closures, occurring within a time interval of less than 5mS, will set an error flag and will not be processed. This feature is to protect against the effects of accidental key presses.

![SEMTECH logo]

These states of operation refer only to the keyboard functionality and, although they are related to power states, they are also independent of them.

"Send All Keys"

Entry Conditions: Power on reset, soft reset, PWR_OK =1, {(LID=1) AND (WUKO=0)}

Exit Conditions: PWR_OK = 0 -> "Send No Keys"(WUKO=1) AND (Key Press) -> "Send Wake-Up Keys Only"(LID = 0) AND (WUKO=0) AND (Key Press) -> "Send XSW Key Only"

Description: This is the UR5HCSPI's normal state of operation, accepting and transmitting every key press to the system. This state is entered after the power-on and is sustained while the unit is being used.

"Send Wake-Up Keys Only"

Entry Conditions꞉ (WUKO=1) AND (Key or Switch press)

Exit Conditions: Soft Reset -> "Send All Keys"PWR_OK = 0 -> "Send No Keys"

Description꞉ This state is entered when the user turns the unit off. A signal line driven by the host will notify the UR5HCSPI about this state transition. While in this state, the UR5HCSPI will transmit only keys programmed to be wake-up keys to the system. It is not necessary for the UR5HCSPI to detect this transition in real time, since it does not effect any operation besides buffering keystrokes.
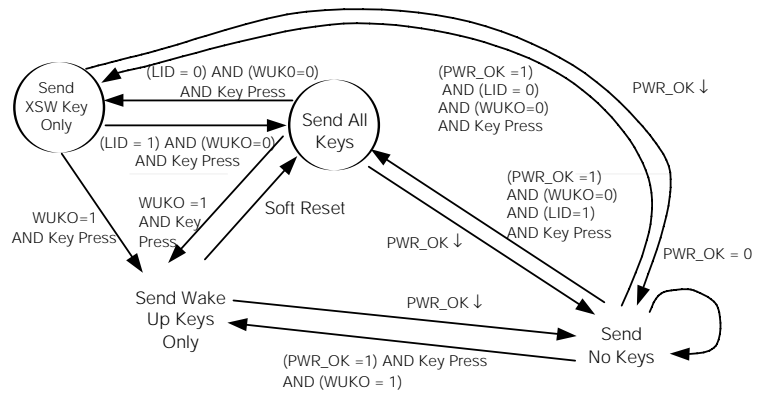

Figure 2: The UR5HCSPI implements four modes of keyboard and switch operation.

"Send No Keys"

Entry Conditions꞉PWR_OK transition from high to low

Exit Conditions: (PWR_OK = 1) AND (Matrix key pressed OR Switch OR _WKUP)

Description: This state is entered when a PWR_OK signal is asserted (transition high to low), indicating a critically low level of battery voltage. The PWR_OK signal will cause an interrupt to the UR5HCSPI, which guarantees that the transition is performed in real time. While in this state, the UR5HCSPI will perform as follows:

1. The LED will be turned off. Nevertheless, its state is saved and will be restored after exiting the disabled state (change of batteries).

2. The UR5HCSPI will enter the STOP mode for maximum energy conservation.

3. Stop mode time-out entry will be shortened to further conserve energy.

4. While in this state all interrupts are disabled. The UR5HCSPI will exit this state on the next interrupt event that detects the PWR_OK line has been de-asserted.

"Send XSW Key Only"

Entry Condition: (LID=0) AND (WUKO=0) AND (Key Press)

Exit Condition: (LID=1) AND (WUKO=0) AND (Key Press) -> "Send All Keys"PWR_OK = 0 -> "Send No Keys" (WUKO = 1) AND (Key Press) -> "Send Wake Up Keys Only"

Description: This state is entered upon closing the lid of the device. While in this state, the encoder will transmit only the XSW key, which is located outside the unit. This feature is designed to accommodate buttons on the outside of the box, such as a microphone button, that need to be used while the lid is closed.

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Key codes range from 01H to 73H and are arranged as follows:

Make code = column_number * 8 + row_number + 1

Break code = Make code OR 80H

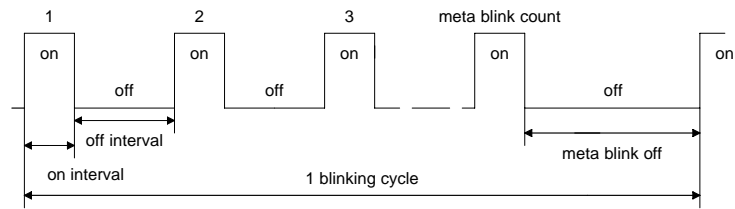Discrete Switches transmit the following codes:

XSW = 71H

SW0 = 72H

Figure 3: The behavior of an LED using the settings 1: LED on; 0: LED off.

The UR5HCSPI provides three LED pins. There are three LED modes: off, on, and blinking. The LED can be individually set to one of these modes. In the Blinking Mode, both the on-interval and the off-interval can be individually set. Additionally, a meta blink count and meta blink interval may be specified. This describes an interval of a different length which may be inserted after each specified number of blinks. All the intervals are based on a 1/16th of a second duration. When the LED is on or blinking, the SPICoder™ will not enter the STOP Mode unless the PWR_OK signal is asserted low. In this case, the device will save the status of the LED and turn it off. The default LED mode is off.

The above timing chart describes the behavior of an LED using these settings,1: LED on; 0: LED off.

SPI COMMUNICATION CHANNEL

SPI data transfers can be performed at a maximum clock rate of 500 KHz. When the UR5HCSPI asserts the _ATN signal to the host Master, the data will have already been loaded into the data register waiting for the clocks from the master. The Slave Select (SS) line can be tied permanently to Ground if the UR5HCSPI is the only slave device in the SPI network. One _ATN signal is used per each byte transfer. If the host fails to provide clock signals for successive bytes in the data packet within 120 mS, the transmission will be aborted and a new session will be initiated by asserting a new ATN signal. In this case, the whole packet will be re-transmitted.

If the SPI transmission fails 20 times consecutively, the synchronization between the master and slave may be lost. In this case, the UR5HCSPI will enter the reset state.

The UR5HCSPI implements the SPI communication protocol according to the following diagram:

CPOL = 0 ---------- SCK line idles in low state

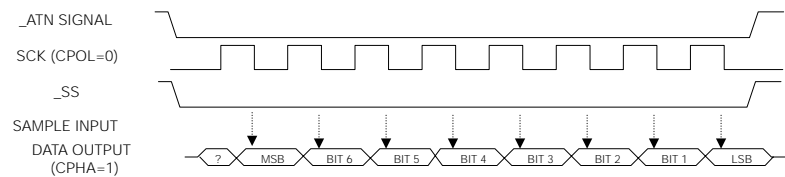CPHA = 1 ---------- SS line is an output enable control

Figure 4: SPI Communication Protocol

When the host sends commands to the keyboard, the UR5HCSPI requires that the minimum and maximum intervals between two successive bytes be 200 µS and 5 mS respectively.

Figure 5: Transmitting Data Waveforms:

Figure 6: Receiving Data Waveforms

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DATA/COMMAND BUFFER

The UR5HCSPI implements a data buffer that contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer will be cleared and an "Initialize" command will be sent to the host. At the same time, the keyboard will be disabled until the "Initialize" or "Initialize Complete" command from the host is received.
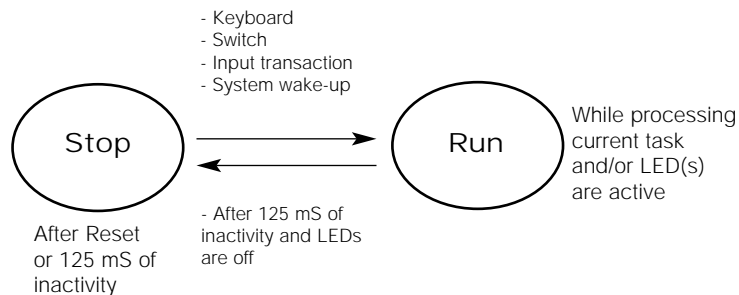
POWER MANAGEMENT UNIT

The UR5HCSPI supports two modes of operation. The following table lists the typical and maximum supply current (no DC loads) for each mode at 3.3 Volts (+/- 10%).

Current	Typical		Max	Unit	Description
RUN	1.5	1	3.0	mA	Entered only while data/commands are in process and if the LEDs are blinking
STOP	2.0		20	µA	Entered after 125 mS of inactivity if LEDs islow

Power consumption of the keyboard sub-system will be determined primarily by the use of the LEDs. While the UR5HCSPI is in the STOP mode, an active low Wake-Up Output from the Master must be connected to the edge-sensitive _WKU pin of the UR5HCSPI. This signal will be used to wake up the UR5HCSPI in order to receive data from the Master host. The Master host will have to wait a minimum of 5 mS prior to providing clocks to the UR5HCSPI. The UR5HCSPI will enter the STOP mode after a 125 mS period of keypad and/or host communications inactivity, or anytime the PWR_OK line is asserted low by the host. Note that while one or more keys are held pressed, the UR5HCSPI will not enter the STOP mode until every key is released.

Figure 7: The power states of the UR5HCSPI

- Keyboard
- Switch
- Input transaction
- System wake-up

Stop

Run

While processing current task and/or LED(s) are active

After Reset or 125 mS of inactivity

- After 125 mS of inactivity and LEDs are off

COMMUNICATION PROTOCOL

There are eight commands that may be sent from the UR5HCSPI to the host, and ten commands that may be sent from the host to the UR5HCSPI.

Each command from UR5HCSPI to the host is composed of a sequence of codes. All commands start with <CONTROL> code (80H) and end with LRC code (see the description of the LRC calculation on page 12). Command details are listed below.

Commands to the Host - Summary

Command Name	Code	Description
Initialize Request	AOH	Sent to the host when the data buffer is full
Initialize Complete	A1H	Issued upon completion of the "Initialize" command issued by the host
Heartbeat Response	A2H	Response to "Heartbeat Request" issued by the host
Identification Response	F2H	Response to "Identification Request" issued by the host
LED Status Report	A3H	Response to "LED Status Request"
Resend Request	A5H	Issued upon error during the reception of a packet

LRC CALCULATION

The LRC is calculated for the whole packet, including the Command Code and the Command Prefix. The LRC is calculated by first taking the bitwise exclusive OR of all bytes from the message. If the most significant bit (MSB) of the LRC is set, the LRC is modified by clearing the MSB and changing the state of the next most significant bit. Thus, the Packet Check Byte will never consist of a valid LRC with the most significant bit set.

COMMANDS TO THE HOST ANALYTICALLY

Initialize Request

<CONTROL>	80H
<INIT>	A0H
<LRC>	20H

The UR5HCSPI will send the Initialize Request Command to the host when its data buffer is full.

Initialization Complete

<CONTROL>	80H
<INIT COMPLETE>	A1H
<LRC>	21H

The UR5HCSPI wil send the Initialize Complete Report to the host when it finishes the initialization caused by Initialize Command from the host.

Heartbeat Response

<CONTROL>	80H
<ONLINE>	A2H
<LRC>	22H

The UR5HCSPI will send the Heartbeat Response to the host when it receives the Heartbeat Request Command from the host.

Identification Response

<CONTROL>	80H	
<ID>	F2H	
<Vendor>	02H	--- USAR
<Revision>	08H	--- Rev 0.8A
<Switch>	00H	.
<LRC>	7EH	

The UR5HCSPI will send the Identification Response to the host when it receives the Identification Request Command from the host.

The following C language function is an example of an LRC calculation program. It accepts two arguments: a pointer to a buffer and a buffer length. Its return value is the LRC value for the specified buffer.

```c
char Calculate LRC (char buffer, size buffer)
{
char LRC;
size_t index;
/*
* Init the LRC using the first two message bytes.
*/
LRC = buffer [0] ^ buffer [1];
/*
* Update the LRC using the remainder of the buffer.
*/
for (index = 2; index < buffer; index ++)
  LRC ^ = buffer[index];
/*
* If the MSB is set then clear the MSB and change the next most significant bit
*/
if (LRC & 0x80)
LRC ^ = 0xC0;
/* * Return the LRC value for the buffer.*/}
```

LED Status Report

<CONTROL>	80H
<LED>	A3H
<Status 0>	xxH LED0 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<Status 1>	xxH LED1 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<Status 2>	xxH LED2 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<LRC>	xxH

The UR5HCSPI will send the LED Status Report to the host when it receives the LED Status Request Command from the host.

Resend Request

<CONTROL>	80H
<RESEND>	A5H
<LRC>	25H

The UR5HCSPI will send this Resend Request Command to the host when its command buffer is full, or if it detects either a parity error or an unknown command during a system command transmission.

COMMANDS FROM THE HOST TO THE UR5HCSPI

Commands from the Host - Summary

Command Name	Code	Description
Initialize	AOH	Causes the UR5HCSPI to enter the power-on state
Initialization Complete	A1H	Issued as a response to the "Initialize Request"
Heartbeat Request	A2H	The UR5HCSPI will respond with "Heartbeat Response"
Identification Request	F2H	The UR5HCSPI will respond with "Identification Response"
LED Status Request	A3H	The UR5HCSPI will respond with "LED Status Response"
LED Modify	A6H	The UR5HCSPI will change the LED accordingly
Resend Request	A5H	Issued upon error during the reception of a packet
Input/Output Mode Modify	A7H	The UR5HCSPI will modify or report the status of the GIO0 pin
Output Data to I/O pin	A8H	The UR5HCSPI will output a signal to the GIO0 pin
Set Wake-Up Keys	A9H	Defines which keys are "wake-up" keys

Each command to UR5HCSPI is composed of a sequence of codes. All commands start with <ESC> code (1BH) and end with the LRC code (bitwise exclusive OR of all bytes).

COMMANDS FROM THE HOST TO THE UR5HCSPI ANALYTICALLY

Initialize

<ESC>	1BH
<INIT>	A0H
<LRC>	7BH

When the UR5HCSPI receives this command, it will clear all buffers and return to the power-on state.

Initialization Complete

<ESC>	1BH
<INIT COMPLETE>	A1H
<LRC>	7AH

When the UR5HCSPI receives this command, it will enable transmission of keyboard data. Keyboard data transmission is disabled if the TX output buffer is full (32 bytes). Note that if the transmit data buffer gets full the encoder will issue an "Initialize Request" to the host.

Heartbeat Request

<ESC>	1BH
<ONLINE>	A2H
<LRC>	79H

When the UR5HCSPI receives this command, it will reply with the Heartbeat Response Report.

Identification Request

<ESC>	1BH
<ID>	F2H
<LRC>	29H

The UR5HCSPI will reply to this command with the Identification Response Report.

Set Wake-Up Keys

<ESC>	1BH
<SETMATRIX>	A9H
<COL0>	xxH (R7

R6 R5 R4 R3 R2 R1 R0 Bitmap: 0-enabled, 1-disabled)

<COL1>	xxH
<COL2>	xxH
<COL3>	xxH
<COL4>	xxH
<COL5>	xxH
<COL6>	xxH
<COL7>	xxH
<COL8>	xxH
<COL9>	xxH
<COL10>	xxH
<COL11>	xxH
<SWITCHES>	xxH
<LRC>	xxH

The "Set Wake-Up Keys" command is used to disable specific keys from waking up the host. Using this command, the host can set only a group of keys.

LED Status Request

<ESC>	1BH
<LED>	A3H
<LRC>	78H

When UR5HCSPI receives this command, it will reply with the LED Status Report.

LED Modify

<ESC>	1BH	
<MODLED>	A6H	
<LED NUMBER>	xxH	LED number (0)
<LED STATE>	xxH	(0=LED OFF; 1=LED ON; 2=LED BLINKING)
<ON INTERVAL>	xxH	Time in 1/16ths of a second for LED to be on
<OFF INTERVAL>	xxH	Time in 1/16ths of a second for LED to be off
<META COUNT>	xxH	Number of blinks after which to apply meta blink interval
<META INTERVAL>	xxH	Time in 1/16ths of a second for LED to be off after <META COUNT> blinks
<LRC>	xxH	

When the UR5HCSPI receives this command, it will change the LED mode accordingly.

UR5HCSPI-FB

Telcom
TC54C4302ECB

Alternatively an RC circuit
or Master Reset Signal
can be used

Slave Select
Tied to Gnd
if not used

Attention Signal

Power OK Signal

Ceramic resonator circuit
with built in capacitors
Alternatively a 2MHz CMOS
signal can be tied directly
to OSC1

Power OK
Signal

Wake Up
Signal
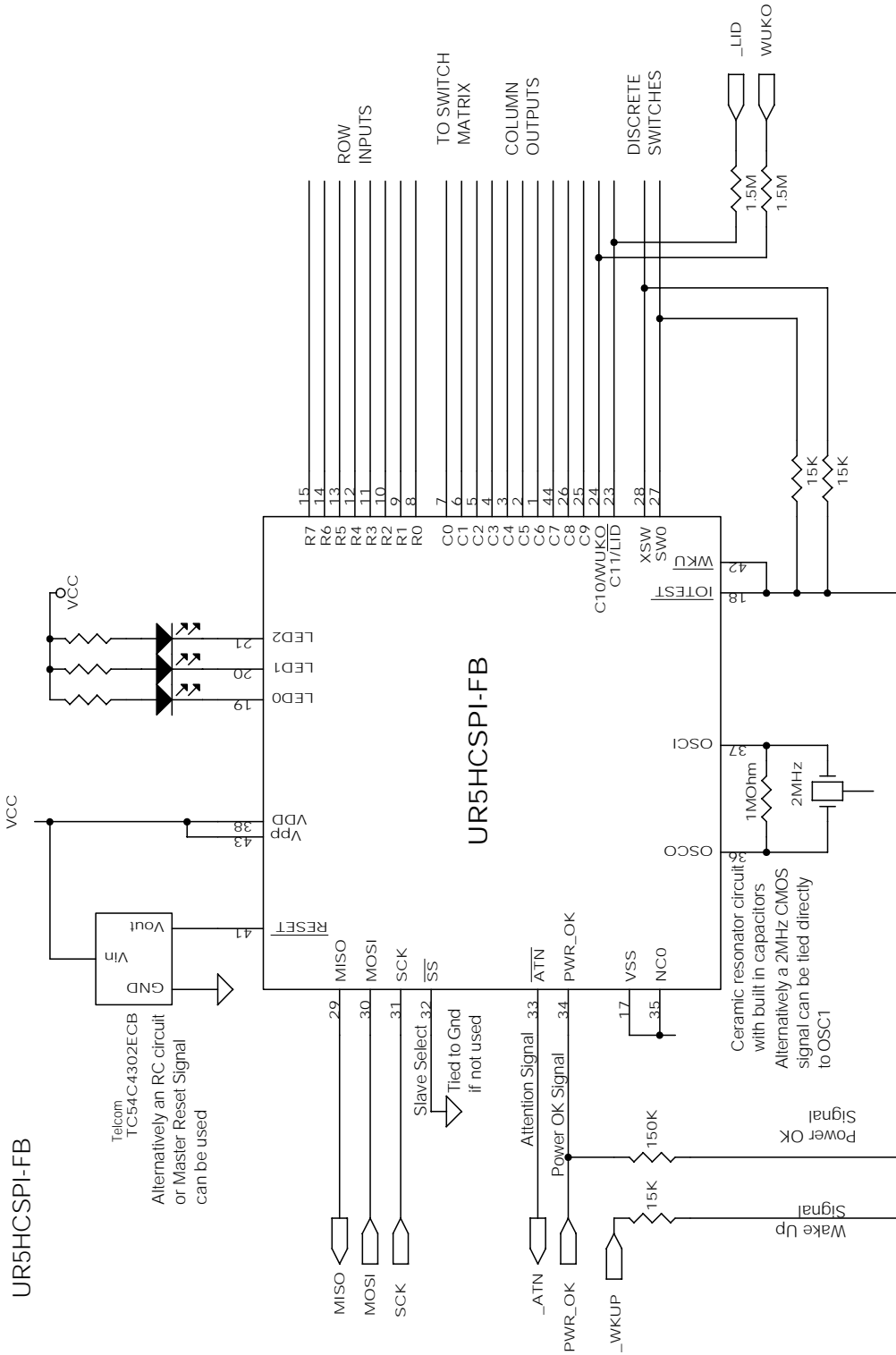
UR5HCSPI-FB V0.9
(c) 2000, USAR, A Semtech Co.

ROW
INPUTS

TO SWITCH
MATRIX

COLUMN
OUTPUTS

DISCRETE
SWITCHES

The following notes pertain to the suggested schematic found on the previous page.

The Built-in Oscillator on the UR5HCSPI-06 requires the attachment of the 2.00 MHz Ceramic Resonators with built-in Load Capacitors.. You can use either an AVX, part number PBRC-2.00 BR; or a Murata part number CSTCC2.00MG ceramic resonator.

It may also be possible to operate with the 2.00 MHz Crystal, albeit with reduced performance. Due to their high Q, the Crystal oscillator circuits start-up slowly. Since the SPICoder™ constantly switches the clock on and off, it is important that the Ceramic Resonator is used (it starts up much quicker than the Crystal). Resonators are also less expensive than Crystals.

Also, if Crystal is attached, two Load Capacitors (33pF to 47pF) should be added, a Capacitor between each side of the Crystal and ground.

In both cases, using Ceramic Resonator with built-in Load Capacitors, or Crystal with external Load Capacitors, a feedback Resistor of 1 Meg should be connected between OSCIN and OSCOUT.

Troubleshoot the circuit by looking at the Output pin of the Oscillator. If the voltage is half-way between Supply and Ground (while the Oscillator should be running) --- the problem is with the Load Caps / Crystal. If the voltage is all the way at Supply or Ground (while the Oscillator should be running) --- there are shorts on the PCB.

Note: When the Oscillator is intentionally turned OFF, the voltage on the Output pin of the Oscillator is High (at the Supply rail).

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	Vdd	-0.3 to +7.0	V
Input Voltage	Vin	Vss -0.3 to Vdd +0.3	V
Current Drain per Pin (not including Vss or Vdd)	I	25	mA
Operating Temperature UR5HCSPI	Ta	T low to T high -40 to +85	° C
Storage Temperature Range	Tstg -	-65 to +150	° C

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance	Tja		°C per W
■ Plastic		60	
■ PLCC		70	

DC Electrical Characteristics (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I load<10µA)	Vol			0.1	V
	Voh	Vdd–0.1			
Output High Voltage (I load=0.8mA)	Voh	Vdd–0.8			V
Output Low Voltage (I load=1.6mA)	Vol:			0.4	V
Input High Voltage	Vih	0.7xVdd		Vdd	V
Input Low Voltage	Vil	Vss		0.2xVdd	V
User Mode Current	Ipp		5	10	mA
Data Retention Mode (0 to 70°C)	Vrm	2.0			V
Supply Current (Run)	Idd		1.53	3.0	mA
(Wait)			0.711	1.0	mA
(Stop)			2.0	20	µA
I/O Ports Hi-Z Leakage Current	Iil			+/-10	µA
Input Current	Iin			+/- 1	µA
I/O Port Capacitance	Cio		8	12	pF

Control Timing (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation	fosc			MHz
■ Crystal Option			2.0	
■ External Clock Option		dc	2.0	
Cycle Time	tcyc	1000		ns
Crystal Oscillator Startup Time	toxov		100	ms
Stop Recovery Startup Time	tilch		100	ms
RESET Pulse Width	trl	8		tcyc
Interrupt Pulse Width Low	tlih	250		ns
Interrupt Pulse Period	tilil	*		tcyc
OSC1 Pulse Width	toh, tol	200		ns

*The minimum period tlil should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 tcyc.

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SPICODER™ BILL OF MATERIALS

UR5HCSPI-FB

Quantity	Manufacturer	Part#	Description
3	Generic	330 Ohms	330 Ohms Resistor
3	Generic	LED	Led used as LED1. LED2. LED3
3	Generic	15 K	15 K Resistors
1	Generic	150 K	150 K Resistors
1	Generic	1M	1M Resistors
2	Generic	1.5 K	1.5 K Resistors
1	TELCOM	TC54VC4302ECB713	IC Volt Detector CMOS 4.3V SOT23, for 5V Operation
		TC54VC2702ECB713	IC Volt Detector CMOS 2.7V SOT23, for 3.3V Operation
1	AVX	PBRC-2.00BR	2.00MHZCeramic Resonator with Built in Capacitors, SMT

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