Juno™ A4 UR8HC007-0A4

Zero-Power™ Input Device and Power Management IC

HID & SYSTEM MANAGEMENT PRODUCTS, H/PC IC FAMILY

DESCRIPTION

The Juno™ A4 is a member of a series of input device and power management companion ICs for RISC-based portable systems. On a single IC, the Juno™ A4 integrates control of any 4-wire or 8-wire resistive touch screen, keyboard scanning, unique power management capabilities, a direct PS/2 port and plenty of General Purpose Input / Output (GPIO).

The Juno™ A4 provides continuous operation between 3V and 5V and scans a fully programmable 8 X 16 keyboard matrix. The IC is equipped with a direct Zero-Power™ PS/2 port for the hot-plug connection of an external PS/2 keyboard or mouse.

The Zero-Power™ Juno™ A4 will power down even between key presses. Proprietary circuitry (patent pending) allows the IC to power down even when the PS/2 device is connected and active. Typical power consumption is less than 1 µA, a first for embedded ICs.

The Juno™ A4 is equipped with a proprietary protocol developed specifically for RISC-based handheld machines. It interfaces the system via either asynchronous serial (UART) or the Serial Peripheral Interface (SPI).

The integration of features, many of them programmable, on one IC increases flexibility and reduces component count and cost.

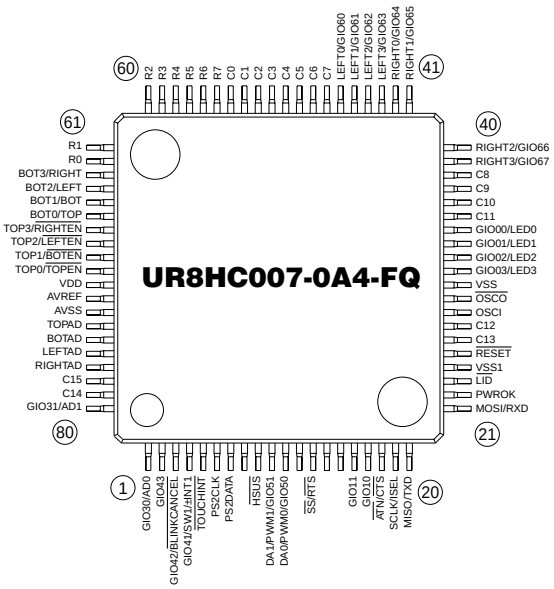
FEATURES

- Typically consumes less than 1µA
- Scans an 8 x 16 keyboard matrix that supports Japanese, English and European keyboards
- Interfaces any four-wire or eight-wire resistive touch screen
- Operates continuously between 3 Volts and 5 Volts
- Offers unique power management capabilities that work in harmony with Windows® CE power modes
- Always runs in "Stop" mode without data or event loss
- Provides a direct Zero-Power™ PS/2 port for the hot-plug connection of an external keyboard or mouse
- Uses proprietary circuitry, so “Stop” mode is entered even when PS/2 device is connected & active
- GPIO pins provide interrupt at both falling and rising edge of signals, ideal for lid functions, power, ring indicators, docking signals, battery measurement, etc.
- Has additional GPIO available for LEDs, switches, etc.
- Offers internal control of LCD brightness/contrast, audio, etc. as well as four 10-bit A/D channels for power management monitoring
- Provides programmable features that allow for maximum design differentiation without customization
- Cost-effective, reducing overall system costs by integrating features that would typically require multiple components
- Available in 80-pin 13 x 13 mm, 1.7mm high package to accommodate slim designs

APPLICATIONS

- Jupiter-class devices
- Professional H/PCs
- H/PCs
- Web Phones, G3 Terminals

PIN ASSIGNMENTS



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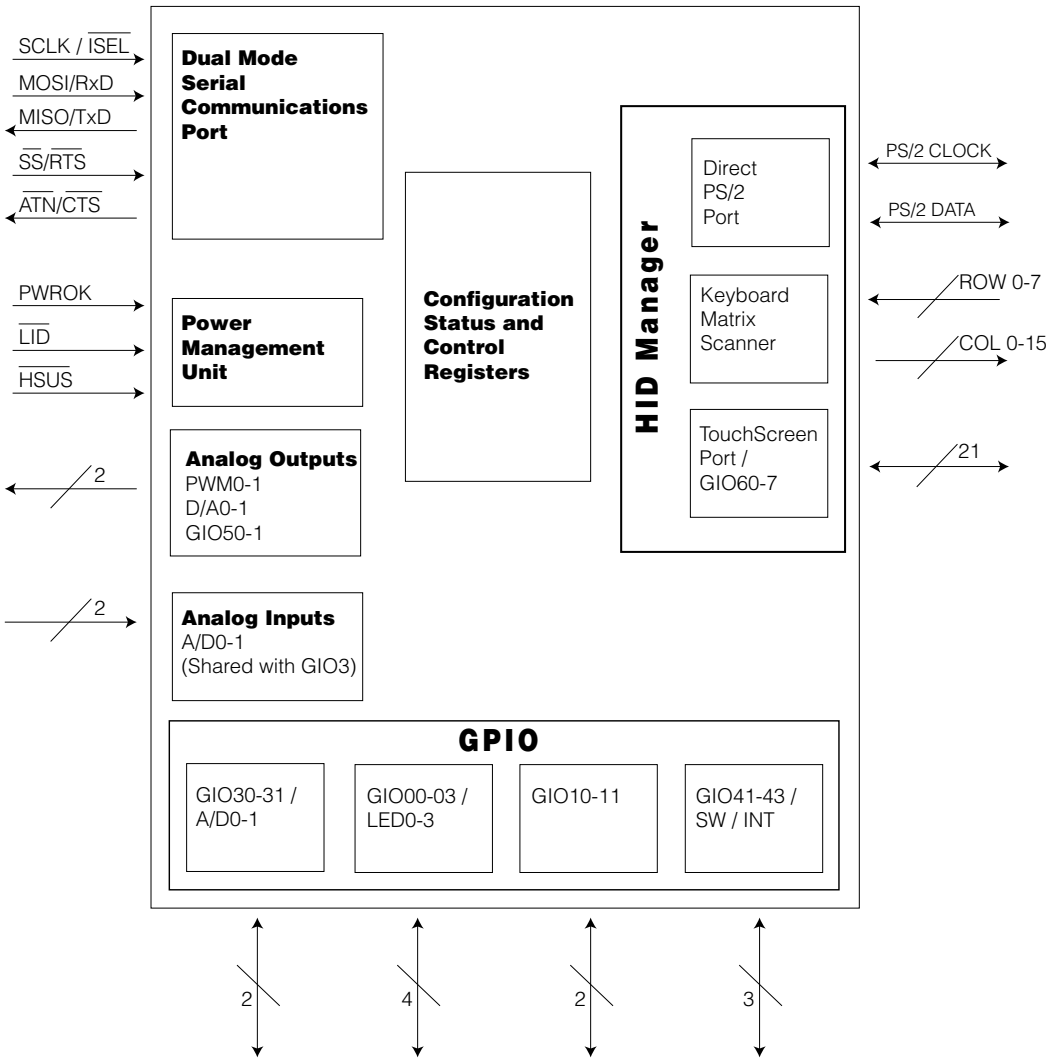
ORDERING CODE

Package Options	Pitch in mm's	TA = 0° C to +75° C
80-pin, Plastic LQFP	0.5	UR8HC007-0A4-XX-FQ

Other Materials	Type	Order number
Technical Reference Manual	Document	DOC8-007-0A4-TR-XXX
Juno™ A4 Eval. Kit	Evaluation Kit	EVK8-007-0A4-XXX
Evaluation Kit Data Sheet	Document	DOC8-007-0A4-EK-XXX

Note 1: XX= Optional for customization; XXX= Denotes revision number

BLOCK DIAGRAM



PIN DEFINITIONS

Pin Numbers

Mnemonic	QFP	Typ	Name and Function
Power Supply			
VDD	71	PWR	**Positive Supply Voltage**
AVREF	72	AI	**Positive analog reference voltage**
AVSS	73	PWR	**Ground**: analog signal
VSS	30	PWR	**Ground**: negative supply voltage
VSS1	24	PWR	**Auxiliary Ground**; must be tied to pin 30
Reset			
_RESET	25	I	**Controller hardware reset pin**: when at Low-level, this pin holds the UR8HC007in a reset state. This pin must be held at a logic-low until Power Supply voltage (VDD) reaches the minimum operating level (2.7V).
Oscillator pins			
OSCI	28	I	**Oscillator input**: connect ceramic resonator with built-in load capacitors or CMOS clock from external oscillator
_OSCO	29	O	**Oscillator Output**: connect ceramic resonator with built-in load capacitors or keep open if external oscillator is used
Scanned matrix pins			
ROW0-ROW7	62-55	I	**Row matrix outputs**
COL0-COL7	54-47	I/nD	**Column matrix outputs**
COL8-COL11	38-35		
COL12-COL13	27-26		
COL14-COL15	79-78		

PIN DEFINITIONS, (CON'T)

Pin Numbers Mnemonic	QFP	Type	Name and Function
General Purpose Input/Ouput			
GIO0			
GIO00/LED0-GIO3/LED3	34-31	I/O	General purpose input/output pin LED driver
GIO1			
GIO10-GIO11	17-16	I/O	General purpose input/output pin,
GIO3 - analog input			
GIO30/AD0	1	I/O/Ai	General purpose input/output pin, A/D input 0
GIO31/AD1	80	I/O/Ai	General purpose input/output pin, A/D input 1
GIO4			
GIO41/SW1/±INT1	4	I/O, I±Int	General purpose input/output pin, switch Input. Capable of interrupt on both positive and negative edges
GIO42/_BLINKCANCEL	3	I/O	General purpose input/output pin; negative input cancels all LED blinking, unless blink-cancel function disabled in register
GIO43	2	I/O	General purpose input/output pin
GIO5 - analog output			
DA0/PWM0/GIO50	11	Ao	D/A output (Range: AVSS to AVREF)
DA1/PWM1/GIO51	10	Ao	D/A output (Range: AVSS to AVREF)
Touch Screen interface			
RIGHT3/GIO67	39	I/O	If no hardware touchscreen driver, drive output to right side of touchscreen; otherwise general purpose I/O
RIGHT2/GIO66	40	I/O	If no hardware touchscreen driver, drive output to right side of touchscreen; otherwise general purpose I/O
RIGHT1/GIO65	41	I/O	If no hardware touchscreen driver, drive output to right side of touchscreen; otherwise general purpose I/O
RIGHT0/GIO64	42	I/O	If no hardware touchscreen driver, drive output to right side of touchscreen; otherwise general purpose I/O
LEFT3/GIO63	43	I/O	If no hardware touchscreen driver, drive output to left side of touchscreen; otherwise general purpose I/O
LEFT2/GIO62	44	I/O	If no hardware touchscreen driver, drive output to left side of touchscreen; otherwise general purpose I/O
LEFT1/GIO61	45	I/O	If no hardware touchscreen driver, drive output to left side of touchscreen; otherwise general purpose I/O
LEFT0/GIO60	46	I/O	If no hardware touchscreen driver, drive output to left side of touchscreen; otherwise general purpose I/O

PIN DEFINITIONS, (CON'T)

Pin Numbers Mnemonic	QFP	Type	Name and Function
BOT3/RIGHT	63	O	If no hardware touchscreen driver, drive output to bottom side of touchscreen; otherwise output for right side of touchscreen
BOT2/LEFT	64	O	If no hardware touchscreen driver, drive output to bottom side of touchscreen; otherwise output for left side of touchscreen
BOT1/BOT	65	O	If no hardware touchscreen driver, drive output to bottom side of touchscreen; otherwise output for bottom side of touchscreen
BOT0/TOP	66	O	If no hardware touchscreen driver, drive output to bottom side of touchscreen; otherwise output for top side of touchscreen
TOP3/_RIGHTEN	67	O	If no hardware touchscreen driver, drive output to top side of touchscreen; otherwise enable output to right side of touchscreen
TOP2/_LEFTEN	68	O	If no hardware touchscreen driver, drive output to top side of touchscreen; otherwise enable output to left side of touchscreen
TOP1/_BOTEN	69	O	If no hardware touchscreen driver, drive output to top side of touchscreen; otherwise enable output to bottom side of touchscreen
TOP0/_TOPEN	70	O	If no hardware touchscreen driver, drive output to top side of touchscreen; otherwise enable output to top side of touchscreen
_TOUCHINT	5	I	Touchscreen interrupt input
RIGHTAD	77	Ai	A/D input from right side of touchscreen
LEFTAD	76	Ai	A/D input from left side of touchscreen
BOTAD	75	Ai	A/D input from bottom side of touchscreen
TOPAD	74	Ai	A/D input from top side of touchscreen
System and Power Management			
_LID	23	I±Int	Lid closed signal from the lid switch (active-low). Capable of interrupt on both positive and negative edges
PWROK	22	I±Int	Power OK signal. Capable of interrupt on both positive and negative edges
_HSUS	9	I	Host Suspended signal (active-low). When "Low," indicates that host computer system is in power-reduced or Stop mode.

PIN DEFINITIONS, (CON'T)

Pin Numbers Mnemonic	QFP	Type	Name and Function
Host Communication Interface			
_SS/_RTS	13	I_Int	Slave_Select (SPI Mode) or Ready_To_Send (Asynchronous Serial Mode). Active-Low signal Input. Low-level indicates that the Host System has data for the UR8HC007 peripheral device or the Host System is ready to accept data from the UR8HC007 peripheral device. Capable of Interrupt on Negative edge. Pin 60 and pin 18 should both be "Low" for data exchange to occur.
_ATN/_CTS	18	O	Attention (SPI Mode) or Clear_To_Send (Asynchronous Serial Mode). Active-Low signal Output. Low-level indicates that the UR8HC007 peripheral device has data for the Host System or the UR8HC007 peripheral device is ready to accept data from the Host System. Pin 18 and pin 60 should both be "Low" for data exchange to occur.
MISO/TXD	20	I/O / O	Master-In-Slave-Out (SPI Mode) or Transmit Data (Asynchronous Serial Mode, Idle = "High" = 1)
MOSI/RXD	21	I	Master-Out-Slave-In (SPI Mode) or Receive Data (Asynchronous Serial Mode)
SCLK/_ISEL	19	I	Serial Clock (SPI Mode) or Interface Select (Asynchronous Serial Mode). Tie "Low" to select Asynchronous Serial Mode. In SPI Mode, use the following Clock sequence: Idle-High / Negative-Edge (Shift Data) \ Positive-Edge (Latch Data), Idle-High.
PS/2 Port			
PS2CLK	6	15V/ nD5V	PS/2 Clock line
PS2DATA	7	15V/ nD5V	PS/2 Data line

Note 2: An underscore before a pin mnemonic denotes an active low signal.
Pin Types Legend: PWR= Power; Ai=Analog Input; Ao= Analog Output; I=Digital Input; I_Int=Digital Input capable of generating interrupts on a positive to negative edge transition; I±Int=Digital Input capable of generating interrupts on either a positive or a negative edge transition of the input signal; Ipup= Digital Input with built-in Pull-up to VDD; O=Output; pD= p-channel open Drain Output (switch to VDD); I/O=Input or Output (Bidirectional pin); nD= n-channel open Drain Output (switch to VSS); 15V= 5 Volt tolerant input (even if VDD is less than 5V); nD5V=5 Volt tolerant n-channel open Drain Output.

The Juno™ family of controllers implements two modes of serial communications: The "Synchronous Peripheral Interface" (SPI) mode and the "Asynchronous Serial Mode" (UART).

The SPI is a synchronous bi-directional, multi-slave interface that supports bit rates up to 500 Kb/s. Several Hosts and companion chips implement the SPI protocol in order to communicate with a wide range of peripherals such as EEPROMs, A/D converters, MCUs and other system components. Alternatively, the SPI may be implemented through software on the Host side.

The Juno™ family implements the _ATN as an additional hand-shake signal in order to support low power operation of the bus.

Asynchronous Serial Mode is a UART-type interface that operates at a fixed baud rate of 62.5 Kb/s.

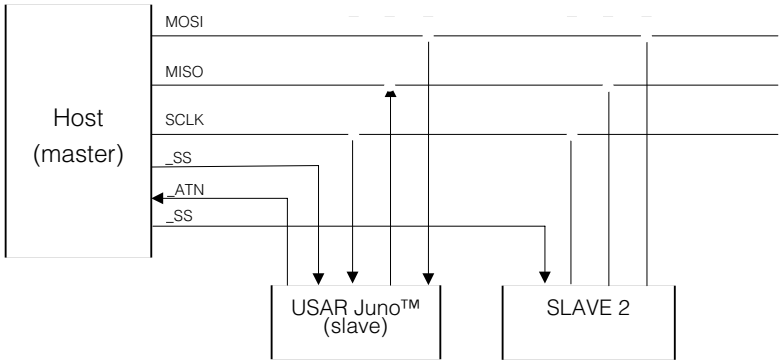
Both interfaces are implemented through the same set of four pins.

The IC determines the mode of communication with the Host during power-up by reading the value of the SCLK/ISEL pin. If the pin is tied low, asynchronous mode is enabled. If it is high, the SPI interface is enabled.

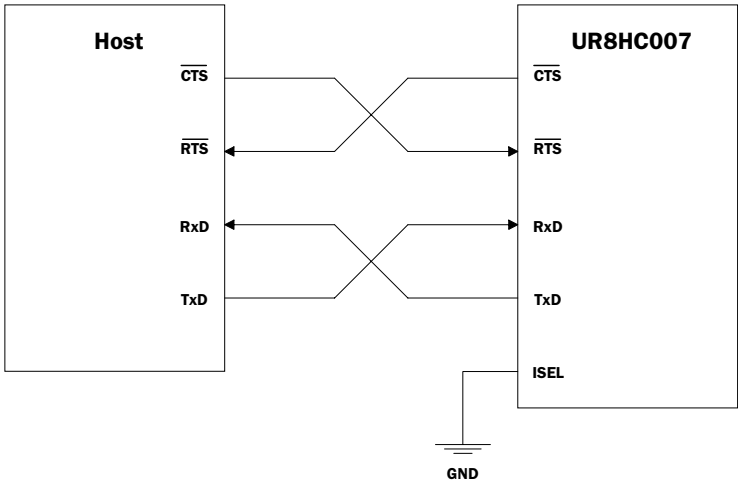
Please refer to the *Juno™ A4 Technical Reference Manual* for a description of handshake and critical timing parameters for each interface.

The diagrams below describe the SPI and asynchronous communications interfaces, respectively.

SPI Communications Interface



Asynchronous Communications Interface



Overview

The Juno™ UR8HC007-0A4 implements and supports four types of transaction messages.

1. Commands from the IC to the Host system

2. Commands from the Host system to the IC

3. Human Input Device (HID) reports to the system

4. Event Alert messages to the system

The protocol is fundamentally implemented through a set of general packet commands that allow handling and reporting of each individual controller register and each bit within each register. In this manner, the system achieves maximum flexibility in manipulating the operation of the UR8HC007-0A4 controller.

General Message Structure

Communications between the Juno™ UR8HC007-0A4 and the Host processor are implemented using a set of packet protocols and commands. The general structure of a message is shown in the following diagram:

Protocol Header
Command/Report Identifier
Message Body (if applicable)
LRC

General Message Format

The Protocol Header identifies the type of transaction. The following table lists the available protocols.

Protocol Headers

Protocols used in commands issued by the Host

Protocol	Header
Simple Commands	80H
Write Register bit	81H
Read Register bit	82H
Write Register	83H
Read Register	84H
Write Block	85H
Read Block	86H

Protocols used in responses, reports and alerts issued by the controller

Protocol	Header
Simple Commands	80H
Report Register bit & Event Alerts	81H
Report Register	83H
Report Block	85H
Relative Pointer Data Report	87H
Keyboard PS/2 Code Data Report	88H
Absolute Pointer Data Report	89H
Keyboard Key Code (position) Report	8AH

HID Data Report

The Pointing Device Data Reports format covers both absolute (where applicable) and relative positioning devices. In addition, it provides support for MouseWheel-type of input devices.

Keyboard Data Report

The Keyboard Data Reports return changes on the keyboard matrix or the External PS/2 keyboard device. The report includes a make or break bit, a column number, and a row number.

LRC (Longitudinal Redundancy Check)

The LRC is calculated for the whole packet, including the Protocol Header. The LRC is calculated by first taking the bitwise exclusive OR of all bytes from the message. If the most significant bit (MSB) of the LRC is set, the LRC is modified by clearing the MSB and changing the state of the next most significant bit. Thus, the Packet Check Byte will never consist of a valid LRC with the most significant bit set.

General Commands Format

For protocols used by either the host or the UR8HC007, a set of simple commands is implemented. These support the basic communication protocol and handle reset and errors in transmission.

A simple command would have the following structure:

Header (80H)
Command Code
LRC

Simple Command Structure

Following is a summary of the simple commands used by both the Host and the UR8HC007-0A4:

Simple Commands Summary

Command	Protocol	Cmd Code	Description
Initialize	Simple	20H	Forces the recipient to enter the known default power-on state
Initialization Complete	Simple	21H	Issued as a hand-shake response only to the "Initialize" command.
Resend Request	Simple	25H	Issued upon error in the reception of a package. The recipient will resend the last transmitted packet

The Juno™ A4 implements a set of internal registers that can be used to control and monitor the operation of the various functional units of the controller IC. These registers can be accessed through the Read/Write Register commands described in the Commands section of the *Juno™ A4 Technical Reference Manual*. The register architecture of the Juno™ A4 allows for maximum flexibility and expandability of the controller operation. At the same time, by using the default values for each register, a system can utilize all the basic functionality of the IC controller with minimum Host driver intervention.

Registers' Page Organization

Figure 1: Registers' Page Organization

POWER MANAGEMENT MODES OF OPERATION

The Juno™ family has three modes of operation relating to its power consumption.

The "Stop" mode is the lowest power consumption mode. In this mode, the crystal is stopped and the IC consumes only 1 µA of leakage current. This is the default mode to which the IC will revert any time an event or a signal condition does not force it to exit this mode.

The "Wait" mode is entered each time it is necessary for a timer to be running in order to perform a system function. Such functions include the LED blinking mode and the use of one of the PWM channels. Typical power consumption in this mode is several hundred µAs.

The "Run" mode is entered briefly, only to process an event or while an interrupt-generating signal condition persists. The controller IC will remain in this mode only for as long a signal prohibits it from reentering a lower power consumption mode or for as long as it is necessary to process a Host-related transaction (a few milliseconds).

POWER MANAGEMENT

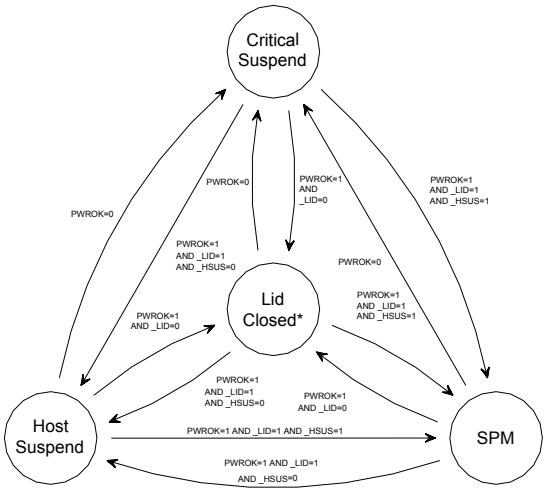
The Juno™ UR8HC007 family of controllers implements two power management methods: system-coordinated power management and Self-Power Management™ (SPM).

System-coordinated power management primarily determines the tasks performed and the type of reports communicated to the Host. The Juno™ 04 monitors the system states through the PWROK (Power OK), _LID (Lid closed) and _HSUS (Host suspended) lines. In addition to these signal inputs, the UR8HC007 family provides a set of registers, described in the "Registers" chapter of the *Juno™ A4 Technical Reference Manual*, that can be used by the host to control the PM-related performance of the controller through software. According to the status of these lines (or register settings), the Juno™ A4 will enable or disable specific tasks and reports suited to the current power and system management state of the Host.

Self-Power Management™ describes a method implemented by the Juno™ family of controllers that, independently of any system intervention, results in the lowest power consumption possible within the given parameters of its operation. Through Self-Power Management™, the Juno™ controllers are capable of typically operating at only 1 µA, independent of the state of the system. Self-Power Management™ primarily determines the actual power consumption of the controller IC.

The Juno™ A4 implements the patented Self-Power Management™ method to achieve the minimum power consumption possible, independent of the Host power management state.

Even when the Host is in the active state, the IC can still operate most of the time at only 1 µA, even with an external PS/2 device attached to it.



ZERO-POWER™ OPERATION OF PS/2 PORTS

The Juno™ A4 implements the patented "Message loss-less wake-up™" method to operate the direct PS/2 port. This method enables the controller to interface with the device attached to its PS/2 port while still operating in the "Stop" mode. Typical power consumption of the PS/2 port is therefore 1 µA.

If the PS/2 device reports a data packet, the controller will exit the "Stop" mode for as long as it takes to process the device message and relay the information, if necessary, to the Host system. This operation is done transparently to the Host, without any message loss or any response delays from the input devices.

This unique technology allows computers to operate at their minimum power consumption state even with the PS/2 device attached. Systems that employ an internal pointing device, such as a touch pad, touch screen or a force stick, can benefit the most from this feature, since the pointing device will force the controller to exit its "Stop" mode only when there is data to be reported.

PS/2 PORTS

The UR8HC007-0A4 provides one direct PS/2 port for the hot-plug connection of an external keyboard or mouse.

All of human input devices are active at all times. Data from both the external and internal keyboards and mice are merged and seamlessly presented to the system.

5-Volt Tolerant PS/2 Port

The UR8HC007-0A4 controller can be powered by a power supply between 3 and 5 Volts (+/- 10%). Even when the IC is powered by a 3-Volt supply, the PS/2 port can directly interface with 5-Volt powered devices — without the need of any external level-shifting circuitry. The Host can enable or disable the direct PS/2 port, in sync with the 5-Volt power plane that powers them. Alternatively, it can select the PS/2 port through the "HID enable/disable control" register.

HID MANAGER

The UR8HC007-0A4 Human Input Device (HID) Manager is responsible for the configuration and handling of HID devices that are embedded or attached to the controller. The HID Manager has the following responsibilities:
1. Enabling and disabling embedded and attached input devices through the "HID enable/disable control" register
2. Formatting and relaying input device reports to the Host
3. Controlling the configuration and operation of both embedded and attached input devices

The HID Manager consists of the four functional blocks: the PS/2 Port Manager; the Keyboard Manager; the Pointing Device Manager; and the Direct Port Manager.

The function of each Manager is explained in full in the Juno™ A4 Technical Reference Manual.

OTHER JUNO™ SERIES MEMBERS

Other members of the Juno™ series of companion ICs offers advanced, ergonomic control of an internal pointing device. Enabled pointing devices include touch pads or force sticks. If the application requires an internal pointing device, using a pointing-enabled Juno™ will eliminate the need for a dedicated mouse encoder IC.

KEYBOARD ENCODING

The UR8HC007-0A4 will encode an 8-row by 16-column keyboard matrix. OEMs may reprogram the matrix by sending commands to the IC from the system. The Juno™ A4 supports English, Japanese and European keyboards. In addition, the IC supports both sticky keys and notebook-style keyboards.

The keyboard below, the Fujitsu FKB7654, is the default keyboard for the UR8HC007-0A4.

Fujitsu FKB7654

GENERAL PURPOSE INPUT OUTPUT

The Juno™ A4 provides many GPIO pins which enable OEMs to easily differentiate their products.

Four GPIO ports provide interrupt at both falling and rising edge of signals. Two of these pins are dedicated for use as a Lid indicator and Digital power monitor. The other two may be used for a ring indicator, docking signal, soft power button, etc.

Three GPIO pins provide A/D input and are ideal for battery measurement.

Three GPIO pins provide two Pulse Width Modulation (PWM) channels and one D/A channel and may be used for analog control functions such as LCD brightness/contrast or audio volume control.

Four GPIO pins with high drive ability are set aside as LED drivers or I/O.

Eight GPIO pins can be used as system control outputs or inputs, for example, for switches.

JUNO™ A4 POINTING DEVICE MANAGER

The Juno™ A4 Pointing Device Manager has the following features:

Pin drive or device drive detection

The designer can select one of two configurations for touchscreen driving: with hardware driver (device drive) and without (pin drive). The Juno™ A4 can detect the configuration automatically at power-up and behave properly for that configuration. The touch and motion qualities are exactly the same for both configurations. For more details, see the analytical pin descriptions for touchscreen in the "Pin information" chapter.

Touch detection

The Pointing Device Manager periodically checks whether there is touch on touchscreen. If no touch is detected, the pointing device manager drives the touchscreen into power saving mode. If a touch is detected, touchscreen is forced into driving state and prepared for measurement.

Touch measurement

When the Pointing Device Manager detects a touch on touchscreen, it drives the touchscreen into drive state and does measurement. If the touch data is not good enough, the measured data are not used for the algorithm. Only good touch data are used for the algorithm.

Touch algorithm

Due to hand shaking and electrical noise, the raw data can not be output directly. The Pointing Device Manager uses a proprietary algorithm to process the data.

Sampling rate

The sampling rate is 100 coordinate points per second.

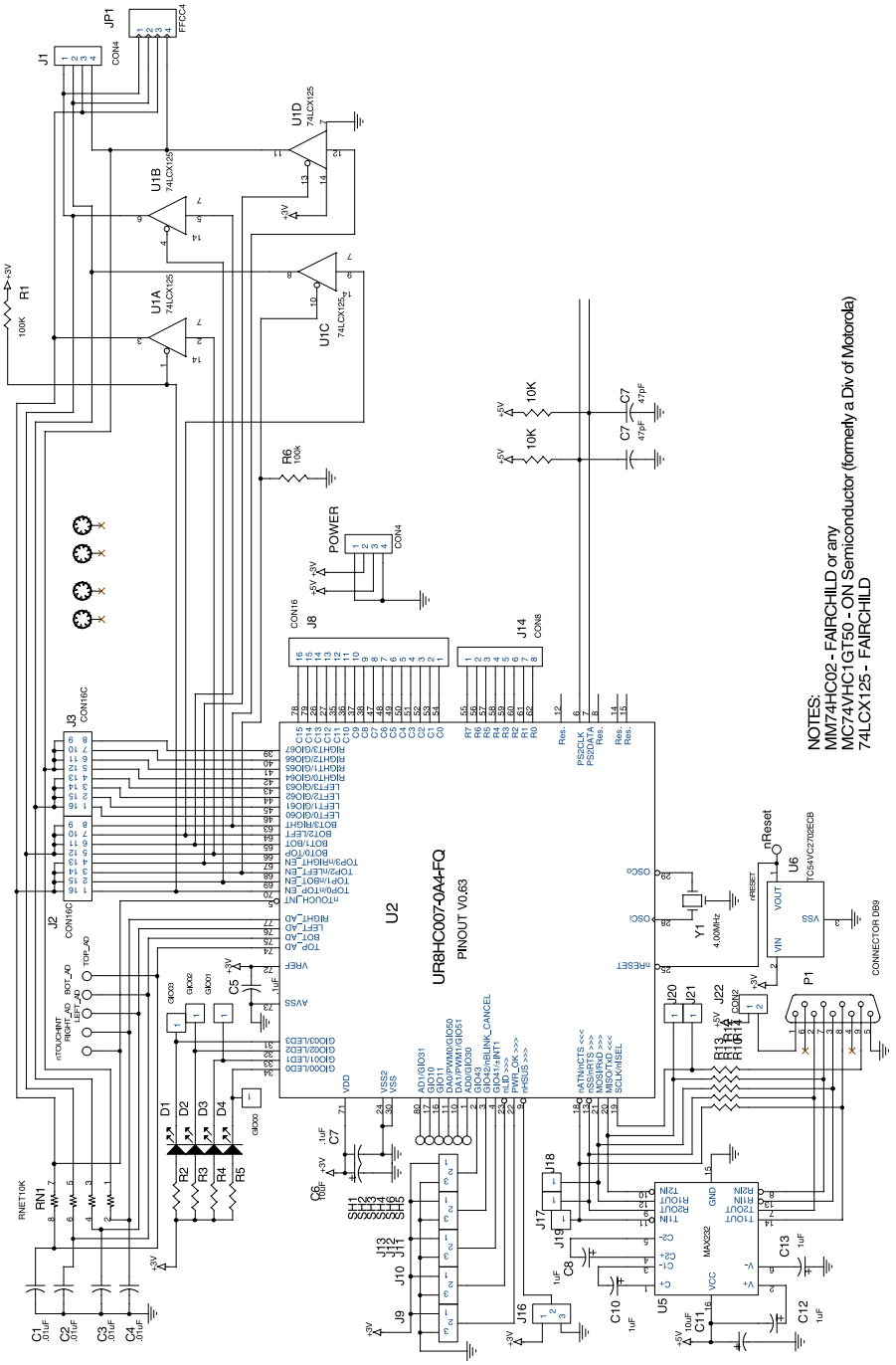
Resolution

The maximum touchscreen resolution is approximately 1000 points per direction. It varies with different touchscreens due to voltage drop on connection wires.

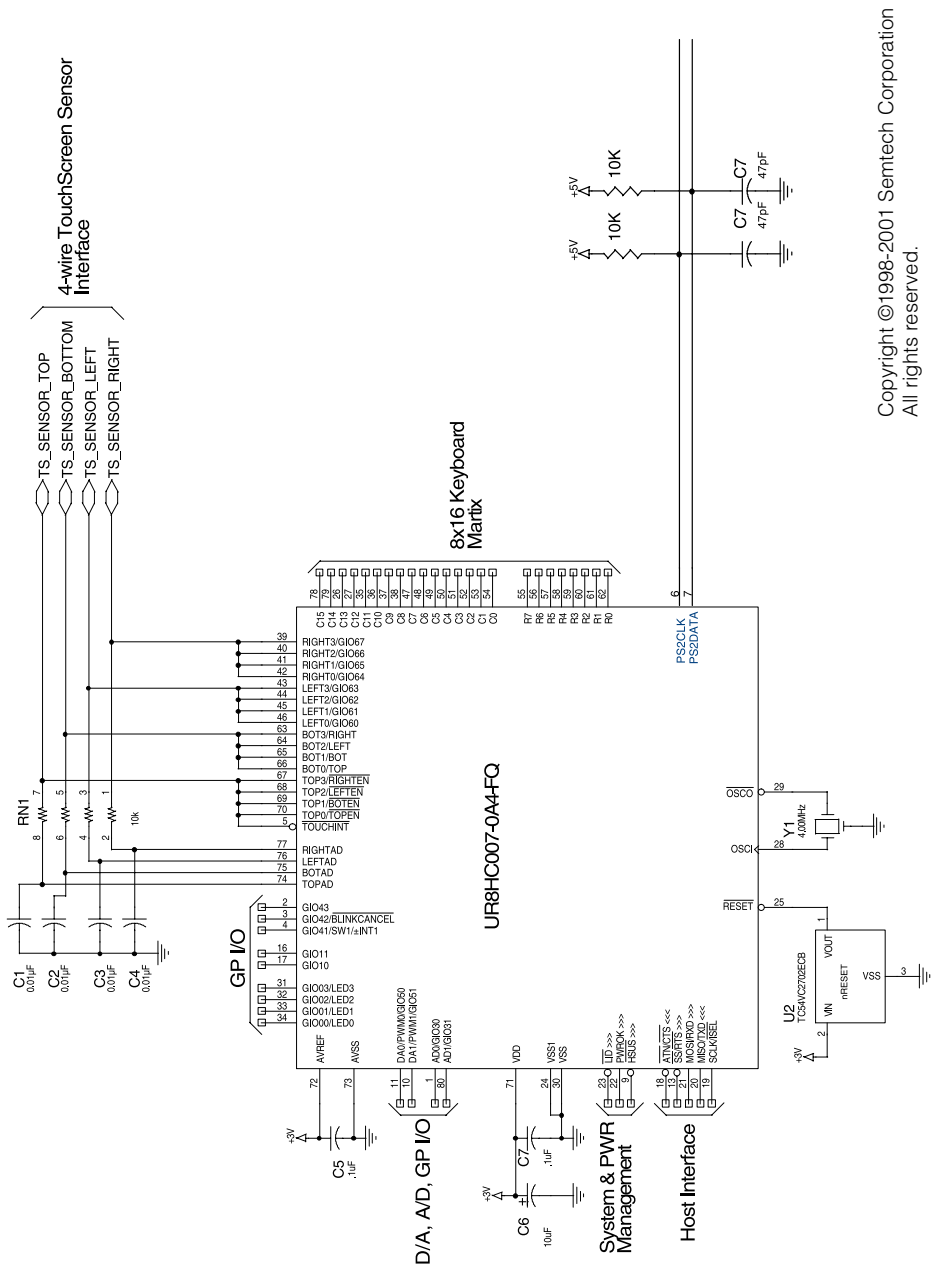
Touchscreens from different manufacturers

Touchscreens from different manufacturers have different parameters. The touchscreen parameters also depend on the size of touchscreen and material from which it is made. Because the Pointing Device Manager takes these properties into account, it can support almost any touchscreen.

SAMPLE SCHEMATIC FOR THE JUNO™ A4 WITH TOUCHSCREEN DRIVER



SAMPLE SCHEMATIC FOR THE JUNO™ A4 WITHOUT THE TOUCH SCREEN DRIVER



JUNO™ A4 ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

(VSS = 0V, Ambient Temperature T_A is in the range T_{LOW} to T_{HIGH})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input voltage			
All pins except 2-9	V_{IN}	-0.3 to VDD+0.3	V
Pins 2-9 (PS/2 ports PS2DATA, PS2CLK, GIO16/SW16, GIO17/SW17)	V_{IN}	-0.3 to +5.8	V
Output current			
Total peak for all pins	ΣI_{OH} (Peak)	-80	
	ΣI_{OL} (Peak)	80	mA
Total average for all pins	ΣI_{OH} (Avg)	-40	
	ΣI_{OL} (Avg)	40	mA
All pins except 31-34			
Peak for each pin	I_{OH} (Peak)	-10	
	I_{OL} (Peak)	10	mA
Average for each pin	I_{OH} (Avg)	-5	
	I_{OL} (Avg)	5	mA
Pins 31-34 (GIO00/LED0 - GIO03/LED3)			
Peak for each pin	I_{OH} (Peak)	-10	
	I_{OL} (Peak)	20	mA
Average for each pin	I_{OH} (Avg)	-5	
	I_{OL} (Avg)	15	mA
Temperature range			
Operating Temperature	T_{LOW} to T_{HIGH}	-20 to 85	ºC
Storage Temperature	T_{STG}	-40 to 125	ºC

POWER CONSUMPTION WHILE OPERATING THE PWM CHANNELS

Users should consider the built-in PWM channels for generating slowly changing DC control voltages. Since continuous clocking is necessary for the PWM operations, the only penalty for using the built-in PWM channels is the requirement for the chip to operate at least in the Reduced Power Mode, with typical Current Consumption of 750 µA.

NOTES FOR ELECTRICALS

Note 3:

Current Consumption values do not include any loading on the Output pins or Analog Reference Current for the built-in A/D or D/A modules.

Note 4:

Since the built-in A/D module consumes current only during short periods of time (when A/D conversion is actually requested), the Analog Reference Current for the built-in A/D module is not a significant contributor to the overall power consumption.

Note 5:

The Analog Reference Current for the built-in D/A module correlates linearly to the Output Voltage. For D/A output of 0V, the Analog Reference Current is null. For D/A outputs approaching Full Scale (AVREF), the maximum Analog Reference Current is indicated in this Table. This current is a significant contributor to the overall power consumption.

JUNO™ A4 ELECTRICAL CHARACTERISTICS, (CON'T)

Recommended Operating Conditions, Digital Section

(VSS = 0V, Ambient Temperature T_A is in the range T_{LOW} to T_{HIGH})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7	3.0	5.5	V
Input logic high voltage					
All pins except 2-9	V_{IH}	0.8V_{DD}		V_{DD}	V
Pins 2-9 (PS/2 ports PS2DATA, PS2CLK, GIO16/SW16, GIO17/SW17)	V_{IH}	0.8V_{DD}		5.5	V
Input logic low voltage					
All pins except 28	V_{IL}	0		0.2V_{DD}	V
Pin 28 (OSCI)	V_{IL}	0		0.16V_{DD}	V
Input current					
V_I = V_{SS}, V_{DD})	I_{IL} / I_{IL}	-5.0	0	5.0	µA
Input Pull-up Current (pins 56-58 / IP6-IP8, V_I = V_{SS})	I_{PUP}	-120		-10	µA
Output voltage					
I_{OH} = -1.0 mA	V_{OH}	V_{DD}-1.0			V
I_{OL} = 1.6 mA	V_{OL}			0.4	V
Current Consumption (see Note 3 below)					
Full Speed Mode (Fosc=4MHz)	I_{DD}		3.5	7.0	mA
Reduced Power Mode (Fosc=4MHz)	I_{DD}		750		µA
Stop Mode (Interrupts active, Fosc=0)	I_{DD}		.1	1.0 (T_A = 25ºC) 10(T_A = 85ºC)	µA

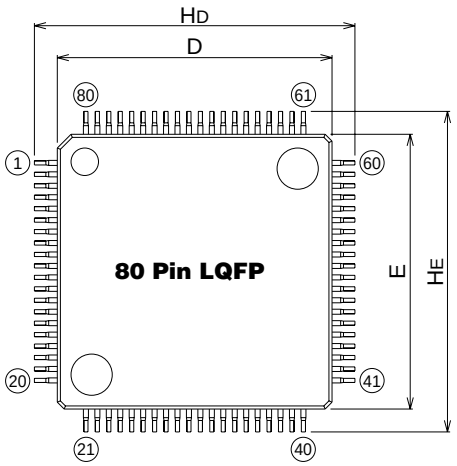
Recommended operating conditions, analog section

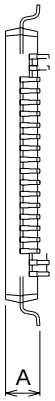
(VSS = 0V, Ambient Temperature T_A is in the range T_{LOW} to T_{HIGH})

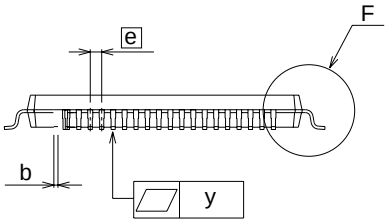
Parameter	Symbol	Min	Typ	Max	Unit
Analog Signal Ground	AVss		0		V
Analog Reference Voltage	AVREF	2.7	V_{DD}	V_{DD}	V
A/D Resolution -				10	Bits
A/D Absolute Accuracy				± 4	LSb
A/D Analog Input Voltage Range	V_{IA}	AVss		AVREF	V
A/D Analog Input Current	I_{IA}			5.0	µA
Analog Reference Current (see Note 4) (A/D is active)	I_{AVREF}			200	µA
D/A Resolution -				8	Bits
D/A Absolute Accuracy -				2.5	%
D/A Output Impedance	R_O	1	2.5	4.0	KOhms
Analog Reference Current (see Note 5) (D/A is active, Output = Full Scale)	I_{AVREF}			3.2	mA

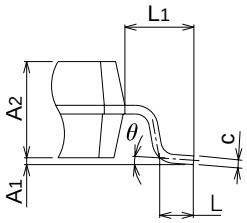
Note 3: please see left
Note 4: please see left
Note 5: please see left

MECHANICAL INFORMATION FOR THE UR8HC007-0A4 LQFP PACKAGE

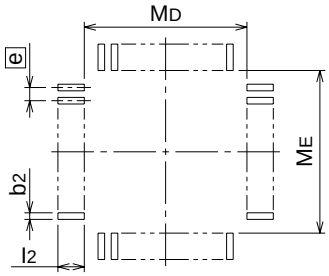








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	12.4	–
M_E	–	12.4	–

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