

# LH168A

## 384-output TFT-LCD Source Driver IC

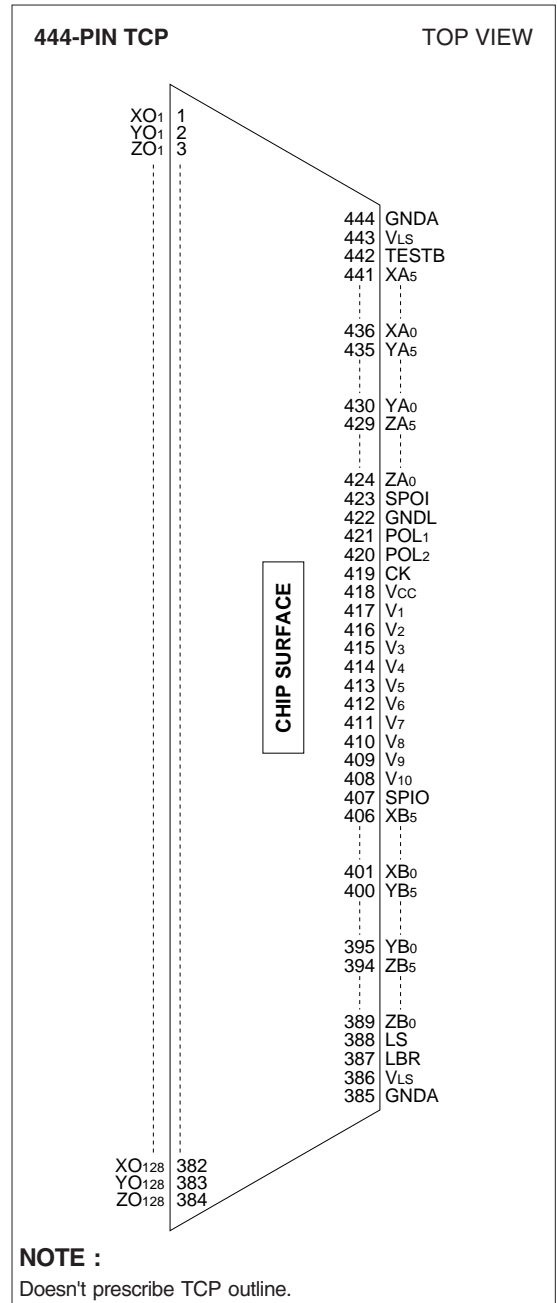
### DESCRIPTION

The LH168A is a 384-output TFT-LCD source driver IC which can simultaneously display 262 144 colors in 64 gray scales.

### FEATURES

- Number of LCD drive outputs : 384
- Built-in 6-bit digital input DAC
- 2-port input for each circuit of data inputs R, G and B, and it is possible to sample and hold display data of two pixels at the same time
- Possible to display 262 144 colors in 64 gray scales with reference voltage input of 10 gray scales : This reference voltage input corresponds to  $\gamma$  correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :  
Output shift direction can be selected  
XO<sub>1</sub>, YO<sub>1</sub>, ZO<sub>1</sub>→XO<sub>128</sub>, YO<sub>128</sub>, ZO<sub>128</sub> or  
ZO<sub>128</sub>, YO<sub>128</sub>, XO<sub>128</sub>→ZO<sub>1</sub>, YO<sub>1</sub>, XO<sub>1</sub>
- Shift clock frequency : 55 MHz (MAX.)
- Supply voltages
  - V<sub>CC</sub> (for logic system) : +2.7 to +3.6 V
  - V<sub>LS</sub> (for LCD drive system) : +3.0 to +5.5 V
- Package : 444-pin TCP (Tape Carrier Package)

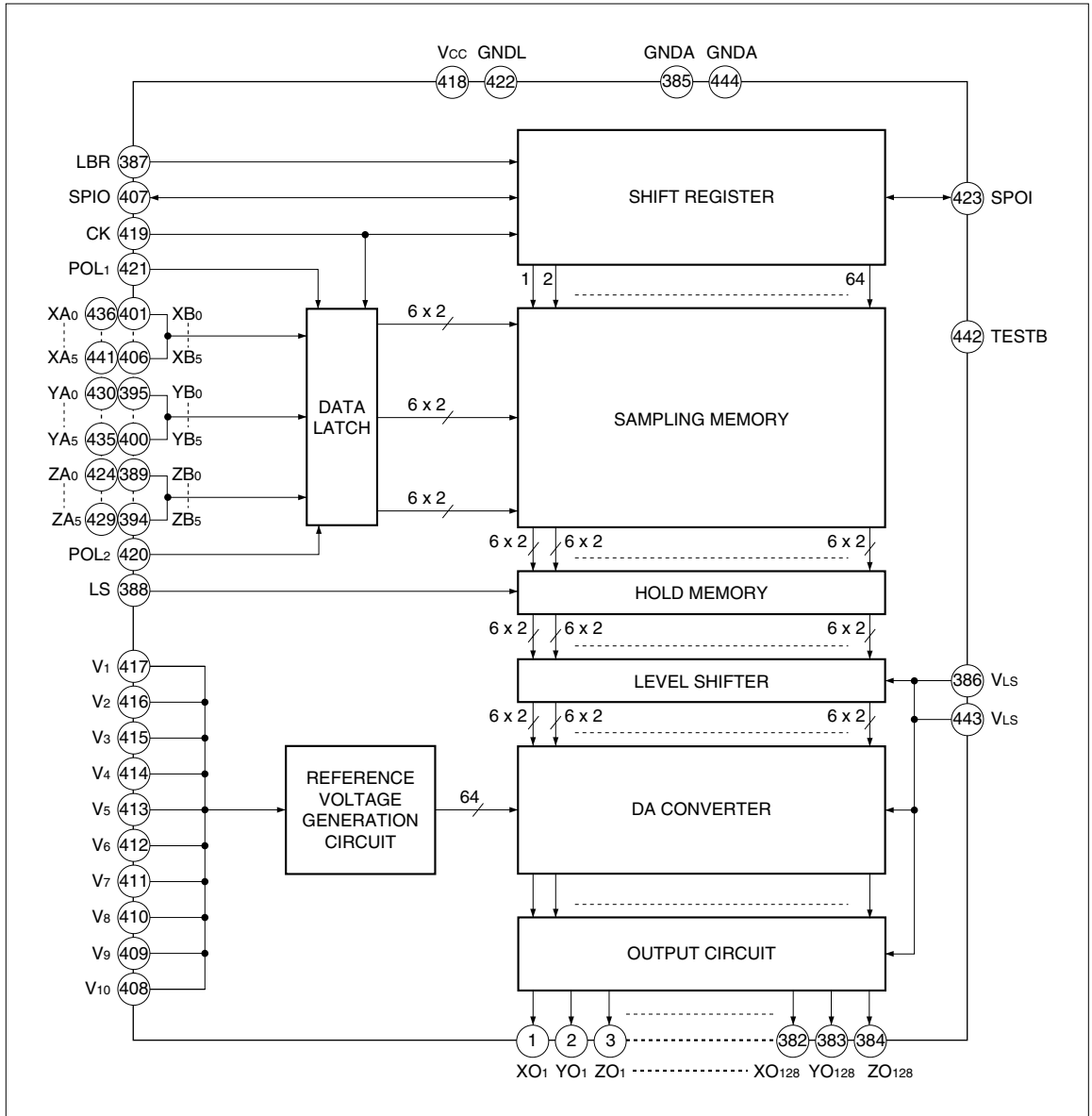
### PIN CONNECTIONS



**PIN DESCRIPTION**

<b>PIN NO.</b>	<b>SYMBOL</b>	<b>I/O</b>	<b>DESCRIPTION</b>
1 to 384	XO1-ZO128	O	LCD drive output pins
385, 444	GND A	–	Ground pins for analog circuit
386, 443	VLS	–	Power supply pins for analog circuit
387	LBR	I	Shift direction selection input pin
388	LS	I	Latch input pin
389 to 394	ZB0-ZB5	I	Data input pins
395 to 400	YB0-YB5	I	Data input pins
401 to 406	XB0-XB5	I	Data input pins
407	SPIO	I/O	Start pulse input/cascade output pin
408 to 417	V10-V1	I	Reference voltage input pins
418	VCC	–	Power supply pin for digital circuit
419	CK	I	Shift clock input pin
420, 421	POL2, POL1	I	Input data polarity exchange input pins
422	GNDL	–	Ground pin for digital circuit
423	SPOI	I/O	Start pulse input/cascade output pin
424 to 429	ZA0-ZA5	I	Data input pins
430 to 435	YA0-YA5	I	Data input pins
436 to 441	XA0-XA5	I	Data input pins
442	TESTB	I	IC test pin

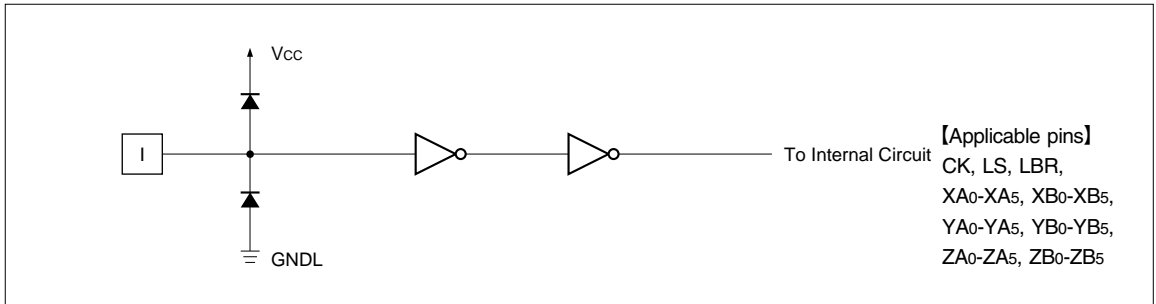
BLOCK DIAGRAM



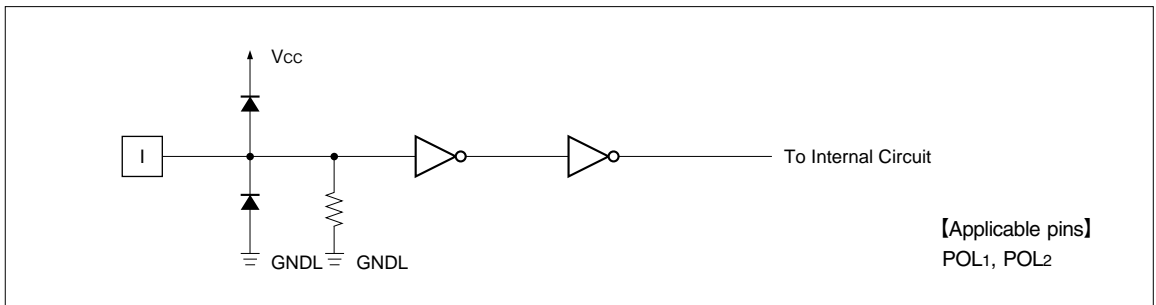
**FUNCTIONAL OPERATIONS OF EACH BLOCK**

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold Memory	Used for temporary latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 64-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 64 gray scales to LCD drive output pin.

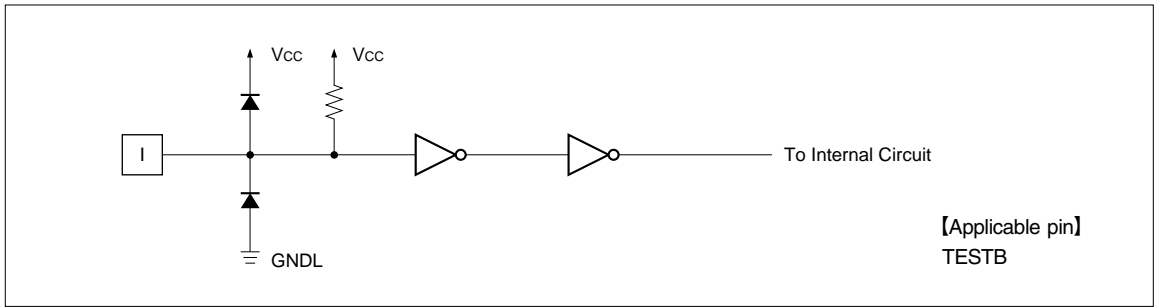
**INPUT/OUTPUT CIRCUITS**



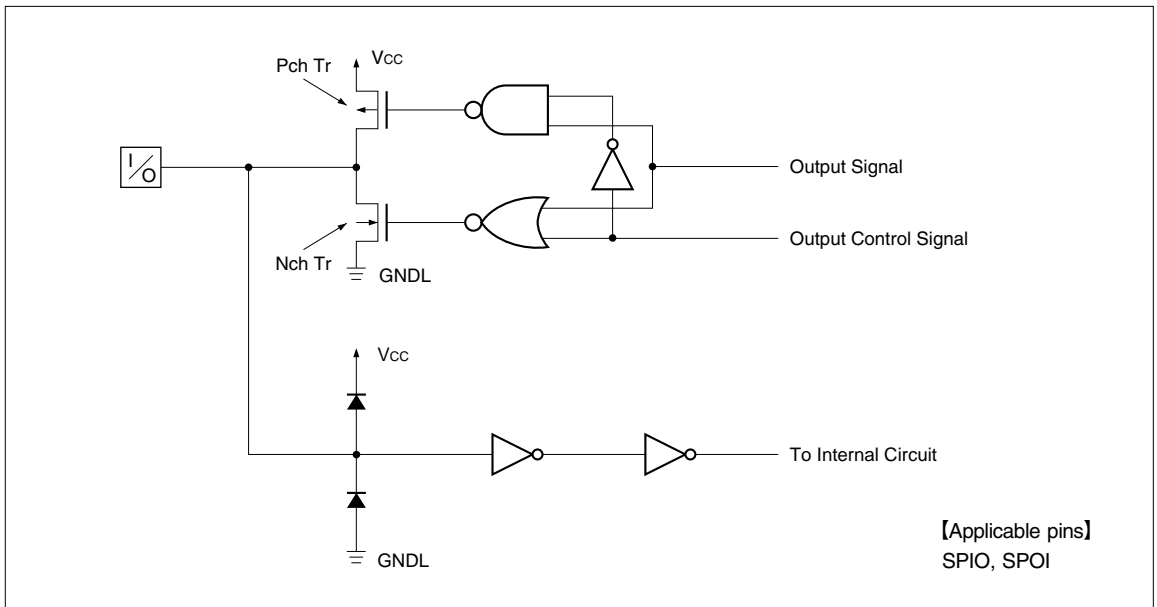
**Fig. 1 Input Circuit (1)**



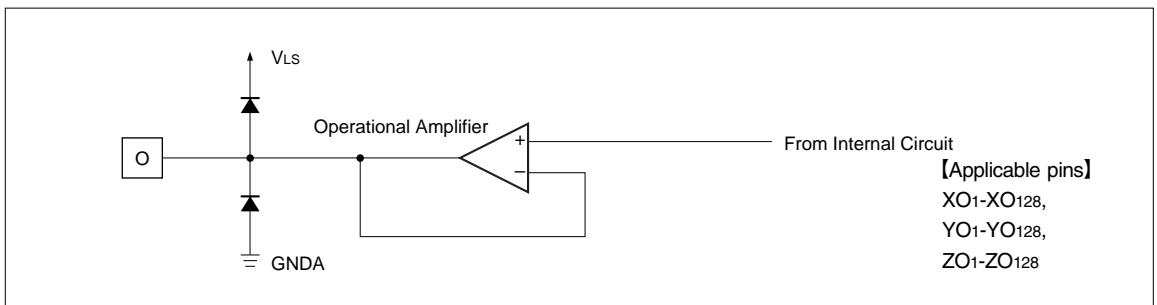
**Fig. 2 Input Circuit (2)**



**Fig. 3 Input Circuit (3)**



**Fig. 4 Input/Output Circuit**



**Fig. 5 Output Circuit**

## FUNCTIONAL DESCRIPTION

### Pin Functions

SYMBOL	FUNCTIONS
VCC	Used as power supply pin for digital circuit, connected to +2.7 to +3.6 V.
VLS	Used as power supply pin for analog circuit, connected to +3.0 to +5.5 V.
GNDL	Used as ground pin for logic circuit, connected to 0 V.
GNDA	Used as ground pin for LCD drive circuit, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting, refer to " <b>Functional Operations</b> ".
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to " <b>Functional Operations</b> ".
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
V1-V10	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to " <b>Output Voltage Value</b> ". For internal gamma correction, refer to " <b>Gamma Correction Value</b> ".
XA0-XA5, YA0-YA5 ZA0-ZA5, XB0-XB5 YB0-YB5, ZB0-ZB5	Used as data input pins of R, G, and B colors. 6-bit x 2-pixel data are input from data pins at the rising edge of CK. For relation between input data and output voltage values, refer to " <b>Functional Operations</b> " and " <b>Output Voltage Value</b> ". Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
XO1-XO128, YO1-YO128, ZO1-ZO128	Used as LCD drive output pins which output the voltage corresponding to the input of data input pins (XA0 to XA5, XB0 to XB5, YA0 to YA5, YB0 to YB5, ZA0 to ZA5, ZB0 to ZB5). Data of XO1 to XO128 correspond to XA0 to XA5 and XB0 to XB5. Data of YO1 to YO128 correspond to YA0 to YA5 and YB0 to YB5, and data of ZO1 to ZO128 correspond to ZA0 to ZA5 and ZB0 to ZB5. For relation between input data and output voltage values, refer to " <b>Functional Operations</b> " and " <b>Output Voltage Value</b> ".
POL1 POL2	Used as input pins for input data polarity exchange. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode (POL1 = A system, POL2 = B system). For relation between input data and output voltage values, refer to " <b>Output Voltage Value</b> ". Must be connected to 0 V or opened.
TESTB	Used as pin for IC testing. Must be connected to VCC or opened.

## Functional Operations

The following describes the relation between data input pin and output direction.

Data input pin	XA0-XA5	YA0-YA5	ZA0-ZA5	XB0-XB5	YB0-YB5	ZB0-ZB5	.....	XB0-XB5	YB0-YB5	ZB0-ZB5
Output direction	XO1	YO1	ZO1	XO2	YO2	ZO2	.....	XO128	YO128	ZO128

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO1, YO1, ZO1→XO128, YO128, ZO128)	LEFT SHIFT (ZO128, YO128, XO128→ZO1, YO1, XO1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

### NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

## Output Voltage Value

Two voltages are selected from all of the reference voltages (V<sub>1</sub>-V<sub>10</sub>) by the upper 3-bit data (D<sub>5</sub>, D<sub>4</sub> and D<sub>3</sub>) of the 6-bit input data (D<sub>5</sub>, D<sub>4</sub>, D<sub>3</sub>, D<sub>2</sub>, D<sub>1</sub> and D<sub>0</sub>) taken by time sharing, and intermediate

value is determined by the lower 3-bit data (D<sub>2</sub>, D<sub>1</sub> and D<sub>0</sub>).

Relation between input data and output voltage values is shown below.

INPUT DATA	OUTPUT VOLTAGE		INPUT DATA	OUTPUT VOLTAGE	
	POL <sub>1</sub> , POL <sub>2</sub> = "L"	POL <sub>1</sub> , POL <sub>2</sub> = "H"		POL <sub>1</sub> , POL <sub>2</sub> = "L"	POL <sub>1</sub> , POL <sub>2</sub> = "H"
0	V <sub>1</sub>	V <sub>10</sub>	20	$V_6 + (V_5 - V_6) \times 7/8$	V <sub>5</sub>
1	$V_2 + (V_1 - V_2) \times 6/7$	V <sub>9</sub>	21	$V_6 + (V_5 - V_6) \times 6/8$	$V_5 + (V_4 - V_5) \times 1/8$
2	$V_2 + (V_1 - V_2) \times 5/7$	$V_9 + (V_8 - V_9) \times 1/7$	22	$V_6 + (V_5 - V_6) \times 5/8$	$V_5 + (V_4 - V_5) \times 2/8$
3	$V_2 + (V_1 - V_2) \times 4/7$	$V_9 + (V_8 - V_9) \times 2/7$	23	$V_6 + (V_5 - V_6) \times 4/8$	$V_5 + (V_4 - V_5) \times 3/8$
4	$V_2 + (V_1 - V_2) \times 3/7$	$V_9 + (V_8 - V_9) \times 3/7$	24	$V_6 + (V_5 - V_6) \times 3/8$	$V_5 + (V_4 - V_5) \times 4/8$
5	$V_2 + (V_1 - V_2) \times 2/7$	$V_9 + (V_8 - V_9) \times 4/7$	25	$V_6 + (V_5 - V_6) \times 2/8$	$V_5 + (V_4 - V_5) \times 5/8$
6	$V_2 + (V_1 - V_2) \times 1/7$	$V_9 + (V_8 - V_9) \times 5/7$	26	$V_6 + (V_5 - V_6) \times 1/8$	$V_5 + (V_4 - V_5) \times 6/8$
7	V <sub>2</sub>	$V_9 + (V_8 - V_9) \times 6/7$	27	V <sub>6</sub>	$V_5 + (V_4 - V_5) \times 7/8$
8	$V_3 + (V_2 - V_3) \times 7/8$	V <sub>8</sub>	28	$V_7 + (V_6 - V_7) \times 7/8$	V <sub>4</sub>
9	$V_3 + (V_2 - V_3) \times 6/8$	$V_8 + (V_7 - V_8) \times 1/8$	29	$V_7 + (V_6 - V_7) \times 6/8$	$V_4 + (V_3 - V_4) \times 1/8$
A	$V_3 + (V_2 - V_3) \times 5/8$	$V_8 + (V_7 - V_8) \times 2/8$	2A	$V_7 + (V_6 - V_7) \times 5/8$	$V_4 + (V_3 - V_4) \times 2/8$
B	$V_3 + (V_2 - V_3) \times 4/8$	$V_8 + (V_7 - V_8) \times 3/8$	2B	$V_7 + (V_6 - V_7) \times 4/8$	$V_4 + (V_3 - V_4) \times 3/8$
C	$V_3 + (V_2 - V_3) \times 3/8$	$V_8 + (V_7 - V_8) \times 4/8$	2C	$V_7 + (V_6 - V_7) \times 3/8$	$V_4 + (V_3 - V_4) \times 4/8$
D	$V_3 + (V_2 - V_3) \times 2/8$	$V_8 + (V_7 - V_8) \times 5/8$	2D	$V_7 + (V_6 - V_7) \times 2/8$	$V_4 + (V_3 - V_4) \times 5/8$
E	$V_3 + (V_2 - V_3) \times 1/8$	$V_8 + (V_7 - V_8) \times 6/8$	2E	$V_7 + (V_6 - V_7) \times 1/8$	$V_4 + (V_3 - V_4) \times 6/8$
F	V <sub>3</sub>	$V_8 + (V_7 - V_8) \times 7/8$	2F	V <sub>7</sub>	$V_4 + (V_3 - V_4) \times 7/8$
10	$V_4 + (V_3 - V_4) \times 7/8$	V <sub>7</sub>	30	$V_8 + (V_7 - V_8) \times 7/8$	V <sub>3</sub>
11	$V_4 + (V_3 - V_4) \times 6/8$	$V_7 + (V_6 - V_7) \times 1/8$	31	$V_8 + (V_7 - V_8) \times 6/8$	$V_3 + (V_2 - V_3) \times 1/8$
12	$V_4 + (V_3 - V_4) \times 5/8$	$V_7 + (V_6 - V_7) \times 2/8$	32	$V_8 + (V_7 - V_8) \times 5/8$	$V_3 + (V_2 - V_3) \times 2/8$
13	$V_4 + (V_3 - V_4) \times 4/8$	$V_7 + (V_6 - V_7) \times 3/8$	33	$V_8 + (V_7 - V_8) \times 4/8$	$V_3 + (V_2 - V_3) \times 3/8$
14	$V_4 + (V_3 - V_4) \times 3/8$	$V_7 + (V_6 - V_7) \times 4/8$	34	$V_8 + (V_7 - V_8) \times 3/8$	$V_3 + (V_2 - V_3) \times 4/8$
15	$V_4 + (V_3 - V_4) \times 2/8$	$V_7 + (V_6 - V_7) \times 5/8$	35	$V_8 + (V_7 - V_8) \times 2/8$	$V_3 + (V_2 - V_3) \times 5/8$
16	$V_4 + (V_3 - V_4) \times 1/8$	$V_7 + (V_6 - V_7) \times 6/8$	36	$V_8 + (V_7 - V_8) \times 1/8$	$V_3 + (V_2 - V_3) \times 6/8$
17	V <sub>4</sub>	$V_7 + (V_6 - V_7) \times 7/8$	37	V <sub>8</sub>	$V_3 + (V_2 - V_3) \times 7/8$
18	$V_5 + (V_4 - V_5) \times 7/8$	V <sub>6</sub>	38	$V_9 + (V_8 - V_9) \times 6/7$	V <sub>2</sub>
19	$V_5 + (V_4 - V_5) \times 6/8$	$V_6 + (V_5 - V_6) \times 1/8$	39	$V_9 + (V_8 - V_9) \times 5/7$	$V_2 + (V_1 - V_2) \times 1/7$
1A	$V_5 + (V_4 - V_5) \times 5/8$	$V_6 + (V_5 - V_6) \times 2/8$	3A	$V_9 + (V_8 - V_9) \times 4/7$	$V_2 + (V_1 - V_2) \times 2/7$
1B	$V_5 + (V_4 - V_5) \times 4/8$	$V_6 + (V_5 - V_6) \times 3/8$	3B	$V_9 + (V_8 - V_9) \times 3/7$	$V_2 + (V_1 - V_2) \times 3/7$
1C	$V_5 + (V_4 - V_5) \times 3/8$	$V_6 + (V_5 - V_6) \times 4/8$	3C	$V_9 + (V_8 - V_9) \times 2/7$	$V_2 + (V_1 - V_2) \times 4/7$
1D	$V_5 + (V_4 - V_5) \times 2/8$	$V_6 + (V_5 - V_6) \times 5/8$	3D	$V_9 + (V_8 - V_9) \times 1/7$	$V_2 + (V_1 - V_2) \times 5/7$
1E	$V_5 + (V_4 - V_5) \times 1/8$	$V_6 + (V_5 - V_6) \times 6/8$	3E	V <sub>9</sub>	$V_2 + (V_1 - V_2) \times 6/7$
1F	V <sub>5</sub>	$V_6 + (V_5 - V_6) \times 7/8$	3F	V <sub>10</sub>	V <sub>1</sub>

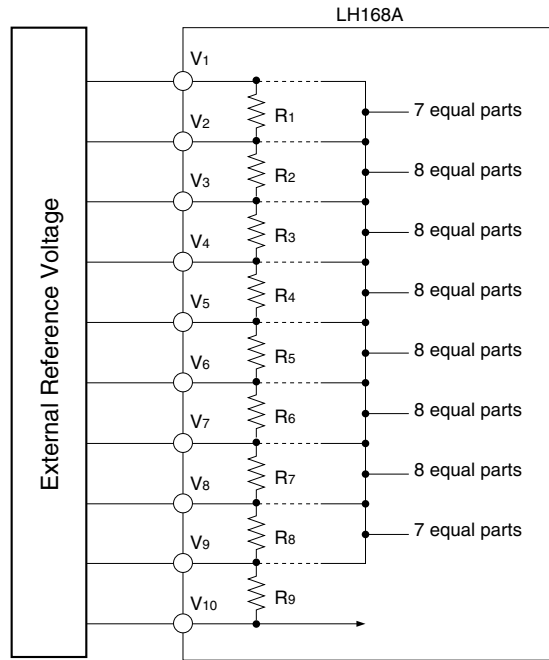


### $\gamma$ (gamma) Correction Value

Between reference voltage input pins, 7 or 8 resistors of the same resistance value are connected in series.

When the resistance ratio between respective

reference voltage input pins matches the reference voltages ( $V_2$  to  $V_9$ ) for  $\gamma$  correction of LCD panel, the external power supply of the intermediate voltages (for  $V_2$  to  $V_9$  pins) is not required.



The following shows the ratio of  $\gamma$  correction resistance.

R9	7.85
R8	1.98
R7	1.32
R6	0.99
R5	0.91
R4	1.24
R3	1.08
R2	2.15
R1	2.48

## PRECAUTIONS

### Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

$V_{CC} \rightarrow$  logic input  $\rightarrow V_{LS}, V_1-V_{10}$

When disconnecting the power supply, follow the reverse sequence.

### Reference voltage input

The relation of the reference voltage input is shown here.

$G_{NDA} < V_1 \leq V_2 \leq \dots \leq V_9 \leq V_{10} < V_{LS}$  or  
 $V_{LS} > V_1 \geq V_2 \geq \dots \geq V_9 \geq V_{10} > G_{NDA}$

### Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

### Target output load

This IC is designed for a 70 pF output load capacity. When using this IC for other than 70 pF panels, confirm the device is having no problem before using it.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	$V_{CC}$	$V_{CC}$	-0.3 to +7.0	V	1, 2
	$V_{LS}$	$V_{LS}$	-0.3 to +7.0	V	
Input voltage	$V_I$	$V_1-V_{10}$	-0.3 to $V_{LS} + 0.3$	V	
	$V_I$	SPIO, SPOI, CK, LS, LBR, POL1, POL2, TESTB, XA0-XA5, XB0-XB5, YA0-YA5, YB0-YB5, ZA0-ZA5, ZB0-ZB5	-0.3 to $V_{CC} + 0.3$	V	
Output voltage	$V_O$	SPIO, SPOI	-0.3 to $V_{CC} + 0.3$	V	
	$V_O$	XO1-ZO128	-0.3 to $V_{LS} + 0.3$	V	
Storage temperature	$T_{STG}$		-45 to +125	°C	

### NOTES :

- $T_A = +25\text{ }^\circ\text{C}$
- The maximum applicable voltage on any pin with respect to GNDL and GNDA (0 V).

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	$V_{CC}$	+2.7		+3.6	V	1
	$V_{LS}$	+3.0		+5.5	V	
Reference voltage input	$V_1-V_{10}$	0		$V_{LS}$	V	
Clock frequency	f <sub>CK</sub>			55	MHz	
LCD drive output load capacity	C <sub>L</sub>			70	pF	
Operating temperature	$T_{OPR}$	-20		+75	°C	

### NOTE :

- The applicable voltage on any pin with respect to GNDL and GNDA (0 V).

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(V<sub>CC</sub> = +2.7 to +3.6 V, V<sub>LS</sub> = +3.0 to +5.5 V, T<sub>OPR</sub> = -20 to +75 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V <sub>IL</sub>		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5,	GNDL		0.3V <sub>CC</sub>	V	
Input "High" voltage	V <sub>IH</sub>		SPIO, SPOI, CK, LS, LBR	0.7V <sub>CC</sub>		V <sub>CC</sub>	V	
Output "Low" voltage	V <sub>OL</sub>	I <sub>OL</sub> = 0.3 mA	SPIO, SPOI	GNDL		GNDL + 0.4	V	
Output "High" voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.3 mA		V <sub>CC</sub> - 0.4		V <sub>CC</sub>	V	
Input "Low" current	I <sub>ILL</sub>		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, SPIO, SPOI, CK, LS, LBR, POL1, POL2			1	μA	
Input "High" current	I <sub>IH1</sub>		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, SPIO, SPOI, CK, LS, LBR			1	μA	
	I <sub>IH2</sub>		POL1, POL2			400	μA	
Supply current (In operation mode)	I <sub>CC1</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz (Data sampling state)	V <sub>CC</sub> -GNDL			12	mA	
Supply current (In standby mode)	I <sub>CC2</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz SPI = GND is fixed. (Standby state)	V <sub>CC</sub> -GNDL			4	mA	
Supply current (In operation mode)	I <sub>LS1</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz (Data sampling state)	V <sub>LS</sub> -GNDA			10	mA	
Supply current (In standby mode)	I <sub>LS2</sub>	f <sub>CK</sub> = 55 MHz f <sub>LS</sub> = 50 kHz SPI = GND is fixed. (Standby state)	V <sub>LS</sub> -GNDA			9	mA	
Output voltage range	V <sub>OUT</sub>		XO1-ZO128	GNDL + 0.1		V <sub>LS</sub> - 0.1	V	1
Deviations between output voltage pins	V <sub>OD</sub>			-20		20	mV	
Output current	I <sub>O1</sub> , I <sub>O2</sub>			20	50		μA	
Resistance between reference voltage input pins	R <sub>GMA</sub>		V1-V10	10		30	kΩ	

## NOTES :

1. Criterion of evaluating voltage deviations.

(a) Between output voltage pins

Measuring values : Output voltage value at the time after  
10 μs at the rising edge of LS.

(Average of several times)

(Conditions) Output load capacity is 70 pF.

In a state when the reference voltage is fixed.

Expecting values : Calculated following these specifications.

(Conditions) In a state when the reference voltage is fixed.

(b) Between LCD drivers

Measuring values : Applicable to (a).

(Conditions) Applicable to (a).

Expecting values : Applicable to (a).

(Conditions) Applicable to (a).

Each input voltage between the LCD drivers must be  
made perfectly equal by connecting corresponding  
reference voltage input pins.

2. I
- <sub>O1</sub>
- : Applied voltage = 3.0 V for output pins XO
- <sub>1</sub>
- to ZO
- <sub>128</sub>
- .

Output voltage = 2.5 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.V<sub>LS</sub> = 5.0 V

- I
- <sub>O2</sub>
- : Applied voltage = 2.0 V for output pins XO
- <sub>1</sub>
- to ZO
- <sub>128</sub>
- .

Output voltage = 2.5 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.V<sub>LS</sub> = 5.0 V

**AC Characteristics** ( $V_{CC} = +2.7$  to  $+3.6$  V,  $V_{LS} = +3.0$  to  $+5.5$  V,  $T_{OPR} = -20$  to  $+75$  °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f <sub>CK</sub>		CK			55	MHz
"H" level pulse width	t <sub>CWH</sub>			4			ns
"L" level pulse width	t <sub>CWL</sub>			4			ns
Input rise time	t <sub>CR</sub>					4	ns
Input fall time	t <sub>CF</sub>					4	ns
Data setup time	t <sub>SUD</sub>		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, POL1, POL2	4			ns
Data hold time	t <sub>HD</sub>			0			ns
Start pulse setup time	t <sub>SUSP</sub>		SPIO, SPOI	4			ns
Start pulse hold time	t <sub>HSP</sub>			0			ns
Start pulse width	t <sub>WSP</sub>					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t <sub>DSP</sub>	C <sub>L</sub> = 10 pF				12	ns
LCD drive output delay time 1	t <sub>DO1</sub>	C <sub>L</sub> = 70 pF	XO1-ZO <sub>128</sub>			3	μs
LCD drive output delay time 2	t <sub>DO2</sub>	C <sub>L</sub> = 70 pF				10	μs
LS signal-SPI signal set up time	t <sub>LSSP</sub>		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t <sub>HLS</sub>			9			ns
LS signal "H" level width	t <sub>WLS</sub>			$\frac{1}{f_{CK}}$			ns

Timing Chart

