

# LH168R

## 384-output TFT-LCD Source Driver IC

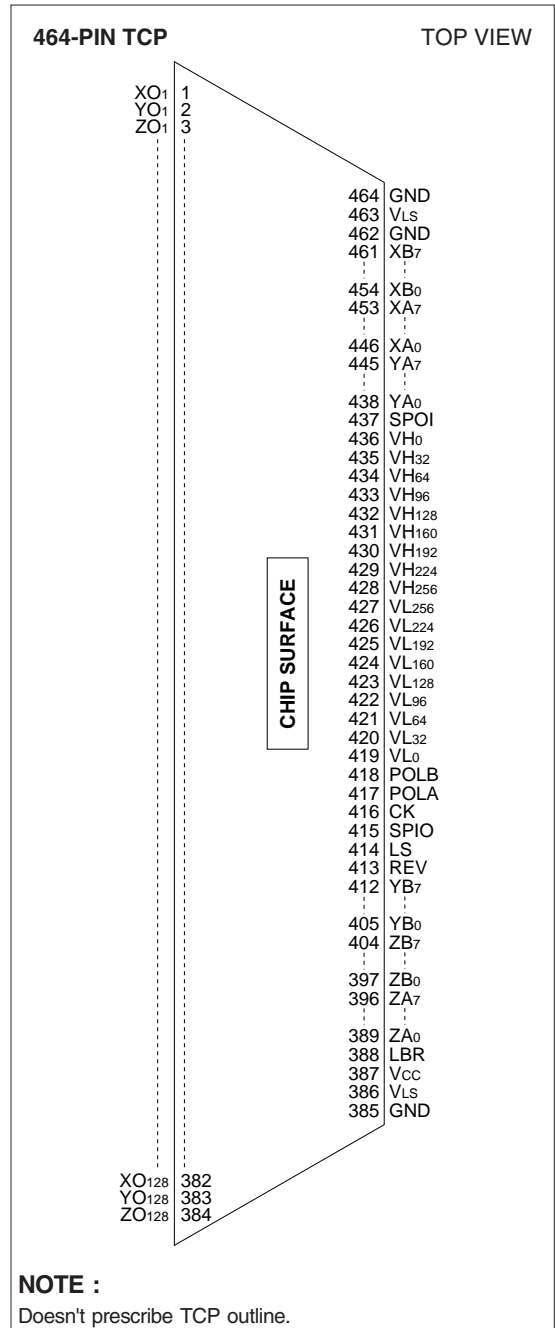
### DESCRIPTION

The LH168R is a 384-output TFT-LCD source driver IC which can simultaneously display 16.7 million colors in 256 gray scales.

### FEATURES

- Number of LCD drive outputs : 384
- Built-in 8-bit digital input DAC
- Dot-inversion drive : Outputs the inverted gray scale voltages between LCD drive pins next to each other
- 2-port input for each circuit of data inputs R, G and B, and it is possible to sample and hold display data of two pixels at the same time
- Possible to display 16.7 million colors in 256 gray scales with reference voltage input of 18 gray scales : This reference voltage input corresponds to  $\gamma$  correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :  
Output shift direction can be selected  
XO<sub>1</sub>, YO<sub>1</sub>, ZO<sub>1</sub>→XO<sub>128</sub>, YO<sub>128</sub>, ZO<sub>128</sub> or  
ZO<sub>128</sub>, YO<sub>128</sub>, XO<sub>128</sub>→ZO<sub>1</sub>, YO<sub>1</sub>, XO<sub>1</sub>
- Shift clock frequency : 65 MHz (MAX.)
- Supply voltages
  - V<sub>CC</sub> (for logic system) : +2.5 to +3.6 V
  - V<sub>LS</sub> (for LCD drive) : +13 V (MAX.)
- Package : 464-pin TCP (Tape Carrier Package)

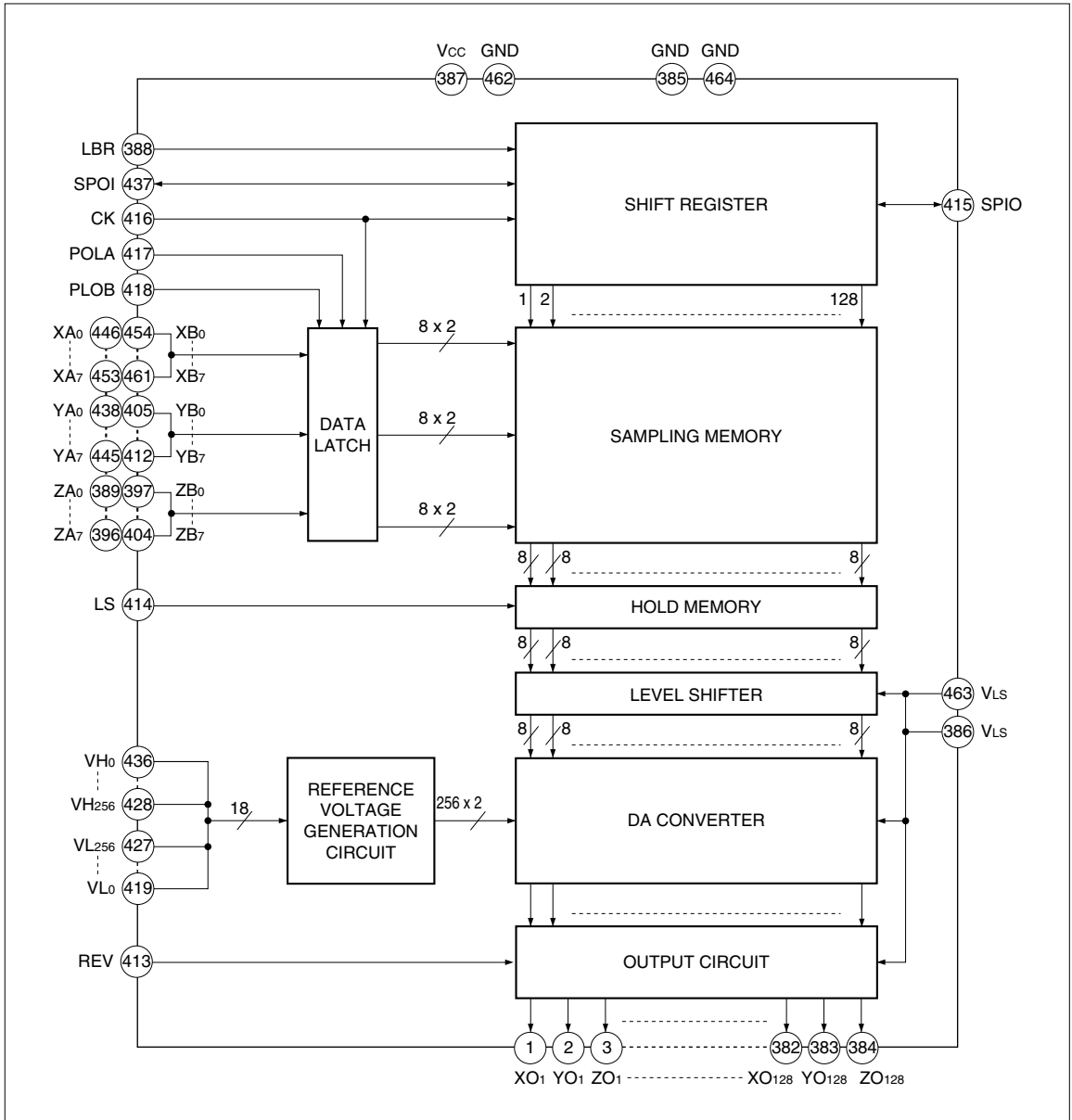
### PIN CONNECTIONS



**PIN DESCRIPTION**

<b>PIN NO.</b>	<b>SYMBOL</b>	<b>I/O</b>	<b>DESCRIPTION</b>
1 to 384	XO1-ZO128	O	LCD drive output pins
385, 462, 464	GND	–	Ground pins
386	VLS	–	Power supply pin for analog circuit
387	VCC	–	Power supply pin for digital circuit
388	LBR	I	Shift direction selection input pin
389 to 396	ZA0-ZA7	I	Data input pins
397 to 404	ZB0-ZB7	I	Data input pins
405 to 412	YB0-YB7	I	Data input pins
413	REV	I	LCD drive output polarity exchange input pin
414	LS	I	Latch input pin
415	SPIO	I/O	Start pulse input/cascade output pin
416	CK	I	Shift clock input pin
417, 418	POLA, POLB	I	Input data polarity exchange input pins
419 to 427	VL0-VL256	I	Reference voltage input pins
428 to 436	VH256-VH0	I	Reference voltage input pins
437	SPOI	I/O	Start pulse input/cascade output pin
438 to 445	YA0-YA7	I	Data input pins
446 to 453	XA0-XA7	I	Data input pins
454 to 461	XB0-XB7	I	Data input pins
463	VLS	–	Power supply pin for analog circuit

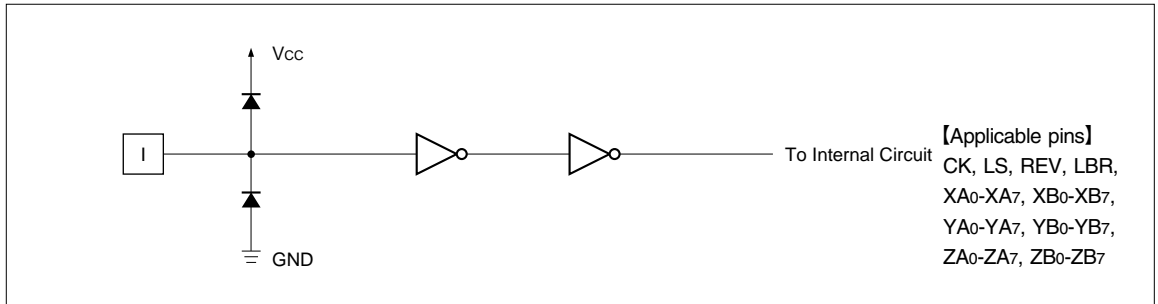
BLOCK DIAGRAM



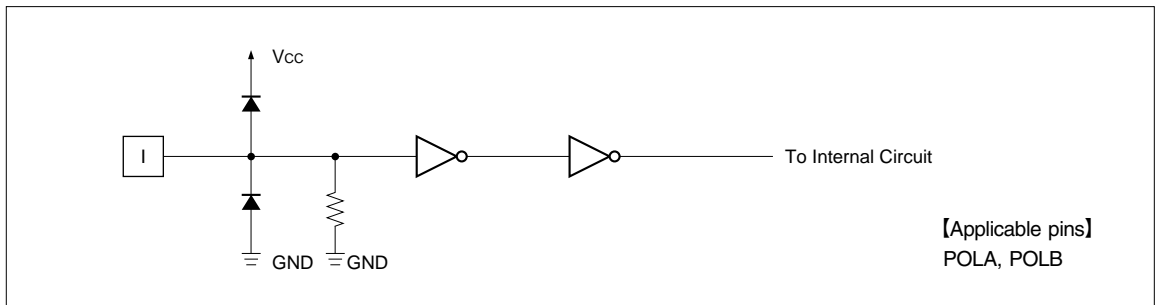
**FUNCTIONAL OPERATIONS OF EACH BLOCK**

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 256 x 2-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 256 x 2 gray scales to LCD drive output pin.

**INPUT/OUTPUT CIRCUITS**



**Fig. 1 Input Circuit (1)**



**Fig. 2 Input Circuit (2)**

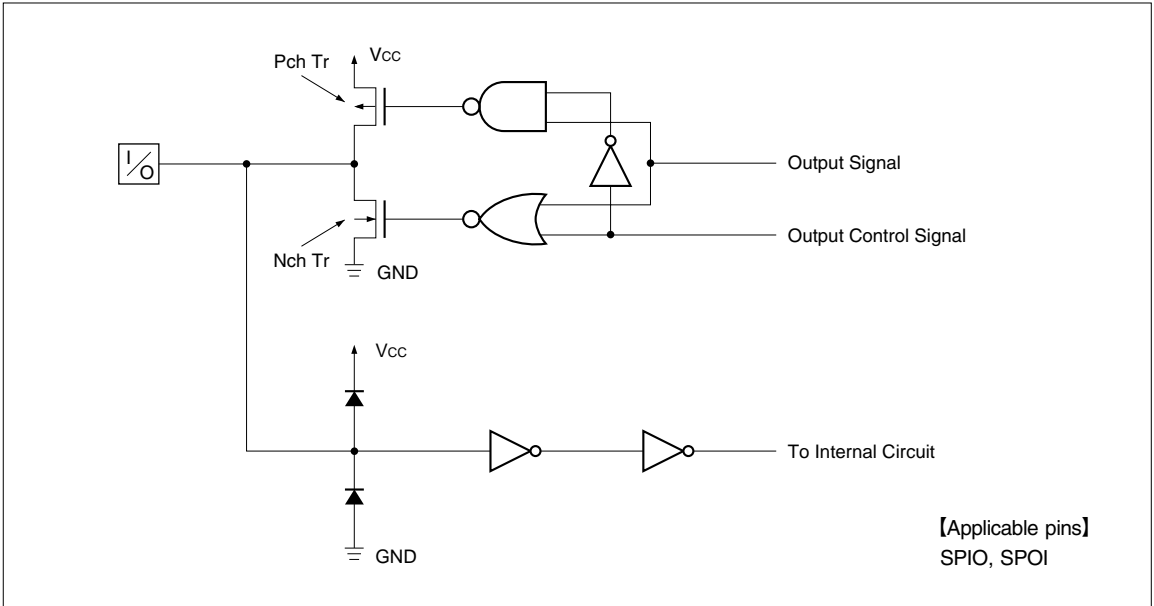


Fig. 3 Input/Output Circuit

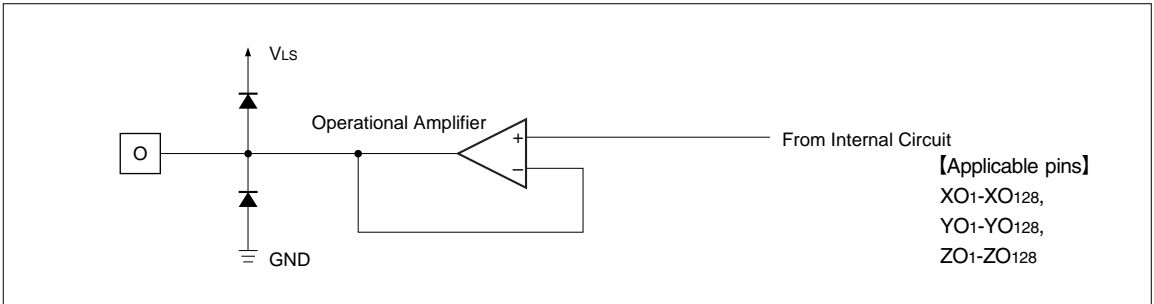


Fig. 4 Output Circuit

## FUNCTIONAL DESCRIPTION

### Pin Functions

SYMBOL	FUNCTION
VCC	Used as power supply pin for digital circuit, connected to +2.5 to +3.6 V.
VLS	Used as power supply pin for analog circuit, connected to +8.0 to +13.0 V.
GND	Used as ground pin, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting , refer to " <a href="#">Functional Operations</a> ".
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to " <a href="#">Functional Operations</a> ".
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
VH0-VH256 VL0-VL256	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to " <a href="#">Output Voltage Value</a> ". For internal gamma correction, refer to " <a href="#">Gamma Correction Value</a> ". Observe the following relation for input voltage. $VLS > VH_0 \geq VH_{32} \geq \dots \geq VH_{256} \geq VL_{256} \geq \dots \geq VL_{32} \geq VL_0 > GND$ .
XA0-XA7, YA0-YA7 ZA0-ZA7, XB0-XB7 YB0-YB7, ZB0-ZB7	Used as data input pins of R, G, and B colors. 8-bit x 2-pixel data are input from data pins at the rising edge of CK. For relation between input data and output voltage values, refer to " <a href="#">Functional Operations</a> " and " <a href="#">Output Voltage Value</a> ". Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
XO1-XO128 YO1-YO128 ZO1-ZO128	Used as LCD drive output pins which output the voltage corresponding to the input of data input pins (XA0 to XA7, YA0 to YA7, ZA0 to ZA7, XB0 to XB7, YB0 to YB7, ZB0 to ZB7). Data of XO1 to XO128 correspond to XA0 to XA7 and XB0 to XB7. Data of YO1 to YO128 correspond to YA0 to YA7 and YB0 to YB7, and data of ZO1 to ZO128 correspond to ZA0 to ZA7 and ZB0 to ZB7. For relation between input data and output voltage values, refer to " <a href="#">Functional Operations</a> " and " <a href="#">Output Voltage Value</a> ".
POLA POLB	Used as input pins for input data polarity exchange, POLA corresponds to XA0 to XA7, YA0 to YA7 and ZA0 to ZA7, and POLB corresponds to XB0 to XB7, YB0 to YB7 and ZB0 to ZB7. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode. For relation between input data and output voltage values, refer to " <a href="#">Output Voltage Value</a> ". These pins are pulled down at the inside.
REV	Used as polarity exchange pin of LCD drive output. Date is taken at the term when LS is "H" and the output polarity of the LCD drive output pin is determined. For exchanging, refer to " <a href="#">Output Characteristics</a> ".

## Functional Operations

The following describes the relation between data input pin and output direction.

Data input pin	XA0-XA7	YA0-YA7	ZA0-ZA7	XB0-XB7	YB0-YB7	ZB0-ZB7	.....	XB0-XB7	YB0-YB7	ZB0-ZB7
Output direction	XO1	YO1	ZO1	XO2	YO2	ZO2	.....	XO128	YO128	ZO128

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO1, YO1, ZO1→XO128, YO128, ZO128)	LEFT SHIFT (ZO128, YO128, XO128→ZO1, YO1, XO1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

### NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

## Output Characteristics

The following describes the relation between REV pin and output polarity of LCD drive pin.

REV	"H"	"L"
XO1	+	-
YO1	-	+
ZO1	+	-
XO2	-	+
YO2	+	-
ZO2	-	+
XO3	+	-
YO3	-	+
:	:	:
XO126	-	+
YO126	+	-
ZO126	-	+
XO127	+	-
YO127	-	+
ZO127	+	-
XO128	-	+
YO128	+	-
ZO128	-	+

### NOTES :

+ : The gray scale voltages corresponding to reference voltage VH0 to VH256 are output.

- : The gray scale voltages corresponding to reference voltage VL0 to VL256 are output.

## Output Voltage Value

Two voltages are selected from all of the reference voltages ( $V_0$ - $V_{256}$ ) by the upper 3-bit data ( $D_7$ ,  $D_6$  and  $D_5$ ) of the 8-bit input data ( $D_7$ ,  $D_6$ ,  $D_5$ ,  $D_4$ ,  $D_3$ ,  $D_2$ ,  $D_1$  and  $D_0$ ) taken by time sharing, and intermediate value is determined by the lower 5-bit data ( $D_4$ ,  $D_3$ ,  $D_2$ ,  $D_1$  and  $D_0$ ).

The  $V_i$  is a reference voltage ( $V_{Hi}$  or  $V_{Li}$ ) that is determined by the polarity exchange input (REV). Relation between input data and output voltage values is shown below.

( $i = 0, 32, 64, 96, 128, 160, 192, 224, 256$ )

INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"
0	$V_0$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 6.61/8.96)/2.13$
1	$V_{32} + (V_0 - V_{32}) \times 31/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 5.74/8.96)/2.13$
2	$V_{32} + (V_0 - V_{32}) \times 30/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4.87/8.96)/2.13$
3	$V_{32} + (V_0 - V_{32}) \times 29/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4/8.96)/2.13$
4	$V_{32} + (V_0 - V_{32}) \times 28/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 3/8.96)/2.13$
5	$V_{32} + (V_0 - V_{32}) \times 27/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 2/8.96)/2.13$
6	$V_{32} + (V_0 - V_{32}) \times 26/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 1/8.96)/2.13$
7	$V_{32} + (V_0 - V_{32}) \times 25/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 8/8)/2.13$
8	$V_{32} + (V_0 - V_{32}) \times 24/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 7/8)/2.13$
9	$V_{32} + (V_0 - V_{32}) \times 23/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 6/8)/2.13$
A	$V_{32} + (V_0 - V_{32}) \times 22/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 5/8)/2.13$
B	$V_{32} + (V_0 - V_{32}) \times 21/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 4/8)/2.13$
C	$V_{32} + (V_0 - V_{32}) \times 20/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 3/8)/2.13$
D	$V_{32} + (V_0 - V_{32}) \times 19/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 2/8)/2.13$
E	$V_{32} + (V_0 - V_{32}) \times 18/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 1/8)/2.13$
F	$V_{32} + (V_0 - V_{32}) \times 17/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 8/8)/2.13$
10	$V_{32} + (V_0 - V_{32}) \times 16/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 7/8)/2.13$
11	$V_{32} + (V_0 - V_{32}) \times 15/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 6/8)/2.13$
12	$V_{32} + (V_0 - V_{32}) \times 14/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 5/8)/2.13$
13	$V_{32} + (V_0 - V_{32}) \times 13/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 4/8)/2.13$
14	$V_{32} + (V_0 - V_{32}) \times 12/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 3/8)/2.13$
15	$V_{32} + (V_0 - V_{32}) \times 11/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 2/8)/2.13$
16	$V_{32} + (V_0 - V_{32}) \times 10/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 1/8)/2.13$
17	$V_{32} + (V_0 - V_{32}) \times 9/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 8/8)/2.13$
18	$V_{32} + (V_0 - V_{32}) \times 8/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 7/8)/2.13$
19	$V_{32} + (V_0 - V_{32}) \times 7/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 6/8)/2.13$
1A	$V_{32} + (V_0 - V_{32}) \times 6/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 5/8)/2.13$
1B	$V_{32} + (V_0 - V_{32}) \times 5/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 4/8)/2.13$
1C	$V_{32} + (V_0 - V_{32}) \times 4/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 3/8)/2.13$
1D	$V_{32} + (V_0 - V_{32}) \times 3/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 2/8)/2.13$
1E	$V_{32} + (V_0 - V_{32}) \times 2/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 1/8)/2.13$
1F	$V_{32} + (V_0 - V_{32}) \times 1/32$	$V_{224}$



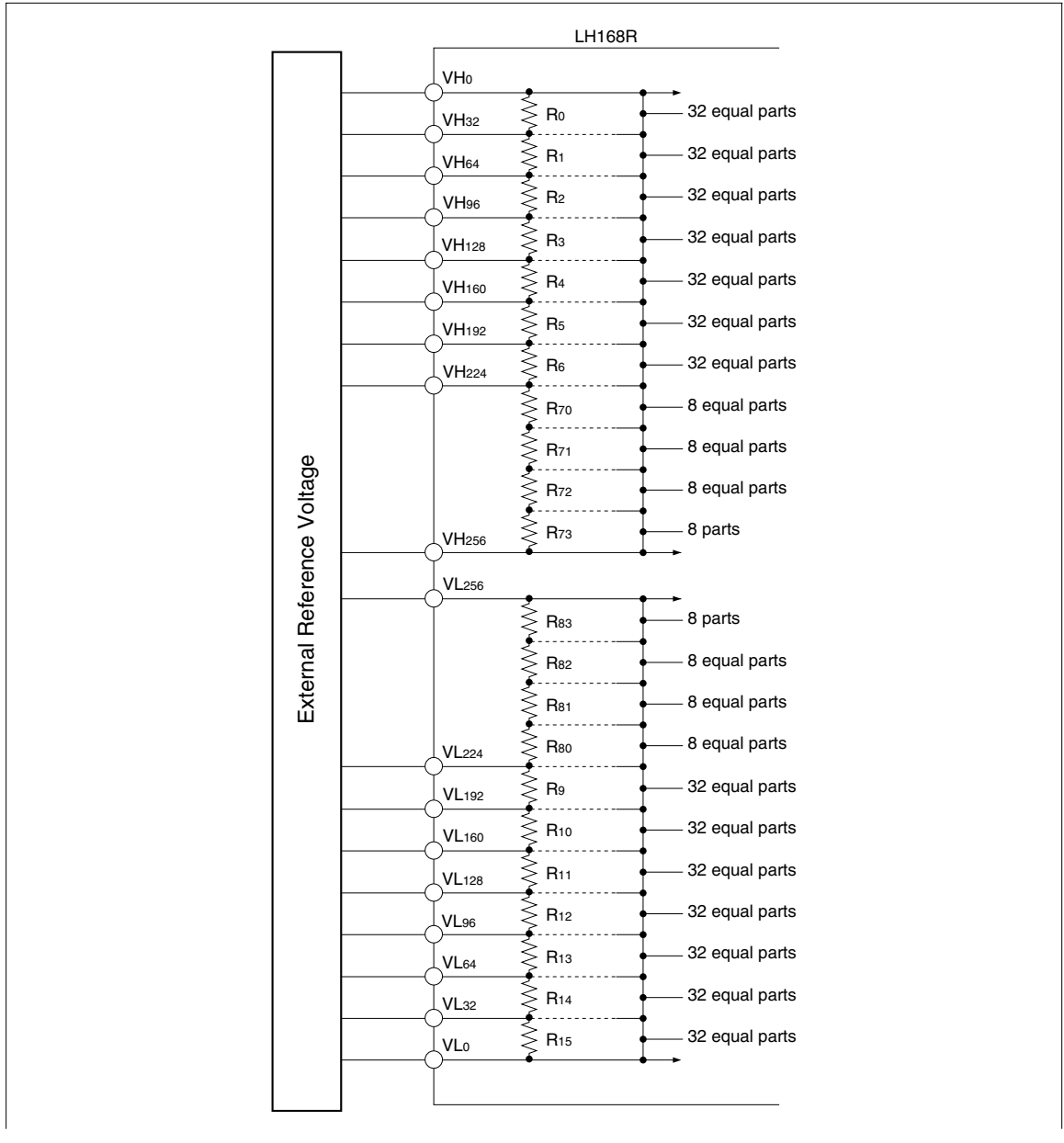
INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"
20	$V_{32}$	$V_{224} + (V_{192} - V_{224}) \times 1/32$
21	$V_{64} + (V_{32} - V_{64}) \times 31/32$	$V_{224} + (V_{192} - V_{224}) \times 2/32$
22	$V_{64} + (V_{32} - V_{64}) \times 30/32$	$V_{224} + (V_{192} - V_{224}) \times 3/32$
:	:	:
3D	$V_{64} + (V_{32} - V_{64}) \times 3/32$	$V_{224} + (V_{192} - V_{224}) \times 30/32$
3E	$V_{64} + (V_{32} - V_{64}) \times 2/32$	$V_{224} + (V_{192} - V_{224}) \times 31/32$
3F	$V_{64} + (V_{32} - V_{64}) \times 1/32$	$V_{192}$
40	$V_{64}$	$V_{192} + (V_{160} - V_{192}) \times 1/32$
41	$V_{96} + (V_{64} - V_{96}) \times 31/32$	$V_{192} + (V_{160} - V_{192}) \times 2/32$
42	$V_{96} + (V_{64} - V_{96}) \times 30/32$	$V_{192} + (V_{160} - V_{192}) \times 3/32$
:	:	:
5D	$V_{96} + (V_{64} - V_{96}) \times 3/32$	$V_{192} + (V_{160} - V_{192}) \times 30/32$
5E	$V_{96} + (V_{64} - V_{96}) \times 2/32$	$V_{192} + (V_{160} - V_{192}) \times 31/32$
5F	$V_{96} + (V_{64} - V_{96}) \times 1/32$	$V_{160}$
60	$V_{96}$	$V_{160} + (V_{128} - V_{160}) \times 1/32$
61	$V_{128} + (V_{96} - V_{128}) \times 31/32$	$V_{160} + (V_{128} - V_{160}) \times 2/32$
62	$V_{128} + (V_{96} - V_{128}) \times 30/32$	$V_{160} + (V_{128} - V_{160}) \times 3/32$
:	:	:
7D	$V_{128} + (V_{96} - V_{128}) \times 3/32$	$V_{160} + (V_{128} - V_{160}) \times 30/32$
7E	$V_{128} + (V_{96} - V_{128}) \times 2/32$	$V_{160} + (V_{128} - V_{160}) \times 31/32$
7F	$V_{128} + (V_{96} - V_{128}) \times 1/32$	$V_{128}$
80	$V_{128}$	$V_{128} + (V_{96} - V_{128}) \times 1/32$
81	$V_{160} + (V_{128} - V_{160}) \times 31/32$	$V_{128} + (V_{96} - V_{128}) \times 2/32$
82	$V_{160} + (V_{128} - V_{160}) \times 30/32$	$V_{128} + (V_{96} - V_{128}) \times 3/32$
:	:	:
9D	$V_{160} + (V_{128} - V_{160}) \times 3/32$	$V_{128} + (V_{96} - V_{128}) \times 30/32$
9E	$V_{160} + (V_{128} - V_{160}) \times 2/32$	$V_{128} + (V_{96} - V_{128}) \times 31/32$
9F	$V_{160} + (V_{128} - V_{160}) \times 1/32$	$V_{96}$
A0	$V_{160}$	$V_{96} + (V_{64} - V_{96}) \times 1/32$
A1	$V_{192} + (V_{160} - V_{192}) \times 31/32$	$V_{96} + (V_{64} - V_{96}) \times 2/32$
A2	$V_{192} + (V_{160} - V_{192}) \times 30/32$	$V_{96} + (V_{64} - V_{96}) \times 3/32$
:	:	:
BD	$V_{192} + (V_{160} - V_{192}) \times 3/32$	$V_{96} + (V_{64} - V_{96}) \times 30/32$
BE	$V_{192} + (V_{160} - V_{192}) \times 2/32$	$V_{96} + (V_{64} - V_{96}) \times 31/32$
BF	$V_{192} + (V_{160} - V_{192}) \times 1/32$	$V_{64}$
C0	$V_{192}$	$V_{64} + (V_{32} - V_{64}) \times 1/32$
C1	$V_{224} + (V_{192} - V_{224}) \times 31/32$	$V_{64} + (V_{32} - V_{64}) \times 2/32$
C2	$V_{224} + (V_{192} - V_{224}) \times 30/32$	$V_{64} + (V_{32} - V_{64}) \times 3/32$
:	:	:
DD	$V_{224} + (V_{192} - V_{224}) \times 3/32$	$V_{64} + (V_{32} - V_{64}) \times 30/32$
DE	$V_{224} + (V_{192} - V_{224}) \times 2/32$	$V_{64} + (V_{32} - V_{64}) \times 31/32$
DF	$V_{224} + (V_{192} - V_{224}) \times 1/32$	$V_{32}$

INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"
E0	$V_{224}$	$V_{32} + (V_0 - V_{32}) \times 1/32$
E1	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 1/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 2/32$
E2	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 2/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 3/32$
E3	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 3/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 4/32$
E4	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 4/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 5/32$
E5	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 5/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 6/32$
E6	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 6/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 7/32$
E7	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 7/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 8/32$
E8	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 8/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 9/32$
E9	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 1/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 10/32$
EA	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 2/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 11/32$
EB	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 3/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 12/32$
EC	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 4/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 13/32$
ED	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 5/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 14/32$
EE	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 6/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 15/32$
EF	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 7/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 16/32$
F0	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 8/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 17/32$
F1	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 1/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 18/32$
F2	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 2/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 19/32$
F3	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 3/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 20/32$
F4	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 4/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 21/32$
F5	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 5/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 22/32$
F6	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 6/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 23/32$
F7	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 7/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 24/32$
F8	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 8/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 25/32$
F9	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 1/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 26/32$
FA	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 2/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 27/32$
FB	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 3/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 28/32$
FC	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 29/32$
FD	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4.87/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 30/32$
FE	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 5.74/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 31/32$
FF	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 6.61/8.96)/2.13$	$V_0$

### $\gamma$ (Gamma) Correction Value

Between reference voltage input pins VH0 and VH256, 256 resistors are connected in series. And between reference voltage input pins VL0 and VL256, 256 resistors are connected in series. No resistor is connected between reference voltage input pins VH256 and VL256.

The  $\gamma$  correction curve is a broken line connected between intermediate voltage inputs (VH32, VH64, VH96, VH128, VH160, VH192, VH224, VL32, VL64, VL96, VL128, VL160, VL192 and VL224). Each  $\gamma$  correction value between the intermediate voltage inputs is divided into 32 parts by resistor.



The following shows the ratio of  $\gamma$  correction resistance, when  $R_0$  equals 1.

R0	1.00
R1	0.60
R2	0.49
R3	0.52
R4	0.60
R5	0.74
R6	1.00
R70	0.33
R71	0.36
R72	0.45
R73	0.99

R83	0.99
R82	0.45
R81	0.36
R80	0.33
R9	1.00
R10	0.74
R11	0.60
R12	0.52
R13	0.49
R14	0.60
R15	1.00

The following shows the ratio of  $\gamma$  correction resistance of R73 and R83, when R730 equals 1.

R73	R730	1.00
	R731	1.00
	R732	1.00
	R733	1.00
	R734	0.87
	R735	0.87
	R736	0.87
	R737 (VH256 side)	2.35

R83	R837 (VL256 side)	2.35
	R836	0.87
	R835	0.87
	R834	0.87
	R833	1.00
	R832	1.00
	R831	1.00
	R830	1.00

## PRECAUTIONS

### Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

$V_{CC} \rightarrow$  logic input  $\rightarrow V_{LS}, V_{H0}\text{-}V_{H256}, V_{L0}\text{-}V_{L256}$

When disconnecting the power supply, follow the reverse sequence.

### Reference voltage input

The relation of the reference voltage input is shown here.

$$V_{LS} > V_{H0} \geq V_{H32} \geq \dots \geq V_{H224} \geq V_{H256} \geq 0.5V_{LS} \\ \geq V_{L256} \geq V_{L224} \geq \dots \geq V_{L32} \geq V_{L0} > \text{GND}$$

### Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

### Target output load

This IC is designed for a 200 pF output load capacity. When using this IC for other than 200 pF panels, confirm the device is having no problem before using it.

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	V <sub>CC</sub>	-0.3 to +6.0	V	1, 2
	V <sub>LS</sub>	V <sub>LS</sub>	-0.3 to +14.0	V	
Input voltage	V <sub>I</sub>	V <sub>H0</sub> -V <sub>L0</sub>	-0.3 to V <sub>LS</sub> + 0.3	V	
	V <sub>I</sub>	SPIO, SPOI, CK, LS, REV, LBR, POLA, POLB, XA0-XA7, XB0-XB7, YA0-YA7, YB0-YB7, ZA0-ZA7, ZB0-ZB7	-0.3 to V <sub>CC</sub> + 0.3	V	
Output voltage	V <sub>O</sub>	SPIO, SPOI	-0.3 to V <sub>CC</sub> + 0.3	V	
	V <sub>O</sub>	XO1-ZO128	-0.3 to V <sub>LS</sub> + 0.3	V	
Storage temperature	T <sub>STG</sub>		-45 to +125	°C	

**NOTES :**

1. T<sub>A</sub> = +25 °C
2. The maximum applicable voltage on any pin with respect to GND (0 V).

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	+2.5		+3.6	V	1
	V <sub>LS</sub>	+8.0		+13.0	V	
Reference voltage input	V <sub>H0</sub> -V <sub>H256</sub>	0.5V <sub>CC</sub>		V <sub>LS</sub> - 0.2	V	
	V <sub>L0</sub> -V <sub>L256</sub>	+0.2		0.5V <sub>CC</sub>	V	
Clock frequency	f <sub>CK</sub>			65	MHz	
LCD drive output load capacity	CL			200	pF	
Operating temperature	T <sub>OPR</sub>	-20		+75	°C	

**NOTE :**

1. The applicable voltage on any pin with respect to GND (0 V).

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(V<sub>CC</sub> = +2.5 to +3.6 V, V<sub>LS</sub> = +8.0 to +13.0 V, T<sub>OPR</sub> = -20 to +75 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT.	NOTE
Input "Low" voltage	V <sub>IL</sub>		XA0-XA7, YA0-YA7, ZA0-ZA7, XB0-XB7, YB0-YB7, ZB0-ZB7,	GND		0.3V <sub>CC</sub>	V	
Input "High" voltage	V <sub>IH</sub>		SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB	0.7V <sub>CC</sub>		V <sub>CC</sub>	V	
Output "Low" voltage	V <sub>OL</sub>	I <sub>OL</sub> = 0.3 mA	SPIO, SPOI	GND		GND + 0.4	V	
Output "H" voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.3 mA		V <sub>CC</sub> - 0.4		V <sub>CC</sub>	V	
Input "Low" current	I <sub>ILL1</sub>		XA0-XA7, YA0-YA7, ZA0-ZA7, XB0-XB7, YB0-YB7, ZB0-ZB7, SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB			10	μA	
Input "High" current	I <sub>IH1</sub>		XA0-XA7, YA0-YA7, ZA0-ZA7, XB0-XB7, YB0-YB7, ZB0-ZB7, SPIO, SPOI, CK, LS, LBR, REV			10	μA	
	I <sub>IH2</sub>		POLA, POLB			400	μA	
Supply current (In operation mode)	I <sub>CC1</sub>	f <sub>CK</sub> = 65 MHz f <sub>LS</sub> = 50 kHz (Data sampling state)	V <sub>CC</sub> -GND			14	mA	
Supply current (In standby mode)	I <sub>CC2</sub>	f <sub>CK</sub> = 65 MHz f <sub>LS</sub> = 50 kHz SPI = GND is fixed. (Standby state)	V <sub>CC</sub> -GND			1.5	mA	
Supply current (In operation mode)	I <sub>LS1</sub>	f <sub>CK</sub> = 65 MHz f <sub>LS</sub> = 50 kHz (Data sampling state)	V <sub>LS</sub> -GND			5	mA	
Supply current (In standby mode)	I <sub>LS2</sub>	f <sub>CK</sub> = 65 MHz f <sub>LS</sub> = 50 kHz SPI = GND is fixed. (Standby state)	V <sub>LS</sub> -GND			4	mA	
Output voltage range	V <sub>OUT</sub>		XO1-ZO <sub>128</sub>	GND + 0.2		V <sub>LS</sub> - 0.2	V	1
Deviations between output voltage pins	V <sub>OD</sub>			-10		+10	mV	
Output current	I <sub>O1</sub> -I <sub>O4</sub>				200		μA	2
Resistance between reference voltage input pins	R <sub>GMAH</sub>		VH0-VH <sub>256</sub>		20		kΩ	
	R <sub>GMAL</sub>		VL0-VL <sub>256</sub>		20		kΩ	

**NOTES :**

1. Criterion of evaluating voltage deviations.
  - (a) Between output voltage pins  
Measuring values : Output voltage value at the time after  
10  $\mu$ s at the rising edge of LS.  
(Average of several times)  
(Conditions) Output load capacity is 200 pF.  
In a state when the reference voltage is fixed.  
Expecting values : Calculated following these specifications.  
(Conditions) In a state when the reference voltage is fixed.
  - (b) Between LCD drivers  
Measuring values : Applicable to (a).  
(Conditions) Applicable to (a).  
Expecting values : Applicable to (a).  
(Conditions) Applicable to (a).  
Each input voltage between the LCD drivers must be made perfectly equal by connecting corresponding reference voltage input pins.
2. I<sub>o1</sub> : Applied voltage = 8.0 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
Output voltage = 7.5 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
V<sub>LS</sub> = 10.0 V  
I<sub>o2</sub> : Applied voltage = 7.0 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
Output voltage = 7.5 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
V<sub>LS</sub> = 10.0 V  
I<sub>o3</sub> : Applied voltage = 3.0 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
Output voltage = 2.5 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
V<sub>LS</sub> = 10.0 V  
I<sub>o4</sub> : Applied voltage = 2.0 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
Output voltage = 2.5 V for output pins XO<sub>1</sub> to ZO<sub>128</sub>.  
V<sub>LS</sub> = 10.0 V

**AC Characteristics** ( $V_{CC} = +2.5$  to  $+2.7$  V,  $V_{LS} = +8.0$  to  $+13.0$  V,  $T_{OPR} = -20$  to  $+75$  °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f <sub>CK</sub>		CK			40	MHz
"H" level pulse width	t <sub>CWH</sub>			8			ns
"L" level pulse width	t <sub>CWL</sub>			8			ns
Input rise time	t <sub>CR</sub>					10	ns
Input fall time	t <sub>CF</sub>					10	ns
Data setup time	t <sub>SUD</sub>		XA0-XA7, YA0-YA7, ZA0-ZA7, XB0-XB7, YB0-YB7, ZB0-ZB7, POLA, POLB	6			ns
Data hold time	t <sub>HD</sub>			6			ns
Start pulse setup time	t <sub>SUSP</sub>		SPIO, SPOI	6			ns
Start pulse hold time	t <sub>HSP</sub>			6			ns
Start pulse width	t <sub>WSP</sub>					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t <sub>DSP</sub>	CL = 15 pF				19	ns
LCD drive output delay time 1	t <sub>DO1</sub>	CL = 200 pF	XO1-ZO128			3	μs
LCD drive output delay time 2	t <sub>DO2</sub>	CL = 200 pF				10	μs
LS signal-SPI signal setup time	t <sub>LSSP</sub>		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t <sub>HLS</sub>			7			ns
LS signal "H" level width	t <sub>WLS</sub>			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t <sub>SURV</sub>		REV	14			ns
REV signal-LS signal hold time	t <sub>HRV</sub>			10			ns



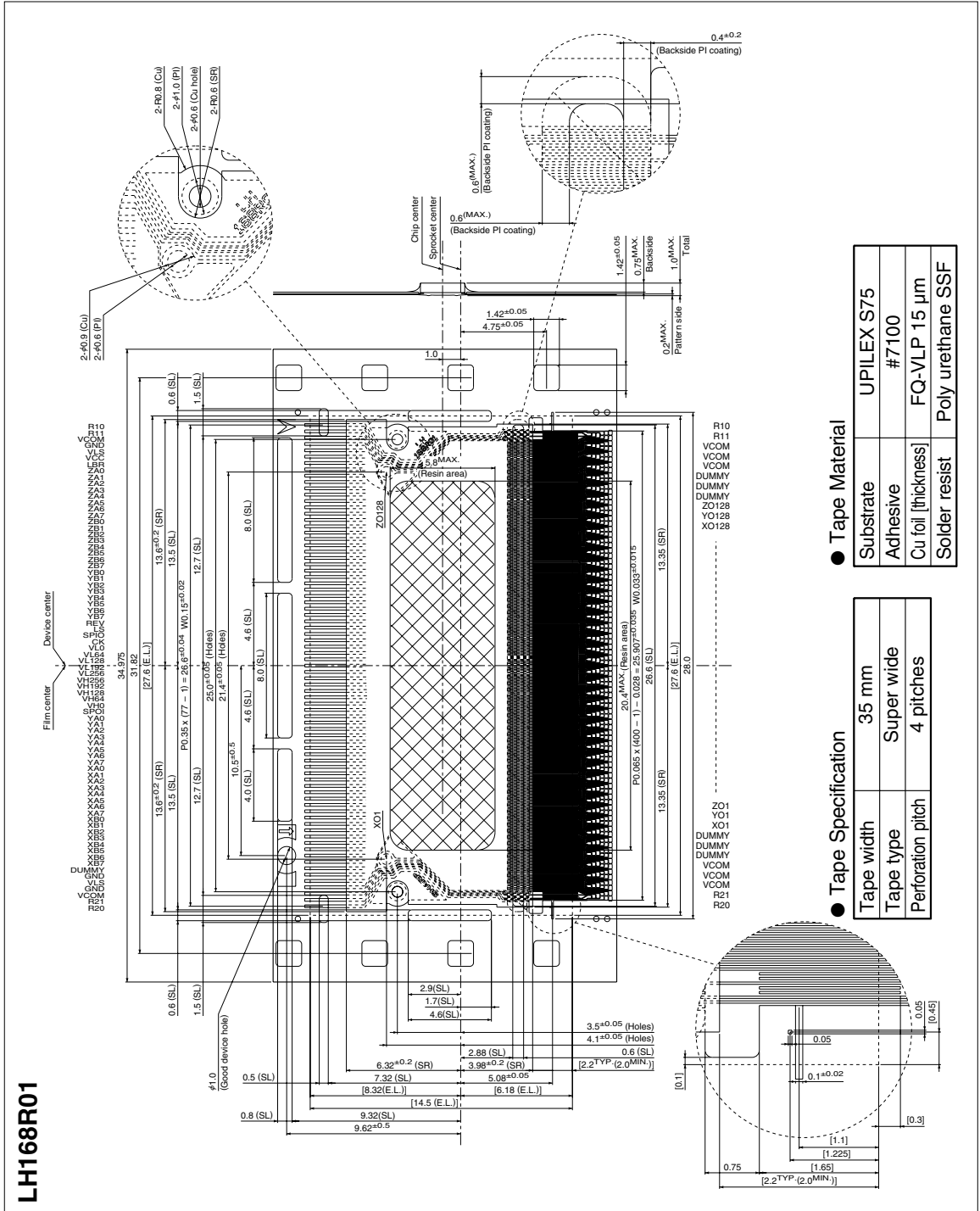
(V<sub>CC</sub> = +2.7 to +3.6 V, V<sub>LS</sub> = +8.0 to +13.0 V, T<sub>OPR</sub> = -20 to +75 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f <sub>CK</sub>		CK			65	MHz
"H" level pulse width	t <sub>CWH</sub>			4			ns
"L" level pulse width	t <sub>CWL</sub>			4			ns
Input rise time	t <sub>CR</sub>					10	ns
Input fall time	t <sub>CF</sub>					10	ns
Data setup time	t <sub>SUD</sub>		XA0-XA7, YA0-YA7, ZA0-ZA7, XB0-XB7, YB0-YB7, ZB0-ZB7, POLA, POLB	4			ns
Data hold time	t <sub>HD</sub>			1			ns
Start pulse setup time	t <sub>SUSP</sub>		SPIO, SPOI	3			ns
Start pulse hold time	t <sub>HSP</sub>			2			ns
Start pulse width	t <sub>WSP</sub>					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t <sub>DSP</sub>	CL = 15 pF				11	ns
LCD drive output delay time 1	t <sub>DO1</sub>	CL = 200 pF	XO1-ZO <sub>128</sub>			3	μs
LCD drive output delay time 2	t <sub>DO2</sub>	CL = 200 pF				10	μs
LS signal-SPI signal setup time	t <sub>LSSP</sub>		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t <sub>HLS</sub>			7			ns
LS signal "H" level width	t <sub>WLS</sub>			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t <sub>SURV</sub>		REV	14			ns
REV signal-LS signal hold time	t <sub>HRV</sub>			10			ns



PACKAGE

(Unit : mm)



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