

LH1694

256-output TFT-LCD Gate Driver IC

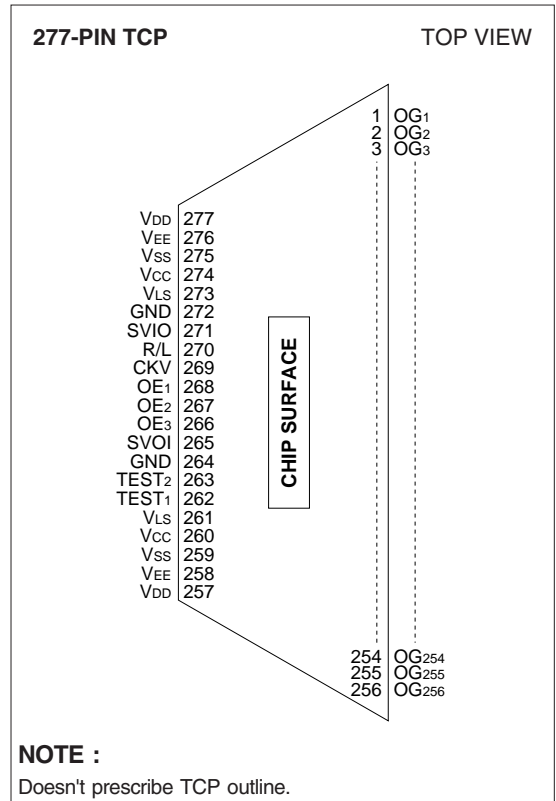
DESCRIPTION

The LH1694 is a 256-output TFT-LCD gate driver IC.

FEATURES

- Number of LCD drive outputs : 256
- LCD drive output sequence :
Output shift direction can be selected
OG₁→OG₂₅₆ or OG₂₅₆→OG₁
- Enable chain connection
- Usable with both positive/negative power supplies
- Output signal masking function
- Input signal voltage : +2.7 to +3.6 V
- LCD drive voltage : +16.0 to +42.0 V
- Operating temperature : -30 to +85 °C
- Package : 277-pin TCP (Tape Carrier Package)

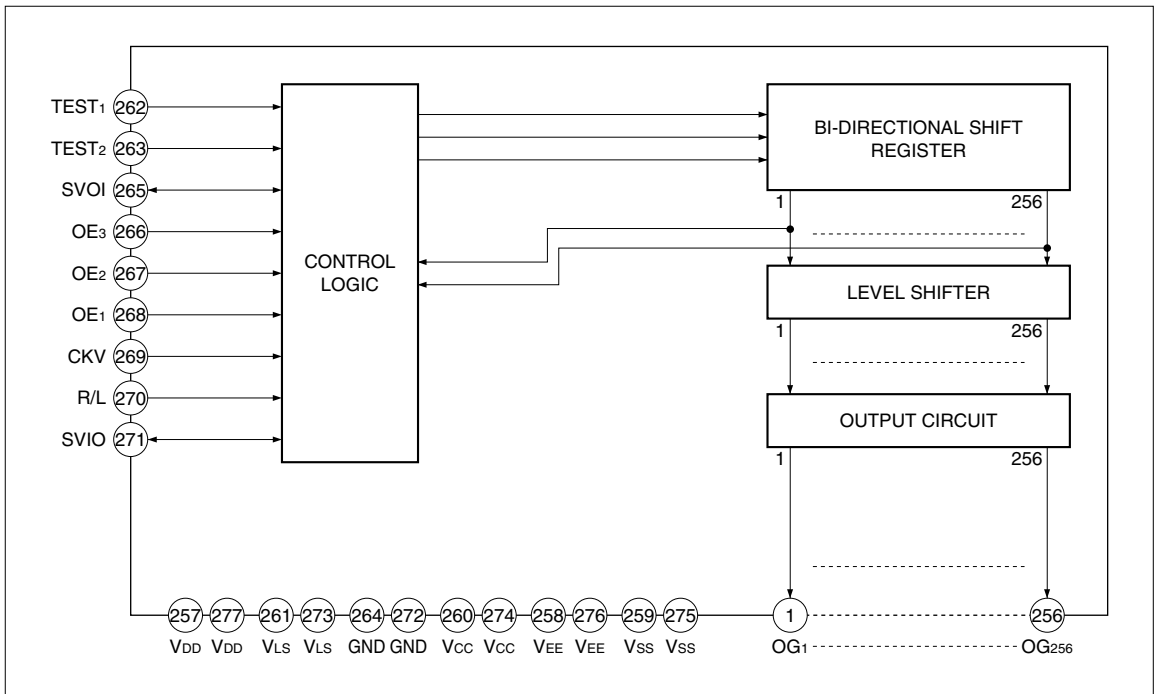
PIN CONNECTIONS



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 256	OG1-OG256	O	LCD drive output pins
257, 277	V _{DD}	-	Power supply pins for LCD drive
258, 276	V _{EE}	-	Power supply pins for LCD drive
259, 275	V _{SS}	-	Power supply pins for logic system
260, 274	V _{CC}	-	Power supply pins for logic system
261, 273	V _{LS}	-	Power supply pins for logic input/output systems
264, 272	GND	-	Ground pins for logic input
262, 263	TEST ₁ , TEST ₂	I	IC test pins
265	SVOI	I/O	Vertical scanning start pulse input/output pin
266 to 268	OE ₃ -OE ₁	I	Input pins for output enable
269	CKV	I	Vertical shift clock input pin
270	R/L	I	Pin for selecting bi-directional shift register and setting cascade sequence
271	SVIO	I/O	Vertical scanning start pulse input/output pin

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Control Logic	Used to create signals necessary for mode selecting signal, cascade sequence setting signal and for operation of bi-directional shift register.
Bi-directional Shift Register	Used as transfer circuit of LCD drive output start signal. It is possible to set LCD drive output sequence of OG ₁ →OG ₂₅₆ direction or OG ₂₅₆ →OG ₁ direction.
Level Shifter	Used as circuit which shifts LCD drive output signals transferred by bi-directional shift register to V _{DD} -V _{EE} level.
Output Circuit	Configured with output buffers to output V _{DD} -V _{EE} level.

INPUT/OUTPUT CIRCUITS

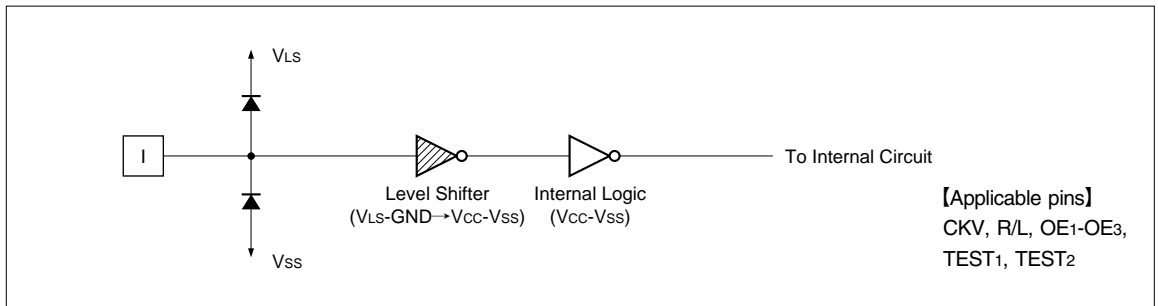


Fig. 1 Input Circuit

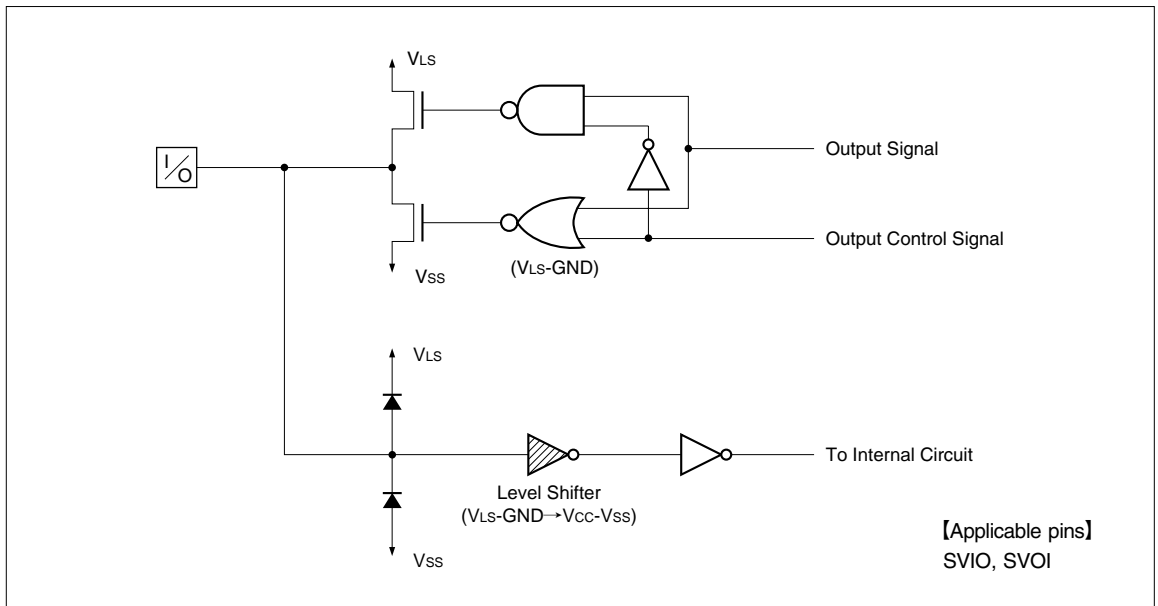


Fig. 2 Input/Output Circuit

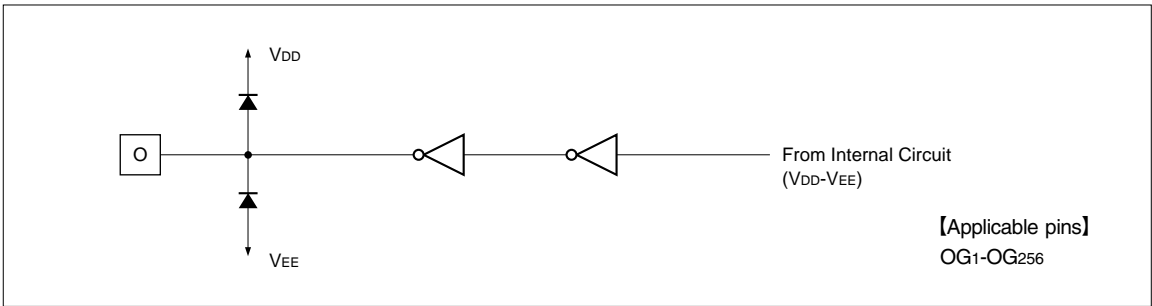


Fig. 3 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
VDD	Used as power supply pin for high level LCD drive.
VLS	Used as power supply pin for input level shifters.
GND	Used as power supply pin for input level shifters.
VCC	Used as power supply pin for logic system, normally connected to Vss + 5.0 V.
VEE	Used as power supply pin for low level LCD drive.
Vss	Used as logic system power supply pin.
CKV	Used as vertical shift clock pulse input pin.
SVIO SVOI	Used as vertical scanning start pulse input/output pins. Data input/output pins for shift register. During input, data is read at the rising edge of the CKV. During output, data is output at the falling edge of the CKV. <ul style="list-style-type: none"> When R/L = "H". SVOI is set to data output pin for next cascade, and SVIO is set to input pin for shift data. When R/L = "L". SVOI is set to input pin for shift data, and SVIO is set to data output pin for next cascade.
R/L	Used as input pin for selecting the shift direction of bi-directional shift register and for setting the sequence of cascade connection. LCD drive outputs shift from OG1 to OG256 when set to "H". LCD drive outputs shift from OG256 to OG1 when set to "L".
OE1 OE2 OE3	Input pins for output-enable. LCD drive output is set to "L", when OE1, OE2, and OE3 pins are set to "H", and it has no relation with clock input. Relationship between enable control and output pins; OE1 : OG1, OG4 ... OG250, OG253, OG256 OE2 : OG2, OG5 ... OG251, OG254 OE3 : OG3, OG6 ... OG252, OG255
TEST1 TEST2	Used as input pins for IC testing. Must be set to "H".
OG1-OG256	Used as output pins for LCD drive output, and which output data at 2 levels. <ul style="list-style-type: none"> Selecting data is output at VDD level . Non-selecting data is output at VEE level .

Functional Operations

LH1694 can select the LCD drive output level (OG₁ to OG₂₅₆) by the set of the input signal (CKV, SVIO, SVOI, OE₁, OE₂, OE₃).

When the pin for selecting the bi-directional shift register (R/L) is set to "H", LCD drive outputs shift from OG₁ to OG₂₅₆, and when set to "L", LCD drive outputs shift from OG₂₅₆ to OG₁.

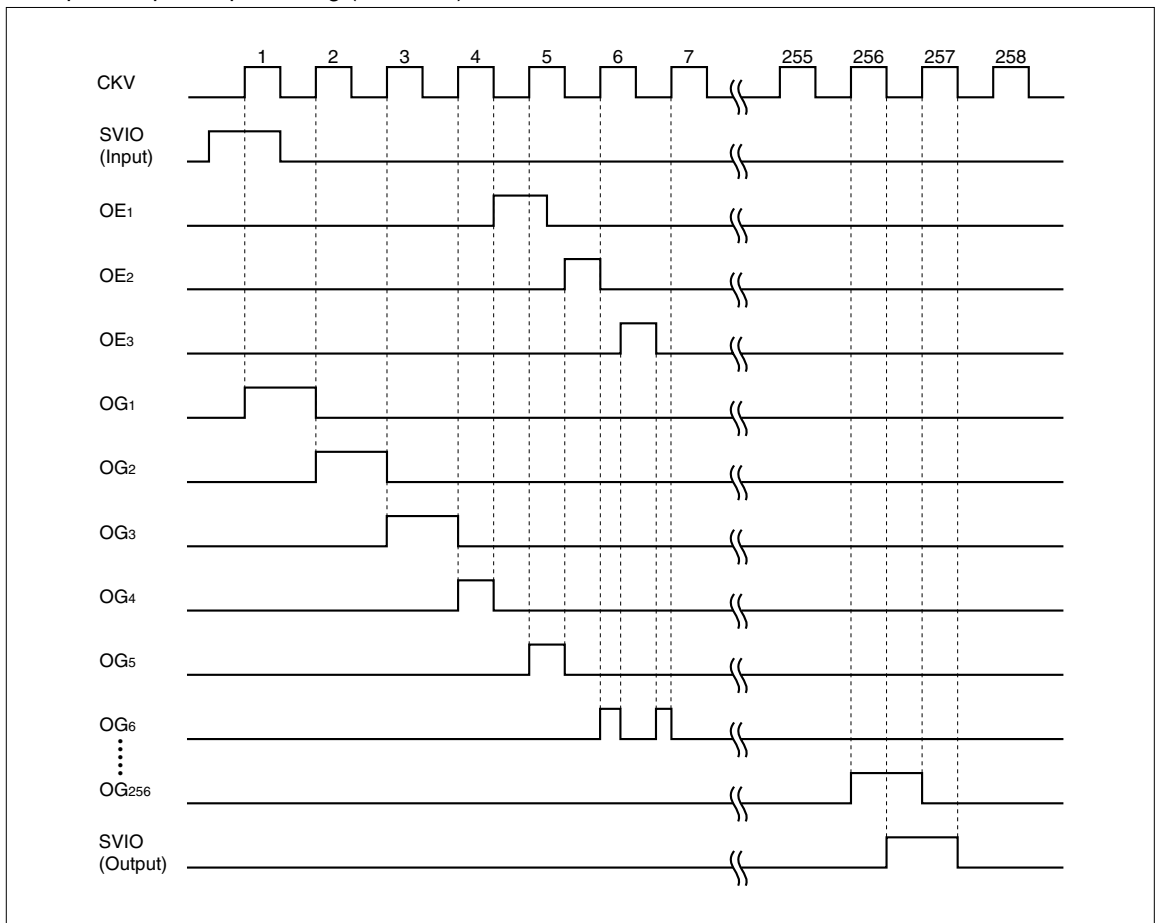
OE₁, OE₂ and OE₃ are signals for output-enable. Output pins output non-selecting data (V_{EE} level) when OE₁ to OE₃ pins are set to "H" and it has no relation with input clock.

While R/L = "H" input data from SVIO is read at the rising edge of shift clock (CKV), and outputs to LCD drive output pin OG₁ at the width for one

cycle of shift clock. Next LCD drive output pins from OG₂ to OG₂₅₆ are sequentially shifted at the rising edge of the CKV for one cycle. Shift signal of OG₂₅₆ is read at the falling edge of the clock signal, and the input data for the next cascade is output from the SVOI pin.

While R/L = "L" input data from SVOI is read at the rising edge of shift clock (CKV), and outputs to LCD drive output pin OG₂₅₆ at the width for one cycle of shift clock. Next LCD drive output pins from OG₂₅₅ to OG₁ are sequentially shifted at the rising edge of the CKV for one cycle. Shift signal of OG₁ is read at the falling edge of the clock signal and the input data for the next cascade is output from the SVIO pin.

Example of Input/Output Timing (R/L = "H")



PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

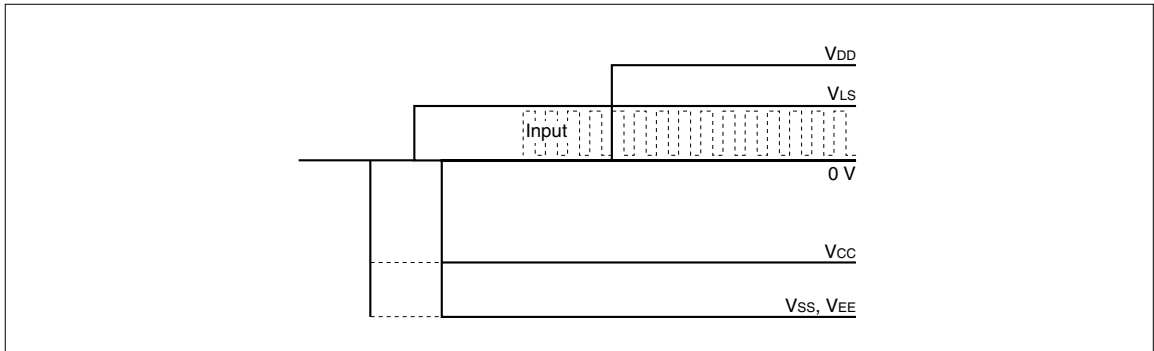
Logic system power supply (V_{LS}) or internal logic system power supply (V_{SS}, V_{CC}; V_{CC} > V_{SS}) → logic input → LCD drive power supply (V_{EE}, V_{DD})

It is possible to set voltage V_{EE} to the same as V_{SS}. When connecting the power supply when V_{EE} = V_{SS}, observe the following sequence and the recommended sequence figure shown below.

Logic system power supply (V_{LS}), internal logic system power supply (V_{SS}, V_{CC}; V_{CC} > V_{SS}) and low-level LCD drive power supply (V_{EE}) → logic input → high-level LCD drive power supply (V_{DD})

When disconnecting the power supply, follow the reverse sequence.

Since the logic state of the internal circuit is unstable immediately after the logic system power is supplied, input CKV and SVIO (or SVOI) while initializing the internal circuit (minimum input clock number is 256 CKV).



Input pin setting

Input pins other than CKV, SVIO and SVOI must be set to "H" or "L" level.

Maximum ratings

When connecting or disconnecting the power, this IC must be used within the range of the absolute maximum ratings.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V _{DD}	V _{DD}	-0.3 to +45.0	V	1, 2
	V _{LS}	V _{LS}	-0.3 to +7.0	V	
	V _{CC} - V _{SS}	V _{CC} , V _{SS}	-0.3 to +7.0	V	
	V _{EE} - V _{SS}	V _{EE} , V _{SS}	-0.3 to +45.0	V	
	V _{DD} - V _{EE} (V _{SS})	V _{DD} , V _{EE} , V _{SS}	-0.3 to +45.0	V	
Input voltage	V _{IN}	CKV, SVIO, SVOI, R/L, OE ₁ -OE ₃ , TEST ₁ , TEST ₂	-0.3 to V _{LS} + 0.3	V	
Storage temperature	T _{STG}		-45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to 0 V.

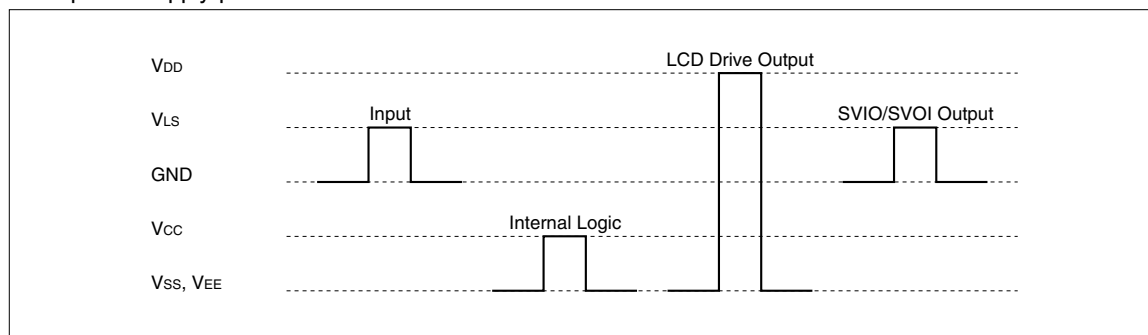
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{DD}	+5.5		+35.0	V	1
	V _{LS}	+2.7	+3.3	+3.6	V	
	V _{SS}	-20.0		-5.0	V	
	V _{CC}	V _{SS} + 4.5		V _{SS} + 5.5	V	
	V _{EE} - V _{SS}	0		+11.0	V	
	V _{DD} - V _{EE} (V _{SS})	+16.0	+25.0	+42.0	V	
Input voltage	V _{IN}	0		V _{LS}	V	
Operating temperature	T _{OPR}	-30		+85	°C	

NOTE :

1. The applicable voltage on any pin with respect to 0 V.

Each power supply pin of LH1694 is set as shown below.



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{LS} = +2.7 to +3.6 V, V_{EE} = V_{SS}, T_{OPR} = -30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}	V _{LS} = 2.7 to 3.0 V	CKV, SVIO, SVOI, OE1-OE3, R/L			0.2V _{LS}	V	
		V _{LS} = 3.0 to 3.6 V				0.3V _{LS}	V	
Input "High" voltage	V _{IH}	V _{LS} = 2.7 to 3.0 V		0.8V _{LS}			V	
		V _{LS} = 3.0 to 3.6 V		0.7V _{LS}			V	
Output "Low" voltage	V _{OL}	I _{OL} = 0.4 mA	OG1-OG ₂₅₆			V _{EE} + 0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} - 0.4			V	
Input "Low" current	I _{IL}	V _I = 0 V	CKV, SVIO, SVOI, OE1-OE3, R/L			5.0	μA	
Input "High" current	I _{IH}	V _I = V _{LS}				5.0	μA	1
Supply current	I _{DD}					100	μA	2
	I _{LS}					1.5	mA	
	I _{CC}					100	μA	
	I _{EE}					100	μA	

NOTES :

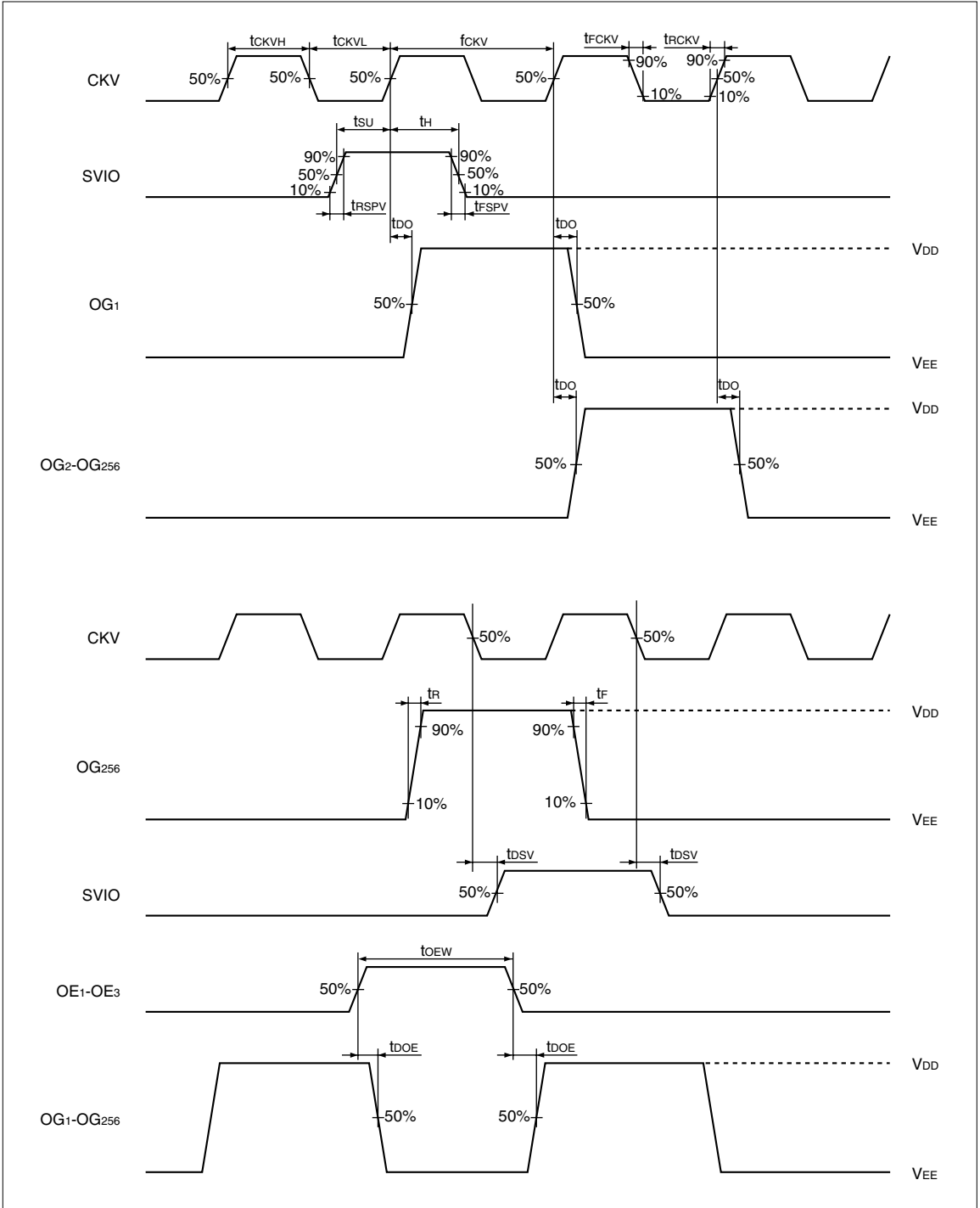
- All input pins : 3.3 V
- CKV : Frequency = 31 kHz, "L" period width t_{wL} = 16.2 μs
 SVIO : Frequency = 60 Hz
 OE1 to OE3 : 0 V
 Other input pins : 3.3 V
 All output pins are opened.

AC Characteristics

(V_{LS} = +2.7 to +3.6 V, V_{EE} = V_{SS}, T_{OPR} = -30 to +85 °C)

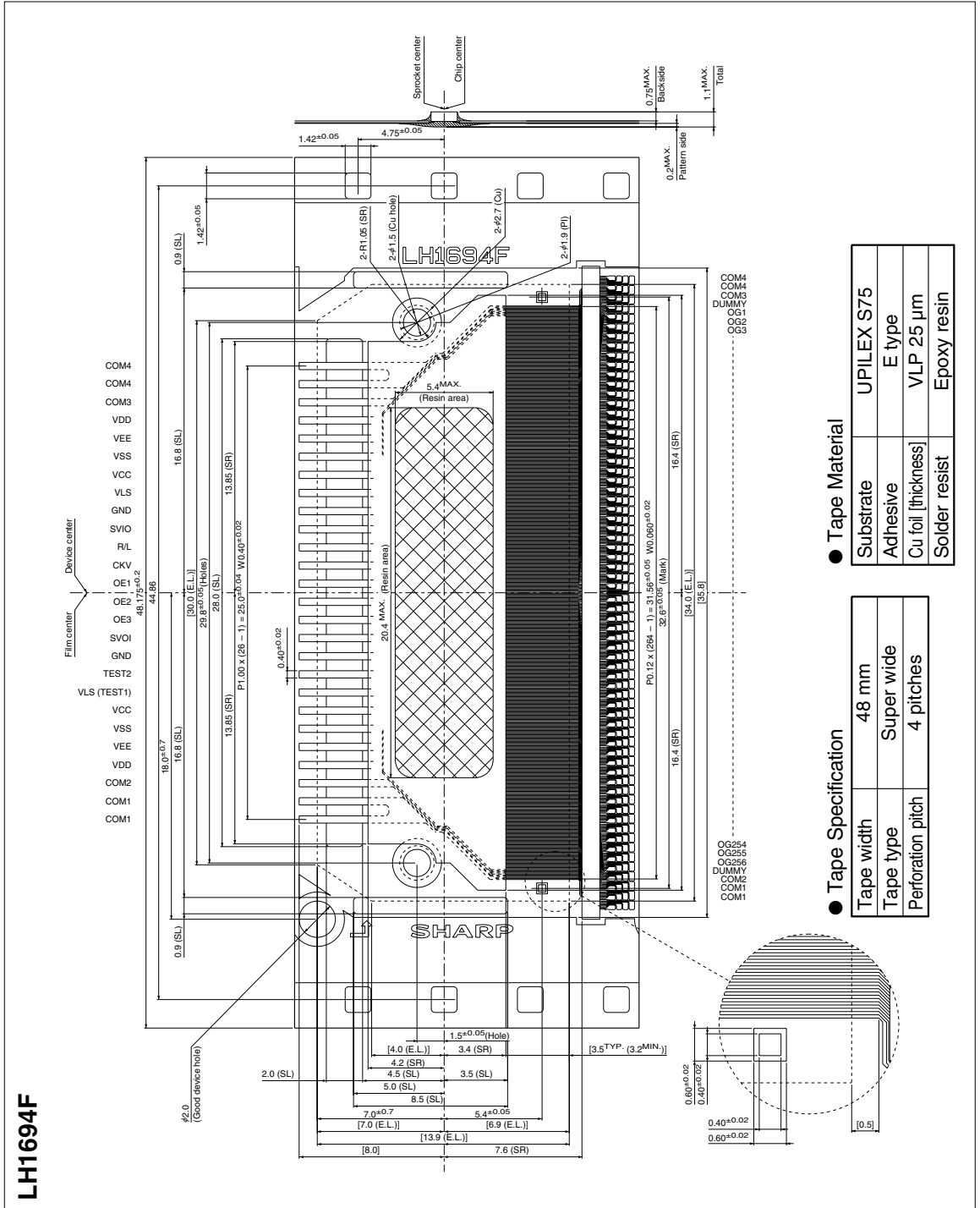
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f _{CKV}		CKV			100	kHz
"H" clock pulse width	t _{CLVH}			1.0			μs
"L" clock pulse width	t _{CKVL}			1.0			μs
Clock rise time	t _{RCKV}					100	ns
Clock fall time	t _{FCKV}					100	ns
Data setup time	t _{SU}		CKV, SVIO, SVOI	100			ns
Data hold time	t _H			300			ns
Pulse rise time	t _{RSPV}		SVIO, SVOI			100	ns
Pulse fall time	t _{FSPV}					100	ns
OE enable time	t _{OEW}		OE1-OE3	1.0			μs
Output transfer delay time 1	t _{DO}	C _L = 300 pF	OG1-OG ₂₅₆			1.0	μs
Output rise time	t _R					1.0	μs
Output fall time	t _F					1.0	μs
Output transfer delay time 2	t _{DOE}						1.0
Output transfer delay time 3	t _{DSV}	C _L = 50 pF	SVIO, SVOI			1.0	μs

Timing Chart



PACKAGE

(Unit : mm)



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