Product Overview

SHARP®

Integrated Circuits Group

ID246 Series

Flash Memory Card

(Model Numbers: ID246xxx)

Spec No.: CPS0008E-001

● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2). even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Introduction

This datasheet is for SHARP's ID246 series flash memory card. This datasheet provides all AC and DC characteristics (including timing waveforms) and a convenient reference for the device command set and the card's integrated registers(including the Flash Memory's status registers). This datasheet provides description of the methods which are very helpful for customer to use the card.

2. Features

2.1 Type — Flash Memory Card

2.2 Overview

		ID246Pxx	ID246Rxx	ID246Sxx
Common Memory Capacity	Byte	32Mbyte	40Mbyte	48Mbyte
	Word	16Mword	20Mword	24Mword
Device		LH28F032SKD 8devices	LH28F032SKD 10devices	LH28F032SKD 12devices
Attribute Memory Capasity		2Kbyte (Note:standard CIS is not writable)		
Supply Voltage		Vcc=5V / Vpp=5V, Vcc=3.3V / Vpp=3.3V,5V		
Access time		150ns(@Vcc=5v) 250ns(@Vcc=3.3v)		
Erase Unit		64K word blocks		
Program/Erase Cycles		100,000cycles/Block		
External Dimensions		PCMCIA Type 1 54.0× 85.6× 3.3mm		

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2.3 Interface — Parallel I/O Interface

2.4 Function Table — See Function Table in page. 9

2.5 Pin Connections — See Pin Connections in page. 5

2.6 Type of Connector — Conforms to PCMCIA PC Card Standard 95 Card Use Connector

Card connector: JC20-J68S-NB3 by JAE or
FCN-568J068-G/0 by Fujitsu or
ICM-C68S-TS13-5035A by JST

2.7 Operating Temperature — 0 to 60°C

2.8 Storage Temperature — -20 to 65°C

2.9 Not designed for rated radiation hardened.

3. Block Diagram

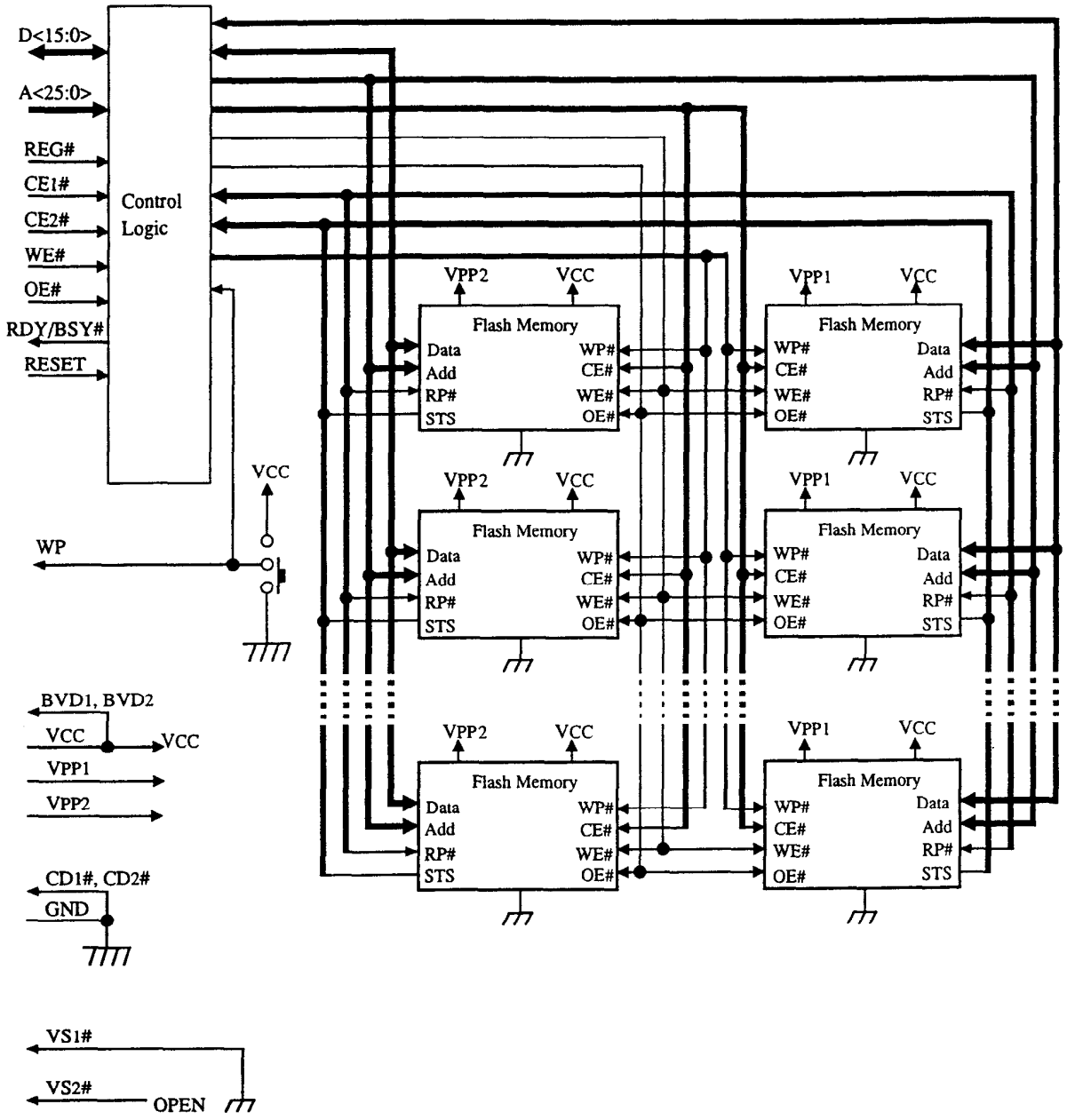

Figure 1. Block Diagram

4. Pin Connections

Table 1. Pin Connections

PIN No.	SIGNAL	I/O	FUNCTION	ACTIVE
1	GND		Ground	
2	D_3	I/O	Data Bit 3	
3	D_4	I/O	Data Bit 4	
4	D_5	I/O	Data Bit 5	
5	D_6	I/O	Data Bit 6	
6	D_7	I/O	Data Bit 7	
7	CE_1#	I	Card Enable 1	LOW
8	A_{10}	I	Address Bit 10	
9	OE#	I	Output Enable	LOW
10	A_{11}	I	Address Bit 11	
11	A_9	I	Address Bit 9	
12	A_8	I	Address Bit 8	
13	A_{13}	I	Address Bit 13	
14	A_{14}	I	Address Bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready Busy	LOW
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Program Voltage	
19	A_{16}	I	Address Bit 16	
20	A_{15}	I	Address Bit 15	
21	A_{12}	I	Address Bit 12	
22	A_7	I	Address Bit 7	
23	A_6	I	Address Bit 6	
24	A_5	I	Address Bit 5	
25	A_4	I	Address Bit 4	
26	A_3	I	Address Bit 3	
27	A_2	I	Address Bit 2	
28	A_1	I	Address Bit 1	
29	A_0	I	Address Bit 0	
30	D_0	I/O	Data Bit 0	
31	D_1	I/O	Data Bit 1	
32	D_2	I/O	Data Bit 2	
33	WP	O	Write Protect	HIGH
34	GND		Ground	

PIN No.	SIGNAL	I/O	FUNCTION	ACTIVE
35	GND		Ground	
36	CD_1#	O	Card Detect 1	LOW
37	D_{11}	I/O	Data Bit 11	
38	D_{12}	I/O	Data Bit 12	
39	D_{13}	I/O	Data Bit 13	
40	D_{14}	I/O	Data Bit 14	
41	D_{15}	I/O	Data Bit 15	
42	CE_2#	I	Card Enable 2	LOW
43	VS_1#	O	Voltage Sense 1	
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address Bit 17	
47	A_{18}	I	Address Bit 18	
48	A_{19}	I	Address Bit 19	
49	A_{20}	I	Address Bit 20	
50	A_{21}	I	Address Bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Program Voltage	
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	
57	VS_2#	O	Voltage Sense 2	
58	RESET	I	Reset	HIGH
59	RFU		Reserved	
60	RFU		Reserved	
61	REG#	I	Atribute Memory Select	LOW
62	BVD_2	O	Battery Voltage Detect 2	
63	BVD_1	O	Battery Voltage Detect 1	
64	D_8	I/O	Data Bit 8	
65	D_9	I/O	Data Bit 9	
66	D_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

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5. Signal Description

Table 2. Signal Description

Symbol	I/O	Electrical Interface	Function
A_0-A_{25}	I	Pull-down (250kΩ @Vcc=5v)	ADDRESS INPUTS: These are address bus lines which enable direct addressing of memory on the card. Signal A_0 is not used in word access mode.
D_0-D_{15}	I/O	Pull-down (250kΩ @Vcc=5v)	DATA INPUT/OUTPUT: D_0 through D_{15} constitute the bi-directional data bus. D_{15} is the most significant bit.
CE_1#,CE_2#	I	Pull-up (250kΩ @Vcc=5v)	CARD ENABLE 1 & 2: CE_1# enables D_0-D_7, CE_2# enables D_8-D_{15}.
OE#	I	Pull-up (250kΩ @Vcc=5v)	OUTPUT ENABLE: Active low signal gating read data from the memory card.
WE#	I	Pull-up (250kΩ @Vcc=5v)	WRITE ENABLE: Active low signal gating write data to the memory card.
RDY/BSY#	O		READY/BUSY OUTPUT: Indicates status of internally timed erase or write activities. ID246 series has two types of Ready/Busy output mode; PCMCIA mode and High-Performance mode. In PCMCIA mode, a high output indicates the memory card is ready to accept accesses. A low output indicates that a device in the memory card is busy. In High-Performance mode, the card outputs low when the card is in default state. A high output indicates at least one of flash memory devices in the card comes to be ready to accept accesses.
CD_1#, CD_2#	O	Pull-down 0Ω	CARD DETECT 1 & 2: These signals provide for card insertion detection. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	O	Low:Pull-down 0Ω High:Pull-up 100kΩ	WRITE PROTECT: Write Protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected.
Vpp1,Vpp2			WRITE / ERASE POWER SUPPLY 1 & 2:
Vcc			CARD POWER SUPPLY:
GND			GROUND:
REG#	I	Pull-up (250kΩ@Vcc=5v)	REGISTER SELECT: Provides access to attribute memory when REG# is low.
RESET	I	Pull-down (250kΩ@Vcc=5v)	RESET: Active high signal for placing card in Power-On Default State.
BVD_1, BVD_2	O	Pull-up 100kΩ	BATTERY VOLTAGE DETECT 1 & 2: These signals are pulled high to maintain SRAM card compatibility.
VS_1#, VS_2#	O	VS_1#: Pull-down VS_2#: N.C.	VOLTAGE SENSE 1 & 2: Notifies the host socket of the CIS's VCC requirements.VS_1# is pulled-down to ground when using the standard CIS, that indicate 3.3V operating is available.
RFU			RESERVED FOR FUTURE USE

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6. Functions

6. 1 Common Memory

6. 1. 1 Common Memory Architecture

Figure 2 shows common memory architecture of ID246 series flash memory card. Device pair is consisted of two pieces of flash memory devices. Each device has individually erasable and lockable blocks. All blocks are divided into odd bytes and even bytes.

Each device pair and block is selected by address bits. Table 3 shows definitions of address bits.

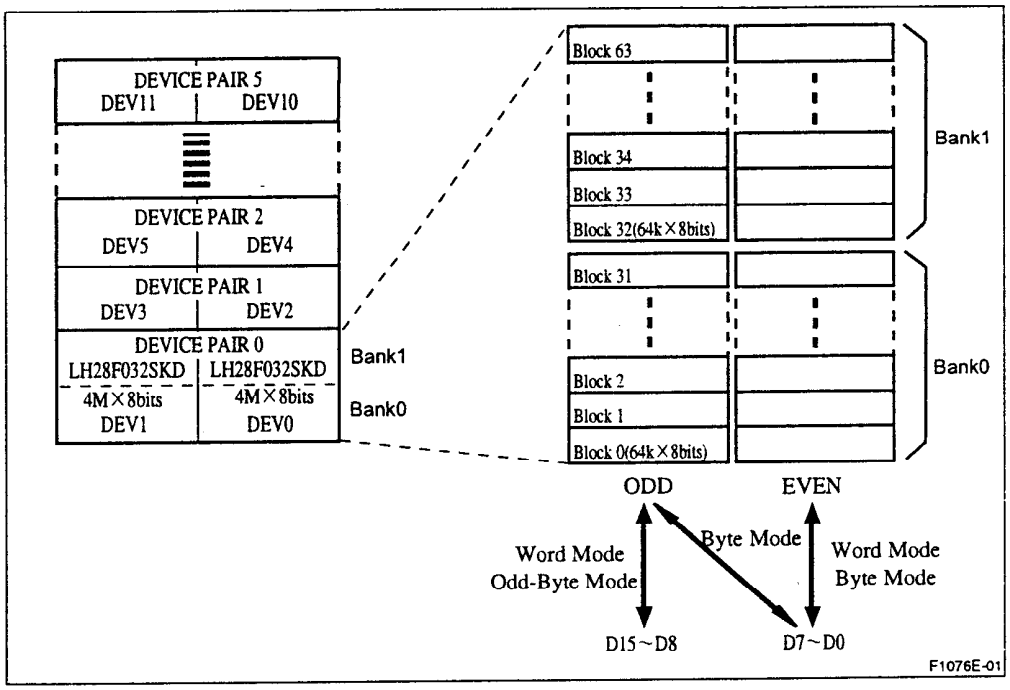

Figure 2. Common Memory Architecture

Table 3. Address Difinitions

Address Pifinitions	32MB , 40MB , 48MB
Select Even / Odd byte in the byte access mode.	A0
Select address in the block.	A16~A1 (64KB/Block)
Select a block.	A21~A17 (32blocks/bank)
Select a bank	A22 (2banks/device)
Select a device pair.	A25~A23

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6. 1. 2 Erase

Erase is executed one block at a time. Erasable block size is 64K bytes in byte access mode and 128K bytes in word access mode.

6. 1. 3 Address Decoding

The higher address area of ID246 series flash memory card which goes beyond common memory area is not decoded in common memory access. It means that the system will access to random memory address of the memory card even if system will try to access to the memory address which exceeds memory capacity of the card. Please do not access to the memory address which goes beyond memory capacity of the card.

As an enhanced function, the memory card enables to output invalid data (either of 0000h or FFFFh) when system will access to the memory address which exceeds memory capacity of the card. Please contact our sales & marketing support to find concrete way of setting.

6. 2 Attribute Memory

Figure 3 shows attribute memory map of ID246 series flash memory card. Attribute memory is contained within the Card Control Logic. Attribute memory contains the Card Information Structure (CIS) and Component Management Registers (CMRs). The CIS contains tuple information and is located at even byte addresses beginning with address 0000h (Please refer to section 7). The standard CIS of ID246 series flash memory card is hardwired and is for read only. As an enhanced function, the hardwired CIS area is switchable to EEPROM so that customer can program required CIS. Please contact our sales & marketing support to find concrete way of setting. The CMRs are located at even byte addresses beginning with address 4000h (Please refer to section 9).

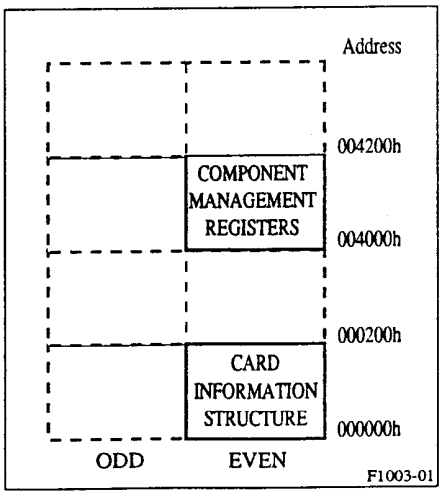

Figure 3. Attribute Memory Map

6.3 Function Table

6.3.1 Common Memory Access

Table 4. Common Memory Access

Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	D_{15-8}	D_{7-0}
Stand-by	X	H	H	X	X	X	High-Z	High-Z
Byte Read	H	H	L	L	L	H	High-Z	Even
	H	H	L	H	L	H	High-Z	Odd
Word Read	H	L	L	X	L	H	Odd	Even
Odd Byte Read	H	L	H	X	L	H	Odd	High-Z
Byte Write	H	H	L	L	H	L	Don't care	Even
	H	H	L	H	H	L	Don't care	Odd
Word Write	H	L	L	X	H	L	Odd	Even
Odd Byte write	H	L	H	X	H	L	Odd	Don't care

6.3.2 Attribute Memory Access

Table 5. Attribute Memory Access

Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	D_{15-8}	D_{7-0}
Stand-by	X	H	H	X	X	X	High-Z	High-Z
Byte Read	L	H	L	L	L	H	High-Z	Even
	L	H	L	H	L	H	High-Z	XX
Word Read	L	L	L	X	L	H	XX	Even
Odd Byte Read	L	L	H	X	L	H	XX	High-Z
Byte Write	L	H	L	L	H	L	Don't care	Even
	L	H	L	H	H	L	Don't care	Don't care
Word Write	L	L	L	X	H	L	Don't care	Even
Odd Byte write	L	L	H	X	H	L	Don't care	Don't care

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XX:Output data is invalid.

The standard CIS is for read only. Write operation is only for CMRs and CIS on EEPROM

7. Card Information Structure (CIS)

The CIS is contained within attribute memory (Please refer to section 6.2). Table 6 shows standard CIS tuples, but it is for read only. As an enhanced function, the hardwired CIS area is switchable to EEPROM so that customer can program required CIS. Please contact our sales & marketing support to find concrete way of setting.

Table 6. Standard CIS

Address	Value	Description
00h	01h	Device Info (Common Memory)
02h	04h	Tuple Link
04h	57h	Flash Memory
06h	22h	Access Time 150ns
08h	7Eh 9Eh BEh	Capacity 32MB 40MB 48MB
0Ah	FFh	End of Tuple
0Ch	1Ch	Device Info (Common Memory Other Conditions)
0Eh	05h	Tuple Link
10h	02h	Conditions 3Vcc
12h	57h	Flash Memory
14h	32h	Access Time 250ns
16h	7Eh 9Eh BEh	Capacity 32MB 40MB 48MB
18h	FFh	End of Tuple
1Ah	17h	Device Info ID (Attribute Memory)
1Ch	04h	Tuple Link
1Eh	1Fh	ROM
20h	2Ah	Access Time 200ns
22h	01h	Capacity 2KB
24h	FFh	End of Tuple
26h	1Dh	Device Info ID (Attribute Memory)
28h	05h	Tuple Link
2Ah	02h	Conditions 3Vcc
2Ch	1Fh	ROM
2Eh	2Ah	Access Time 200ns
30h	01h	Capacity 2KB
32h	FFh	End of Tuple
34h	18h	JEDEC Code ID
36h	02h	Tuple Link
38h	B0h	Manufacture Code
3Ah	D0h	Device Code
3Ch	00h	End of Tuple
3Eh	15h	Version Info Level 1
40h	23h	Tuple Link
42h	04h	Major Version
44h	01h	Minor Version

Address	Value	Description
46h	53h	S:Product Info
48h	48h	H
4Ah	41h	A
4Ch	52h	R
4Eh	50h	P
50h	00h	END TEXT
52h	49h	I
54h	44h	D
56h	32h	2
58h	34h	4
5Ah	53h	S
5Ch	52h	R
5Eh	20h	SPACE
60h	00h	END TEXT
62h	53h	S :Maker Info
64h	48h	H
66h	41h	A
68h	52h	R
6Ah	50h	P
6Ch	20h	SPACE
6Eh	43h	C
70h	4Fh	O
72h	52h	R
74h	50h	P
76h	4Fh	O
78h	52h	R
7Ah	41h	A
7Ch	54h	T
7Eh	49h	I
80h	4Fh	O
82h	4Eh	N
84h	00h	END TEXT
86h	FFh	End of Tuple
88h	1Ah	Configuration Info
8Ah	05h	Tuple Link
8Ch	01h	2 Bytes Field
8Eh	02h	Last Index of Configuration Table
90h	00h	CMRs Base Adress(LSB)
92h	40h	CMRs Base Adress(MSB)
94h	0Bh	CMR Mask
96h	00h	Null
98h	1Bh	Configuration Table Entry 1

Table 8. Standard CIS (Continued)

Address	Value	Description
9Ah	08h	Tiple Link
9Ch	01h	Index
9Eh	02h	Vcc & Vpp
A0h	79h	Parameter Selection
A2h	55h	Vcc Voltage 5V
A4h	0Ch	Icc Static
A6h	06h	Icc Average
A8h	06h	Icc Peak
AAh	23h	Icc Powerdown
ACh	1Bh	Configuration Table Entry 2
AEh	09h	Tuple Link
B0h	02h	Index
B2h	01h	Vcc Onry
B4h	79h	Parameter Selection
B6h	B5h	Vcc Voltage 5V
B8h	1Eh	
BAh	0Ch	Icc Static
BCh	7Dh	Icc Average
BEh	7Dh	Icc Peark
C0h	1Bh	Icc Powerdown
C2h	1Eh	Device Geometry
C4h	06h	Tuple Link
C6h	02h	Bus
C8h	11h	Erase
CAh	01h	Read size
CCh	01h	Write size
CEh	01h	Partation: 1block
D0h	01h	Non-interleaved
D2h	20h	Manufacturer ID
D4h	04h	Tuple Link
D6h	B0h	Manufacturer Code
D8h	00h	
DAh	0Fh 11h 12h	Manufacturer Info: 32MB 40MB 48MB
DCh	31h	Manufacturer Info: DVO
DEh	21h	Function Identification
E0h	02h	Tuple Link
E2h	01h	Function: MEMORY
E4h	00h	System: None
E6h	FFh	End of CIS

8. Card Control

8. 1 Reset

The card is in initial state directly after power-up. But we recommend to do reset operation after power-up to make sure to initialize the card.

During block erase, byte write, or lock-bit configuration modes, an active RESET will abort the operation. RDY/BSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET goes to logic-Low (V_{IL}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET to the card during a system reset. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs.

For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data. Sharp's ID246 Series Flash Memory Card allows proper card reset following a system reset through the use of the RESET input.

8. 2 Status Register

Each flash memory device in the card has status register. The status register may be read to determine when a write, block erase, or lock-bits configuration is complete, and whether that operation completed successfully (please refer to Table 7). It may be read at any time by writing the Read Status Register command (70h, 7070h) into the CUI. In word access mode, the status register data of even byte devices are output to D7~0,and the status register data of odd byte devices are output to D15~8.

8. 3 Write Protect Switch

The ID246 Series Flash Memory Card has a write protect switch on the back of the card. When the switch is in the write protect position, the card blocks all writes to the common and attribute memory without Card Management Registers region (see Figure 4).

8. 4 Read Identifier Codes / Block Status Code

Manufacture Code and Device Code are contained within each flash memory device in the memory card. The identifier code operation is initiated by writing the Read Identifier Codes command (90h, 9090h) into the CUI of each memory device. The specific address of each device is necessary to be selected to read these codes (Table 9).

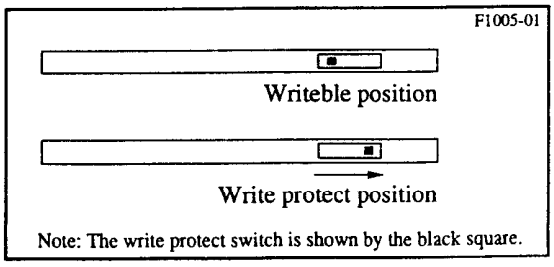

Figure 4. Write Protect Switch

Table 7(a). Status Register Definition

WSMS	BESS	ECBLBS	WSBLBS	VPPS	WSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS
1 = Error in Erase or Clear Block Lock-Bits
0 = Successful Erase or Clear Block Lock-Bit

SR.4 = WRITE AND SET BLOCK LOCK-BIT STATUS
1 = Error in Write or Set Block Lock-Bit
0 = Successful Write or Set Block Lock-Bit

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2 = WRITE SUSPEND STATUS
1 = Write Suspended
0 = Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Block Lock-Bit and/or WP# Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

Check RY/BY# pin or SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion.
SR.6-0 are invalid while SR.7="0"

If both SR.5 and SR.4 are "1"safter a block erase, full chip erase,(multi) word/bite write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered.

SR.3 docs not provide a continuous indication of V_{PP} level. the WSM interrogates and indicates the V_{PP} level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when V_{PP}/=V_{PPH1}.

SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates block lock-bit, and WP# only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. Itinforms the system, depending on the attempted operation, If the block lock-bit is set and/or WP# is not V_{IH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.

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Table 7(b). Extended Status Register Definition

SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.7 = STATE MACHINE STATUS
1 = Multi Word/byte Write available
0 = Multi Word/byte Write not available

XSR.6-0=RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

After issue a Multi Word/Byte Write command: XSR.7 indicates that a next Multi Word/Byte Write command is available.

XSR.6-0 is reserved for future use and should be masked out when polling the extended status register.

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Table 8. Identifier Codes / Block Status

	Select Device-pair A_{25}-A_{21}	Address in Device A_{20}-A_1	Even/Odd A_0	Data Output D_7-D_0
				32MB , 40MB , 48MB
Manufacture Identifier Code	DPA	00000h 00001h	0:Even 1:Odd	B0h
Device Identifier Code	DPA	00002h 00003h	0:Even 1:Odd	D0h
Block Status Code	DPA	X0004h X0005h (X: Select Block)	0:Even 1:Odd	Block Status Code D_0: 0=Unlocked, 1=Locked D_1: 0=Last Erase operation completed successfully 1=Last Erase operation did not completed successfully D_7-D_2: Reserved

NOTE: A_0 is ignored in word access mode, and D_{15}-D_8 outputs the Odd byte data.

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DPA: Address as select device pair
BLKD: Block Lock Configuration Data
MLKD: Master Lock Configuration Data

9. Component Management Registers (CMR)

Component Management Registers (CMR) are mapped at even byte locations beginning at address 4000h in attribute memory.

9. 1 Configuration Option Register (Address:4000h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4000h	SRESET	Reserved						

SRESET: 1=Reset State 0=End Reset Cycle

9. 2 Card Configuration Register (Address:4002h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4002h	Reserved					PWDN	Reserved	

PWDN: 1=Power-Down
Device pairs that apointed by Sleep Control Register(4118h-411Ah) are in Power-Down.
0=Power-Up

9. 3 Socket and Copy Register (Address:4006h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4006h	Reserved	Copy No.			Soket No.			

Soket No.: Socket Number
Copy No.: Copy Number
The card may use to distinguish between similar cards installed in a system.

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9. 4 Card Status Register (Address:4100h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4100h	ADM	ADS	SRESET	CMWP	PWDN	CISWP	WP	RDY/BSY

ADM: ORed value of the Ready/Busy Mask Register.
1 = Any device is masked. 0 = All Devices are not Masked.
ADS: ORed value of the Sleep Control Register.
1 = Any device-pair is Controled power-down by bit.2 of the Card Configuration Register.
SRESET: Reflects the bit.7 of the Configuration Option Register.
CMWP: Reflects the bit.1 of the Write Protection Register.
PWDN: Reflects the bit.2 of the Card Configuration Register.
CISWP: Reflects the bit.0 of the Write Protection Register.
WP: Indicates the Write Protect Switch status.
1 = Write Protect Switch: ON 1 = Write Protect Switch: OFF
RDY/BSY: Reflects the Ready/Busy Status Register.
1 = All devices are READY. 0 = Any device is BUSY.

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9. 5 Write Protection Register (Address:4104h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4104h	Reserved					BLKEN	CMWP	CISWP

BLKEN: Block Locking Enable
1 = Enable Block Locking 0 = All Block Unlocked
Common Memory Write Protect
CMWP: 1 = Common Memory without CIS region in Write Protect Status
Common Memory CIS Write Protect
CISWP: 1 = Common Memory CIS in Write Protect Status

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9. 6 Sleep Control Register (Address:4118h~411Ah)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
411Ah	Reserved							
4118h	Reserved		DEV10/11	DEV8/9	DEV6/7	DEV4/5	DEV2/3	DEV0/1

1= Select sleep mode device-pair
If set to "1", the corresponding device-pairs are putted into deep power-down mode by PWDN bit of Configuration Status Register.

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9. 7 Ready/Busy Mask Register (Address:4120h~4122h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4122h	Reserved				DEV11	DEV10	DEV9	DEV8
4120h	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0

1 =Mask the Rdy/Bsy#
The corresponding device's Rdy/Bsy# signals to set bit are ignored for card's RDY/BSY# output.

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9. 8 Ready/Busy Status Register (Address:4130h~4132h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4132h	Reserved				DEV11	DEV10	DEV9	DEV8
4130h	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0

1=READY 0=BUSY
Each bit indicates the corresponding device's Rdy/Bsy# signal.

T1041-01

9. 9 Ready/Busy Mode Register (Address:4140h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4140h	Reserved						RACK	MODE

RACK: Ready Acknowledge Bit
Must clear this bit after receiving ready status to prepare for next device's ready transition.
MODE: RDY/BSY# Mode
1 = High-Performance Mode 0 = PCMCIA Mode

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10. Command Definitions

Device operations are determined by writing specific commands to the Command User Interface. Table 9 defines the commands.

Table 9. Command Definitions

Command	Note	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array / Reset		Write	DA	FFh (FFFFh)	-	-	-
Read Identifier Codes	1	Write	DA	90h (9090h)	Read	IA	ID
Query		Write	DA	98h (9898h)	Read	QA	QD
Read Status Register	2	Write	DA	70h (7070h)	Read	DA	SRD
Clear Status Register		Write	DA	50h (5050h)	-	-	-
Full Chip Erase Setup/Confirm		Write	DA	30h (3030h)	Write	DA	D0H
Word/Byte Write	3	Write	WA	40h (4040h) or 10h (1010h)	Write	WA	WD
Multi Word/Byte Write Setup/Confirm	4	Write	WA	E8h (E8E8h)	Write	WA	N-1
Block Erase	3	Write	BA	20h (2020h)	Write	BA	D0h (D0D0h)
Block Erase and Word/Byte Write Suspend	3	Write	DA	B0h (B0B0h)	-	-	-
Block Erase and Word/Byte Write Resume	3	Write	DA	D0h (D0D0h)	-	-	-
Set Block Lock-Bit		Write	BA	60h (6060h)	Write	BA	01h (0101h)
Clear Block Lock-Bit		Write	DA	60h (6060h)	Write	DA	D0h (D0D0h)
STS Configuration Level-Mode for Erase and Write (RY/BY# Mode)		Write	DA	B8h (B8B8h)	Write	DA	00h (0000h)
STS Configuration Pulse-Mode for Erase		Write	DA	B8h (B8B8h)	Write	DA	01h (0101h)
STS Configuration Pulse-Mode for Write		Write	DA	B8h (B8B8h)	Write	DA	02h (0202h)
STS Configuration Pulse-Mode for Erase and Write		Write	DA	B8h (B8B8h)	Write	DA	03h (0303h)

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Address		Data	
IA	=Identifier code Address	ID	=Identifier Codes
WA	=Write Address	WD	=Write Data
BA	=Block Address	SRD	=Data from Status Register
DA	=Device Address	QA	=Query Offset Address
QD	=Data read from Query database		

Note:

1. Following the Read Identifier Codes command, read operations access manufacture, device, block status codes.
2. Status Register may be read to determine when a write, block erase, or lock bit configuration is complete, and whether that operation completed successfully.
3. If the block is locked, block erase or write operations are desabled.
4. Following the Third Bus Cycle,inputs the write address and write data of 'N'+1 times.Finally, input the confirm command 'D0H'.

10. 1 Query Command

Query database can be read by writing Query command (98H). Following the command write, read cycle from address shown in Table 11-15 retrievethe critical information to write, erase and otherwise control the flash component.

In word mode, D_8-D_{15} output the Query data of odd Byte Devices.

Table 10. Example of Query Structure Output

Mode	Offset Address		Output	
	(A6 - A1)	A_0	D_{15}-D_8	D_7-D_0
X8 mode	A_6, A_5, A_4, A_3, A_2, A_1 1 , 0 , 0 , 0 , 0 , 0 (20H) 1 , 0 , 0 , 0 , 0 , 1 (21H) 1 , 0 , 0 , 0 , 1 , 0 (22H) 1 , 0 , 0 , 0 , 1 , 1 (23H)	0 = Even 1 = Odd	High-Z High-Z High-Z High-Z	"Q" "Q" "R" "R"
X16 mode	A_6, A_5, A_4, A_3, A_2 1 , 0 , 0 , 0 , 0 (10H) 1 , 0 , 0 , 0 , 1 (11H)	X	"Q" "R"	"Q" "R"

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10. 1. 1 Block Status Register

This field provides lock configuration and erase status for the specified block. These informations are only available when device is ready (SR.7=1). If block erase or full chip erase operation is finished irregulary, block erase status bit will be set to "1",this block is invalid.

Table 11. Query Block Status Register

Offset (Word Address)	Length	Description
(BA+2)H	01H	Block Status Register D0 : Block Lock Configuration 0=Block is unlocked 1=Block is locked D1 : Block Erase Status 0=Last erase operation completed successfully 1=Last erase operation not completed successfully D2-7: Reserved for future use

NOTE: 1.BA=The beginning of a Block Address.

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10. 1. 2 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, If indicates which version of the spec and which Vendor-specified command set(s) is(are) supported.

Table 12. CFI Query Identification String

Offset (Word Address)	Length	Description
10H,11H,12H	03H	Query Unique ASCII string "QRY" 51H,52H,59H
13H,14H	02H	Primary Vendor Command Set and Control Interfase ID Code 01H,00H (SCS ID Code)
15H,16H	02H	Addressfor Primary Algorithm Extended Query Table 31H,00H (SCS Extended Query Table Offset)
17H,18H	02H	Alternate Vendor Command Set and Control Interfase ID Code 0000H (0000H means that no alternate exists)
19H,1AH	02H	Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists)

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10. 1. 3 System Interface Information

The following device information can be useful in optimizing system interface software.

Table 13. System Information String

Offset (Word Address)	Length	Description
1BH	01H	V_{CC} Logic Supply Minimum Write/Erase voltage 27H (2.7V)
1CH	01H	V_{CC} Logic Supply Maximum Write/Erase voltage 55H (5.5V)
1DH	01H	V_{PP} Programming Supply Minimum Write/Erase voltage 27H (2.7V)
1EH	01H	V_{PP} Programming Supply Maximum Write/Erase voltage 55H (5.5V)
1FH	01H	Typical Timeout per Single Byte/Word Write 03H (2^3=8 usec)
20H	01H	Typical Timeout for Maximum Size Buffer Write (32 Bytes) 03H (2^6=64 usec)
21H	01H	Typical Timeout per Individual Block Erase 0AH (0AH=10 , 2^{10}=1024 msec)
22H	01H	Typical Timeout for Full Chip Erase 0FH (0FH=15 , 2^{15}=32768 msec)
23H	01H	Maximum Timeout per Single Byte/Word Write, 2^N times of typical 04H (2^4=16 , 8 usec x16=128 usec)
24H	01H	Maximum Timeout Maximum Size Buffer Write, 2^N times of typical 04H (2^4=16 , 64 usec x16=1024 usec)
25H	01H	Maximum Timeout per Individual Block Erase, 2^N times of typical 04H (2^4=16 , 1024 msec x16=16384 msec)
26H	01H	Maximum Timeout for Full Chip Erase, 2^N times of typical 04H (2^4=16 , 32768 msec x16=524288 msec)

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10. 1. 4 Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 14. Device Geometry Definition

Offset (Word Address)	Length	Description
27H	01H	Device Size 15H (15H=21, 2^{21}=2097152=2M Bytes
28H, 29H	02H	Flash Device Interface description 02H,00H (x8/x16 supports x8 and x16 via BYTE#)
2AH, 2BH	02H	Maximum Number of Bytes in Multi word/byte write 05H,00H (2^5=32 Bytes)
2CH	01H	Number of Erase Block Regions within device 01H (symmetrically blocked)
2DH, 2EH	02H	The Number of Erase Blocks 1FH,00H (1FH=31 ==>31+1=32 Blocks
2FH, 30H	02H	The Number of "256 Bytes" cluster in a Erase block 00H,01H (0100H=256 ==>256 Bytes x 256=64K Bytes in a Erase Block)

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10. 1. 5 SCS OEM Specific Extended Query Table

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific Query table(s) may be used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

Table 15. SCS OEM Specific Extended Query Table

Offset (Word Address)	Length	Description
31H,32H,33H	03H	PRI 50H, 52H, 49H
34H	01H	31H (1) Major Version Number , ASCII
35H	01H	30H (0) Minor Version Number, ASCII
36H. 37H. 38H. 39H	04H	0FH, 00H, 00H, 00H Optional Command support bit0=1 : Chip Erase Supported bit1=1 : Suspend Erase Supported bit2=1 : Suspend Write Supported bit3=1 : Lock/Unlock Supported bit4=0 : Queued Erase Not Supported bit5-31=0 : reserved for future use
3AH	01H	01H Supported Functions after Suspend bit0=1 : Write Supported after Erase Suspend bit1-7=0 : reserved for future use
3BH, 3CH	02H	03H, 00H Block Status Register Mask bit0=1 : Block Status Register Lock Bit [BSR.0] active bit1=1 : Block Status Register Valid Bit [BSR.1] active bit2-15=0 : reserved for future use
3DH	01H	V_{CC} Logic Supply Optimum Write/Erase voltage (highest performance) 50H (5.0V)
3EH	01H	V_{PP} Programming Supply Optimum Write/Erase voltage (highest performance) 50H (5.0V)
3FH	reserved	Reserved for future versions of the SCS Specification

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10. 2 STS Configuration Command

The RDY/BSY# pin can be configured to different states using the STS Configuration command. Once the RDY/BSY# pin has been configured, it remains in that configuration until another configuration command is issued, the device is powered down or card is reset. Upon initial power-up and after exit from deep power-down mode, the RDY/BSY# pin defaults to RY/BY# operation where STS low indicates that the WSM is busy. STS high indicates that the WSM is ready for a new operation.

To reconfigure the RDY/BSY# pin to other modes, the STS Configuration is issued followed by the appropriate configuration code. The three alternate configurations are all pulse mode for use as a system interrupt.

Table 16. STS Configuration Coding Description

Configuration Bits	Effects
00H	Set STS pin to default level mode (RY/BY#). RY/BY# in the default level-mode of operation will indicate WSM status condifion.
01H	Set STS pin to plused output signal for specific erase operation. In this mode, STS provides low pulse at the completion of Block Erase,Full Chip Erase and Clear Block Lock-bit operation.
02H	Set STS pin to pulsed output signal for a specific write operation. In this mode, STS provides low pulse at the completion of (multi) Byte Write and Set Block Lock-bit operation.
03H	Set STS pin to pulsed output signal for specific write and erase operation.STS provides low pulse at the completion of Block Erase, Full Chip Erase, (Multi) Word/Byte Configuration operations.

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Table 17. Write Protection Alternatives

Operation	Block Lock-Bit	BLKEN bit of Write Protection Register	Effect
Block Erase, (Multi) Word/Byte Write	0	X	Block Erase and (Multi) Word/Byte Write Enabled.
	1	1	Block is Locked. Block Erase and (Multi) Word/Byte Write Disabled.
		0	Block Lock-Bit Override. Block Erase and (Multi) Word/Byte Write Enabled.
Full Chip Erase	0,1	1	All unlocked blocks are erased, lockd blocks are not erased.
	X	0	All Block Lock-Bit Disabled.
Set Block Lock-Bit	X	1	Set Block Lock-Bit Disabled.
		0	Set Block Lock-Bit Enabled.
Clear Block Lock-Bits	X	1	Clear Block Lock-Bit Disabled.
		0	Clear Block Lock-Bit Enabled.

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11. Electrical Specifications

11. 1 Absolute Maximum Ratings

PARAMETER	NOTE	SYMBOL	RATING	UNIT
Supply Voltage	2	V_{CC}	-0.3 to 6.0	V
Program Voltage	2	V_{PP}	-0.2 to 7.0	V
Input Voltage	2	V_{IN}	-0.3 to Vcc+0.3(Max:6.0)	V
Operating Temperature	1	T_{OPR}	0 to 60	℃
Storage Temperature		T_{STG}	-20 to 65	℃

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NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. During transitions, this level may undershoot to -2.0v for periods <20ns or overshoot to Vcc+2.0v for periods <20ns.

11. 2 Recommended Operating Conditions

PARAMETER	NOTE	SYMBOL	MIN	MAX	UNIT
Supply Voltage		V_{CC1}	3.0	3.6	V
		V_{CC2}	4.75	5.25	V
		V_{CC3}	4.5	5.5	V
Program Voltage		V_{PP1}	3.0	3.6	V
		V_{PP2}	4.5	5.5	V
Operating Temperature		T_{OPR}	0	60	℃

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11. 3 Capacitance

Ta=25℃, f=1MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	-	15	-	pF	V_{IN}=0.0V
Input/Output Capacitance	C_{IO}	-	25	-	pF	V_{OUT}=0.0V

11. 4 AC Input/Output Test Conditions

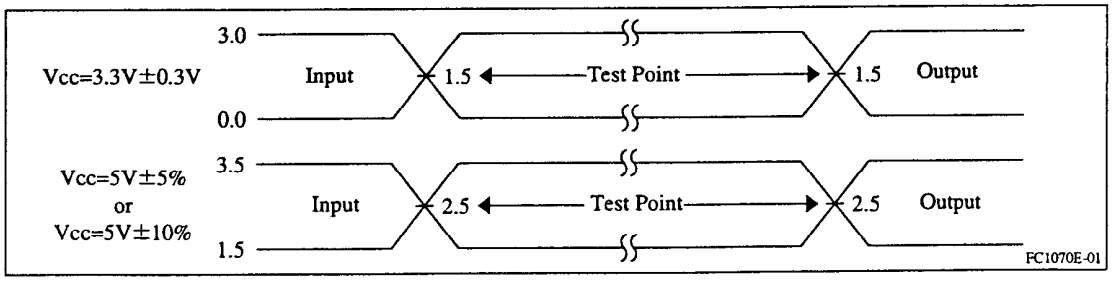

Figure 5. Transient Input/Output Reference Waveform

Figure 5 shows Input/Output level and test level for AC test. Input rise and fall times (10% to 90%) < 10ns.

12. DC Characteristics

(Ta = 0 to 60℃)

PARAMETER	SYM-BOL	NO-TE	Densi-ty	Vcc=3.3V ±0.3V		Vcc=5V ±5% Vcc=5V ±10%		UNIT	TEST CONDITION
				MIN	MAX	MIN	MAX		
Input Low Voltage	V_{IL}	1			0.3Vcc		1.5	V	
Input High Voltage	V_{IH}	1		0.7Vcc		3.5		V	
Input Low Current	$-I_{IL1}$	2			± 2.0		± 2.0	μA	V_I = 0V
	$-I_{IL2}$	3		2.0	30.0	8.0	60.0	μA	V_I = 0V
Input High Current	I_{IH1}	3			± 2.0		± 2.0	μA	V_I = Vcc
	I_{IH2}	2		2.0	30.0	8.0	60.0	μA	V_I = Vcc
Output Low Voltage	V_{OL1}	4,5			-		0.4	V	I_{OL} = 6mA
					0.4		-	V	I_{OL} = 3mA
Output High Voltage	V_{OH1}	4		-		4.0		V	I_{OH} = -3mA
				Vcc-0.5		-		V	I_{OH} = -1.5mA
	V_{OH2}	5		-		4.0		V	I_{OH} = -6mA
				Vcc-0.5		-		V	I_{OH} = -3mA
Vcc Stand-by Current	I_{CCS}	6	32MB		821		845	μA	CE_1#,CE_2#=Vcc A_0~A_{25}=GND I_{OUT}=0mA
			40MB		1025		1045	μA	
			48MB		1225		1245	μA	
Vcc Deep Power-Down Current	I_{CCD}	6	32MB		141		162	μA	RESET=Vcc CE_1#,CE_2#=Vcc A_0~A_{25}=GND I_{OUT}=0mA
			40MB		171		192	μA	
			48MB		201		222	μA	
Vcc Read Current	I_{CCR}	6			65		129	mA	CE_1#,CE_2#=GND I_{OUT}=0mA
Vcc Word Write or Set Lock-Bit Current	I_{CCW}	6,8			35.1		-	mA	V_{PP}=3.3V ± 0.3V
					35.1		71.1	mA	V_{PP}=5.0V ± 10%
Vcc Block Erase or Clear Lock-Bit Current	I_{CCE}	6,8			35.1		-	mA	V_{PP}=3.3V ± 0.3V
					35.1		61.1	mA	V_{PP}=5.0V ± 10%
VccWord Write or Block Erase Suspend Current	I_{CCWS} I_{CCES}	6			13.1		21.1	mA	
Vcc Lockout Voltage	V_{LKO}			2.0		2.0		V	

(Continue to next page)

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DC Characteristics (Continued) (Ta = 0 to 60℃)

PARAMETER	SYM-BOL	NO-TE	Densi-ty	Vcc=3.3V±0.3V		Vcc=5V±5% Vcc=5V±10%		UNIT	TEST CONDITION
				MIN	MAX	MIN	MAX		
V_{PP} Stand-by or Read Current	I_{PPS} I_{PPR}	6	32MB		± 120		± 120	μA	$V_{PP} \leqq Vcc$
			40MB		± 150		± 150	μA	
			48MB		± 180		± 180	μA	
			32MB		1.6		-	mA	$V_{PP}>Vcc$
			40MB		2.0		-	mA	
			48MB		2.4		-	mA	
V_{PP} Deep Power-Down Current	I_{PPD}	6	32MB		40		40	μA	
			40MB		50		50	μA	
			48MB		60		60	μA	
V_{PP} Word Write or Set Lock-Bit Current	I_{PPW}	6,8			160.2		-	mA	V_{PP}=3.3V±0.3V
					160.0		160.2	mA	V_{PP}=5.0V±10%
V_{PP} Block Erase or Clear Lock-Bit Current	I_{PPE}	6,8			80.2		-	mA	V_{PP}=3.3V±0.3V
					80.0		80.2	mA	V_{PP}=5.0V±10%
V_{PP} Word Write or Block Erase Suspend Current	I_{PPWS} I_{PPES}	6	32MB		490		490	μA	$V_{PP} \leqq Vcc$
			40MB		520		520	μA	
			48MB		550		550	μA	
			32MB		1.6		-	mA	$V_{PP}>Vcc$
			40MB		2.0		-	mA	
			48MB		2.4		-	mA	
V_{PP} Lockout Voltage	V_{PPLK}	7,8			1.5		1.5	V	

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NOTE:

1. These parameters are applied to all input pins and all input/output pins in input mode.
2. These parameters are applied to A_0~A_{25} and D_0~D_{15} in input mode and RESET.
3. These parameters are applied to CE_1#,CE_2#,WE#,OE# and REG#.
4. These parameters are applied to RDY/BSY#.
5. These parameters are applied to D_0~D_{15} in output mode.
6. All currents are in RMS unless otherwise notes.
7. Block erase, word/byte write, and lock-bit configurations are inhibited when $V_{PP} \leqq V_{PPLK}$, and guaranteed in the V_{PP} Voltage is V_{PP1}, or V_{PP2}.
8. Sampled.

13. AC Characteristics

Testing Conditions :

1) Input Pulse Level : 1.5 to 3.5V (@Vcc=5V±5%,Vcc=5V±10%)
   0 to 3.0V (@Vcc=3.3±0.3V)
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 2.5V (@Vcc=5V±5%,Vcc=5V±10%)
   1.5V (@Vcc=3.3V±0.3V)
4) Output Load : 1TTL+100pF (@Vcc=5V±5%,Vcc=5V±10%)
   (including scope and jig capacitance) 1TTL+50pF (@Vcc=3.3V±0.3V)

13. 1 Common Memory Read Operations

(Ta = 0 to 60℃)

PARAMETER	SYMBOL		Vcc=3.3V± 0.3V		Vcc=5V± 5%		Vcc=5V± 10%		Unit
	IEEE	PCMCIA	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{AVAV}	t_{cR}	250	-	150	-	160	-	ns
Address Access Time	t_{AVQV}	t_a(A)	-	250	-	150	-	160	
CE# Access Time	t_{ELQV}	t_a(CE)	-	250	-	150	-	160	
OE# Access Time	t_{GLQV}	t_a(OE)	-	125	-	75	-	80	
Output Disable Time from CE1#,CE2# *	t_{EHQZ}	t_{dis}(CE)	-	100	-	75	-	80	
Output Disable Time from OE# *	t_{GHQZ}	t_{dis}(OE)	-	100	-	75	-	80	
Output Enable Time from CE1#,CE2#	t_{ELQNZ}	t_{en}(CE)	5	-	5	-	5	-	
Output Enable Time from OE#	t_{GLQNZ}	t_{en}(OE)	5	-	5	-	5	-	
Data Valid Time from Address Change		t_v(A)	0	-	0	-	0	-	

*:Time until output becomes floating. (The output voltage is not defined.)

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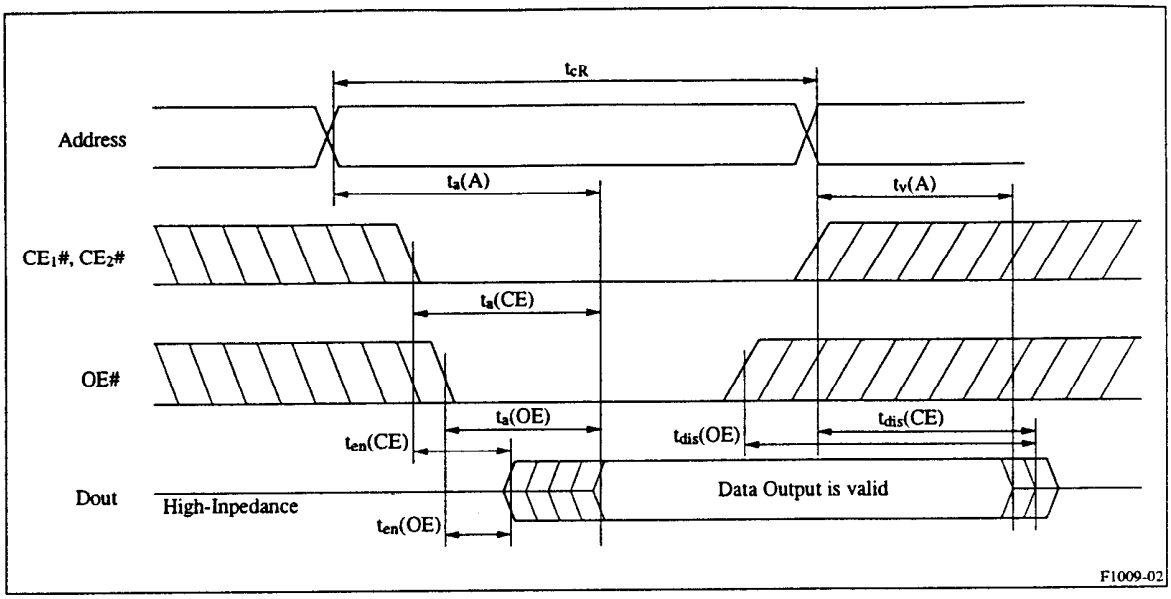


Figure 6. AC Waveforms for Read Operations

Note) 1. WE# = "HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, ta (A), ta (CE) or ta (OE) have concluded.

13. 2 Command Write Operations : Common Memory

13. 2. 1 WE# Controlled Write Operations

(Vcc=3.3V±0.3V, Ta=0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=3.3V±0.3V		Unit
	IEEE	PCMCIA		MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		250	-	ns
Address Setup Time	t_{AVWL}	t_{su}(A)		30	-	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)		30	-	ns
Data Setup Time for WE#	t_{DVWH}	t_{su}(D-WEH)		80	-	ns
Data Hold Time	t_{WHDX}	t_{h}(D)		30	-	ns
OE# Hold Time from WE#	t_{WHGL}	t_{h}(OE-WE)		120	-	ns
CE# Setup Time for WE#	t_{ELWH}	t_{su}(CE-WEH)		180	-	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)		180	-	ns
Write Pulse Width	t_{WLWH}	t_{w}(WE)		150	-	ns
WE# High to RDY/BSY# going Low	t_{WHRL}			-	140	ns
RESET Recovery Time	t_{PHWL}			1	-	μs
V_{PP} Setup Time	t_{VPWH}			180	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	ns
Word/Byte Write Time	t_{WHQV1}		V_{PP}=3.3V±0.3V	-	250	μs
			V_{PP}=5V±10%	-	180	μs
Block Erase Time	t_{WHQV2}		V_{PP}=3.3V±0.3V	-	16.5	s
			V_{PP}=5V±10%	-	10.9	s
Set Lock-Bit Time	t_{WHQV3}		V_{PP}=3.3V±0.3V	-	250	μs
			V_{PP}=5V±10%	-	180	μs
Clear Block Lock-Bits Time	t_{WHQV4}		V_{PP}=3.3V±0.3%	-	10.0	s
			V_{PP}=5V±10%	-	10.0	s
Word/Byte Suspend Latency Time to Read	t_{WHRH1}		V_{PP}=3.3V±0.3%	-	10.0	μs
			V_{PP}=5V±10%	-	9.3	μs
Erase Suspend Latency Time to Read	t_{WHRH2}		V_{PP}=3.3V±0.3%	-	21.1	μs
			V_{PP}=5V±10%	-	17.2	μs

T1168E-01

(Vcc=5V±5%, Vcc=5V±10%,, Ta = 0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=5V±5%		Vcc=5V±10%		Unit
	IEEE	PCMCIA		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		150	-	150	-	ns
Address Setup Time	t_{AVWL}	t_{su}(A)		20	-	20	-	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)		20	-	20	-	ns
Data Setup Time for WE#	t_{DVWH}	t_{su}(D-WEH)		50	-	50	-	ns
Data Hold Time	t_{WHDX}	t_{h}(D)		20	-	20	-	ns
OE# Hold Time from WE#	t_{WHGL}	t_{h}(OE-WE)		80	-	80	-	ns
CE# Setup Time for WE#	t_{ELWH}	t_{su}(CE-WEH)		100	-	100	-	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)		100	-	100	-	ns
Write Pulse Width	t_{WLWH}	t_{w}(WE)		80	-	80	-	ns
WE# High to RDY/BSY# going Low	t_{WHRL}			-	140	-	140	ns
RESET Recovery Time	t_{PHWL}			1	-	1	-	μs
V_{PP} Setup Time	t_{VPWH}			100	-	100	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	0	-	ns
Word/Byte Write Time	t_{WHQV1}		V_{PP}=5V±10%	-	120	-	120	μs
Block Erase Time	t_{WHQV2}		V_{PP}=5V±10%	-	7.5	-	7.5	s
Set Lock-Bit Time	t_{WHQV3}		V_{PP}=5V±10%	-	120	-	120	μs
Clear Block Lock-Bits Time	t_{WHQV4}		V_{PP}=5V±10%	-	10	-	10	s
Word/Byte Suspend Latency Time to Read	t_{WHRH1}		V_{PP}=5V±10%	-	7.0	-	7.0	μs
Erase Suspend Latency Time to Read	t_{WHRH2}		V_{PP}=5V±10%	-	13.1	-	13.1	μs

T1169E-01

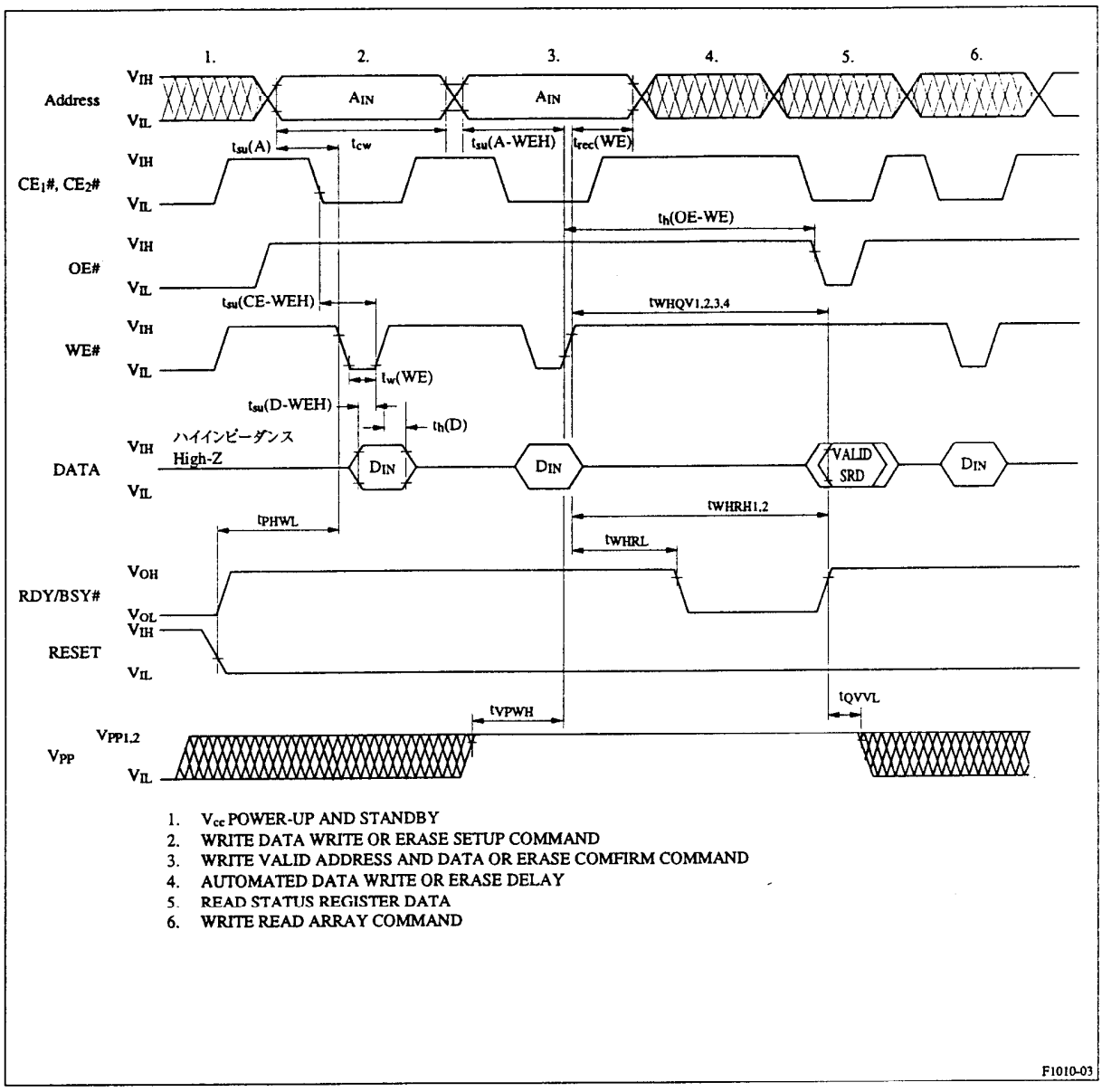


Figure 7. AC Waveforms for Write Operations (WE# Controlled)

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

13. 2. 2 CE# Controlled Write Operations

(Vcc=3.3V±0.3V, Ta = 0 to 60℃)

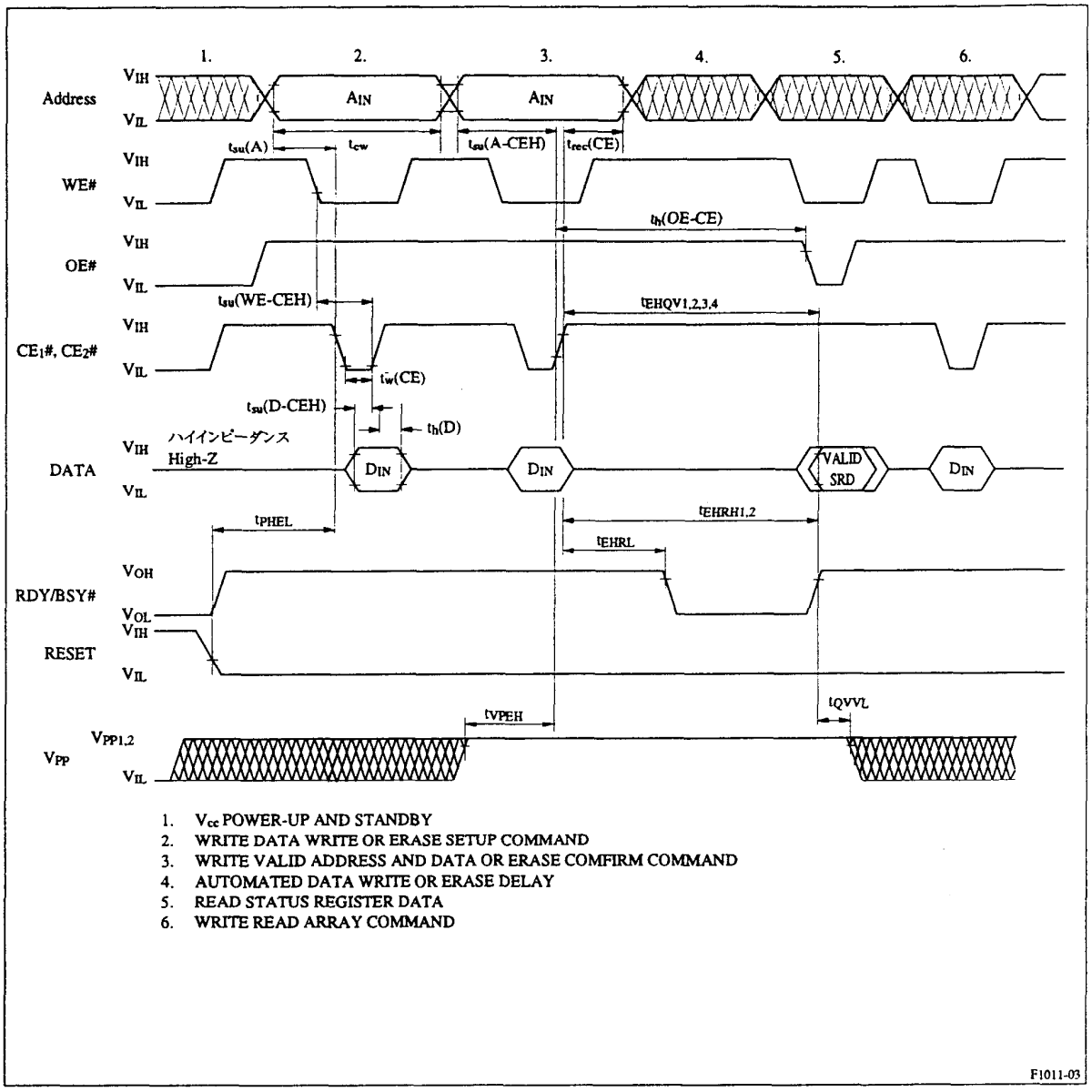
PARAMETER	SYMBOL		CONDITION	Vcc=3.3V±0.3V		Unit
	IEEE	PCMCIA		MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		250	-	ns
Address Setup Time	t_{AVEL}	t_{su}(A)		30	-	ns
Write Recovery Time	t_{EHAX}	t_{rec}(CE)		30	-	ns
Data Setup Time for CE#	t_{DVEH}	t_{su}(D-CEH)		60	-	ns
Data Hold Time	t_{EHDX}	t_{h}(D)		30	-	ns
OE# Hold Time from CE#	t_{EHGL}	t_{h}(OE-CE)		120	-	ns
WE# Setup Time for CE#	t_{WLEH}	t_{su}(WE-CEH)		180	-	ns
Address Setup Time for CE#	t_{AVEH}	t_{su}(A-CEH)		180	-	ns
Write Pulse Width	t_{ELEH}	t_{w}(CE)		150	-	ns
CE# High to RDY/BSY# going Low	t_{EHRL}			-	140	ns
RESET Recovery Time	t_{PHEL}			1	-	μs
V_{PP} Setup Time	t_{VPEH}			180	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	ns
Word/Byte Write Time	t_{EHQV1}		V_{PP}=3.3V±0.3V	-	250	μs
			V_{PP}=5V±10%	-	180	μs
Block Erase Time	t_{EHQV2}		V_{PP}=3.3V±0.3V	-	16.5	s
			V_{PP}=5V±10%	-	10.9	s
Set Lock-Bit Time	t_{EHQV3}		V_{PP}=3.3V±0.3V	-	250	μs
			V_{PP}=5V±10%	-	180	μs
Clear Block Lock-Bits Time	t_{EHQV4}		V_{PP}=3.3V±0.3V	-	10	s
			V_{PP}=5V±10%	-	10	s
Word/Byte Suspend Latency Time to Read	t_{EHRH1}		V_{PP}=3.3V±0.3V	-	10.0	μs
			V_{PP}=5V±10%	-	9.3	μs
Erase Suspend Latency Time to Read	t_{EHRH2}		V_{PP}=3.3V±0.3V	-	21.1	μs
			V_{PP}=5V±10%	-	17.2	μs

T1170E-01

(Vcc=5V±5%, Vcc=5V±10%, Ta=0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=5V±5%		Vcc=5V±10%		Unit
	IEEE	PCMCIA		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		150	-	150	-	ns
Address Setup Time	t_{AVEL}	t_{su}(A)		20	-	20	-	ns
Write Recovery Time	t_{EHAX}	t_{rec}(CE)		20	-	20	-	ns
Data Setup Time for CE#	t_{DVEH}	t_{su}(D-CEH)		50	-	50	-	ns
Data Hold Time	t_{EHDX}	t_{h}(D)		20	-	20	-	ns
OE# Hold Time from CE#	t_{EHGL}	t_{h}(OE-CE)		80	-	80	-	ns
WE# Setup Time for CE#	t_{WLEH}	t_{su}(WE-CEH)		100	-	100	-	ns
Address Setup Time for CE#	t_{AVEH}	t_{su}(A-CEH)		100	-	100	-	ns
Write Pulse Width	t_{ELEH}	t_{w}(CE)		80	-	80	-	ns
CE# High to RDY/BSY# going Low	t_{EHRL}			-	140	-	140	ns
RESET Recovery Time	t_{PHEL}			1	-	1	-	μs
V_{PP} Setup Time	t_{VPEH}			100	-	100	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	0	-	ns
Word/Byte Write Time	t_{EHQV1}		V_{PP}=5V±10%	-	120	-	120	μs
Block Erase Time	t_{EHQV2}		V_{PP}=5V±10%	-	7.5	-	7.5	s
Set Lock-Bit Time	t_{EHQV3}		V_{PP}=5V±10%	-	120	-	120	μs
Clear Block Lock-Bits Time	t_{EHQV4}		V_{PP}=5V±10%	-	10	-	10	s
Word/Byte Suspend Latency Time to Read	t_{EHRH1}		V_{PP}=5V±10%	-	7.0	-	7.0	μs
Erase Suspend Latency Time to Read	t_{EHRH2}		V_{PP}=5V±10%	-	13.1	-	13.1	μs

T1171E-01



1. V_{CC} POWER-UP AND STANDBY
2. WRITE DATA WRITE OR ERASE SETUP COMMAND
3. WRITE VALID ADDRESS AND DATA OR ERASE COMFIRM COMMAND
4. AUTOMATED DATA WRITE OR ERASE DELAY
5. READ STATUS REGISTER DATA
6. WRITE READ ARRAY COMMAND

F1011-03

Figure 8. AC Waveforms for Write Operations (CE# Controlled)

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

13. 3 Attribute Memory Read Operation

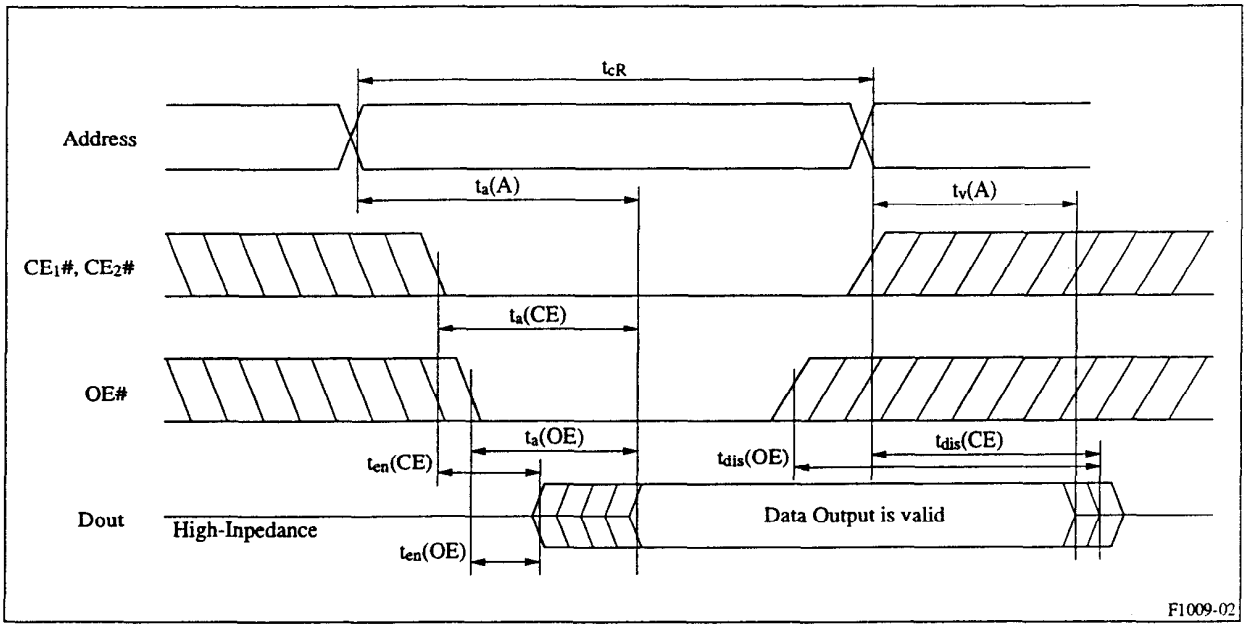
(Ta=0～60℃)

PARAMETER	SYMBOL		Vcc=3.3V± 0.3V		Vcc=5V± 10%		Unit
	IEEE	PCMCIA	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{AVAV}	t_{cR}	600	—	300	—	ns
Address Access Time	t_{AVQV}	t_a(A)	—	600	—	300	
CE# Access Time	t_{ELQV}	t_a(CE)	—	600	—	300	
OE# Access Time	t_{GLQV}	t_a(OE)	—	300	—	150	
Output Disable Time from CE1#,CE2# *	t_{EHQZ}	t_{dis}(CE)	—	150	—	100	
Output Disable Time from CE#	t_{GHQZ}	t_{dis}(OE)	—	150	—	100	
Output Disable Time from CE1#,CE2#	t_{ELQNZ}	t_{en}(CE)	5	—	5	—	
Output Disable Time from OE#	t_{GLQNZ}	t_{en}(OE)	5	—	5	—	
Data Valid Time from Address Change		t_v(A)	0	—	0	—	

*: Time until becomes floating. (The output voltage is not defined)

T1056-01

Note) When the CIS constructed by EEPROM, this card requires 5V voltage for Vcc.



F1009-02

Figure 9. Attribute Memory Read Operation

13. 4 Attribute Memory Write Operation

(Ta=0～60℃)

PARAMETER	SYMBOL		Vcc=3.3V± 0.3V		Vcc=5V± 10%		Unit
	IEEE	PCMCIA	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}	600	—	250	—	ns
Address Setup Time	t_{AVWL}	t_{su}(A)	50	—	30	—	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)	70	—	30	—	ns
Data Setup Time	t_{DVWH}	t_{su}(D-WEH)	150	—	80	—	ns
Data Hold Time	t_{WHDX}	t_h(D)	70	—	30	—	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)	350	—	180	—	ns
Write Pulse Width	t_{WLWH}	t_w(WE)	300	—	150	—	ns
Setup Time for OE#	t_{GHWL}	t_{su}(OE-WE)	35	—	10	—	ns
Hold Time for OE#	t_{WHGL}	t_h(OE-WE)	35	—	10	—	ns
Setup Time for CE#	t_{ELWH}	t_{su}(CE)	0	—	0	—	ns
Hold Time for CE#	t_{GHEH}	t_h(CE)	35	—	20	—	ns

T1057-01

Note) When the CIS constructed by EEPROM, this card requires 5V voltage for Vcc.

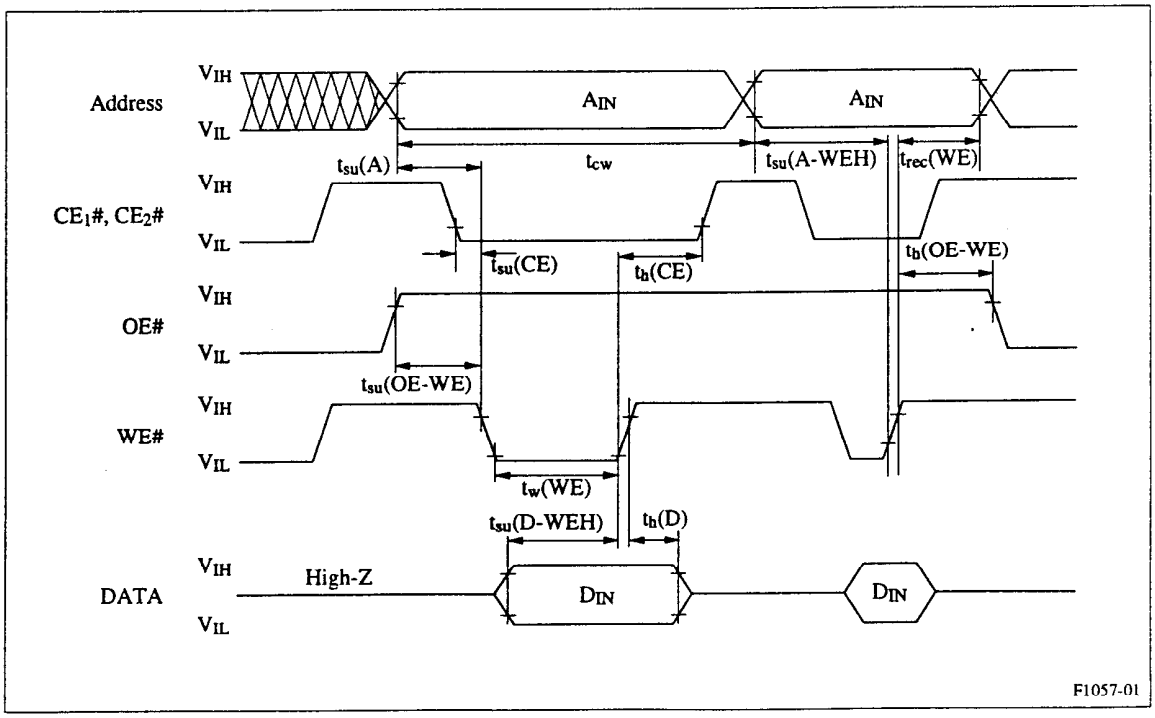


Figure 10. Attribute Memory Write Operation

13. 5 Power-Up/Power Down

PARAMETER	SYMBOL PCMCIA	NOTES	MIN	MAX	UNITS
CE# Signal Level (0.0V < V_{CC} < 2.0V)	V_i (CE)	1	0	V_{iMAX}	V
CE# Signal Level (2.0V < V_{CC} < V_{IH})		1	V_{CC}–0.1	V_{iMAX}	V
CE# Signal Level (V_{IH} < V_{CC})		1	V_{IH}	V_{iMAX}	V
CE# Setup Time	t_{su} (V_{CC})	—	20	—	ms
RESET Setup Time	t_{su} (RESET)	—	20	—	ms
CE# Recover Time	t_{rec} (V_{CC})	—	1.0	—	µs
V_{CC} Rising Time	t_{pr}	2	0.1	300	ms
V_{CC} Falling Time	t_{pf}	2	3.0	300	ms
RESET Width	t_w (RESET)	—	10	—	µs
RESET Width	t_h (Hi–Z RESET)	—	1	—	ms
RESET Width	t_s (Hi–Z RESET)	—	0	—	ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0V < V_{CC} < 2.0 V, Vi (CE#) is only 0.00V-V_{iMAX}
2. The t_{pr} and t_{pf} are defined as "linear waveforms" in the period of 10% to 90%, or vice-versa. Even if the waveform is not a "liner waveform," its rising and falling time must meet this specification.

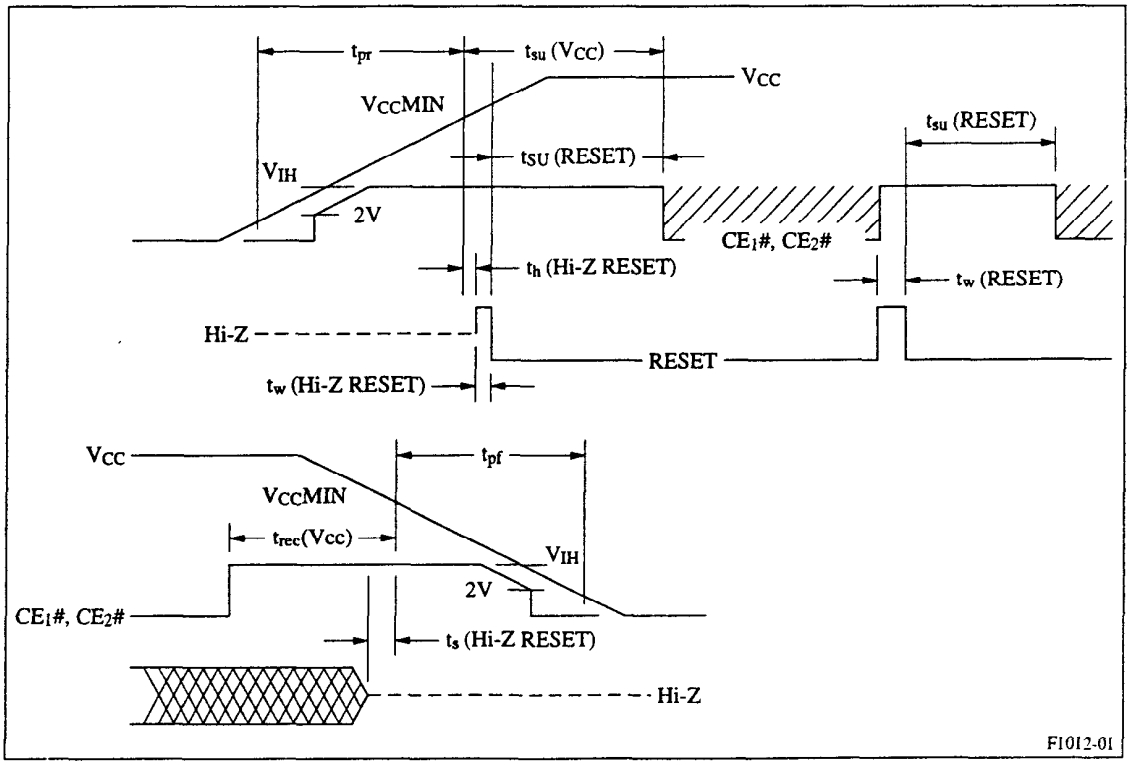


Figure 11. Power-Up/Down Timing

14. Specification Changes

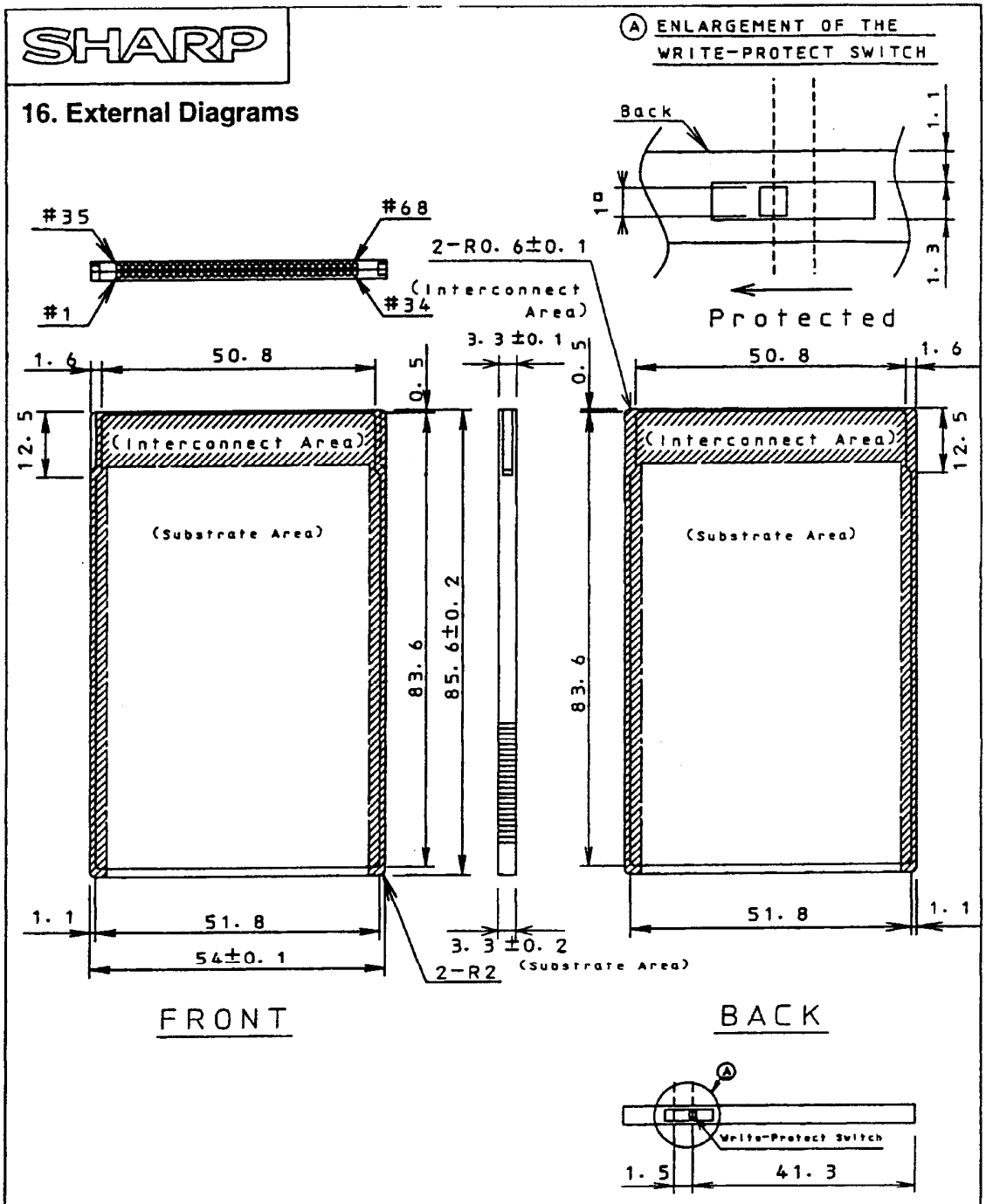
This datasheet is for ID246 series product overview, and final specifications will be submitted for qualification of the memory card. Please note that contents of this datasheet may be revised without announcement beforehand. Please do NOT finalize a system design with this information.

15. Other Precautions

- Permanent damage occurs if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

SHARP

16. External Diagrams



APPPLICABLE		SCALE	UNIT	1997.9.12	All revised	aoaki
		1/1	mm	CH. DATE	REVISE	CHARGE
THICKNESS		MATERIAL	FINISH	NAME	MEMORY CARD EXTERNAL DIAGRAM	
DATE	1997.9.8				PCMCIA Rel. 2.0 TYPE1	
DESIGN / DRAW / TRACE / CHECK / APPROVE	Card Business Project Team					
S.Sawada	FUKUYAMA IC GROUP SHARP CORPORATION			DRAWING NO.	IMC026-A103	