PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LRS1329

Stacked Chip

16M Flash and 2M SRAM

(Model No.: LRS1329)

Spec No.: MFM2-J11601
Issue Date: June 10, 1999

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(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

Part 1 Overview

1. Description

The LRS1329 is a combination memory organized as 1M x16/2M x8 bit flash memory and 256K x8 bit static RAM in one package.

Features

○Power supply .... 2.7 V to 3.6 V
○Operating temperature .... −25 ℃ to +85 ℃
○Not designed or rated as radiation hardened
○ 72 pin CSP (LCSP072-P-0811) plastic package
○Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

Flash Memory

○Access Time .... 100 ns (Max.)

○Operating current (The current for F-V_{CC} pin)
Read .... 25 mA (Max. t_{CYCLE}=200ns)
Word/Byte write .... 17 mA (Max.)
Block erase .... 17 mA (Max.)
○Deep power down current (The current for F-V_{CC} pin) .... 10 μA (Max. F-$\overline{CE}$≧F-V_{CC}-0.2V, F-$\overline{RP}$≦0.2V, F-V_{PP}≦0.2V)

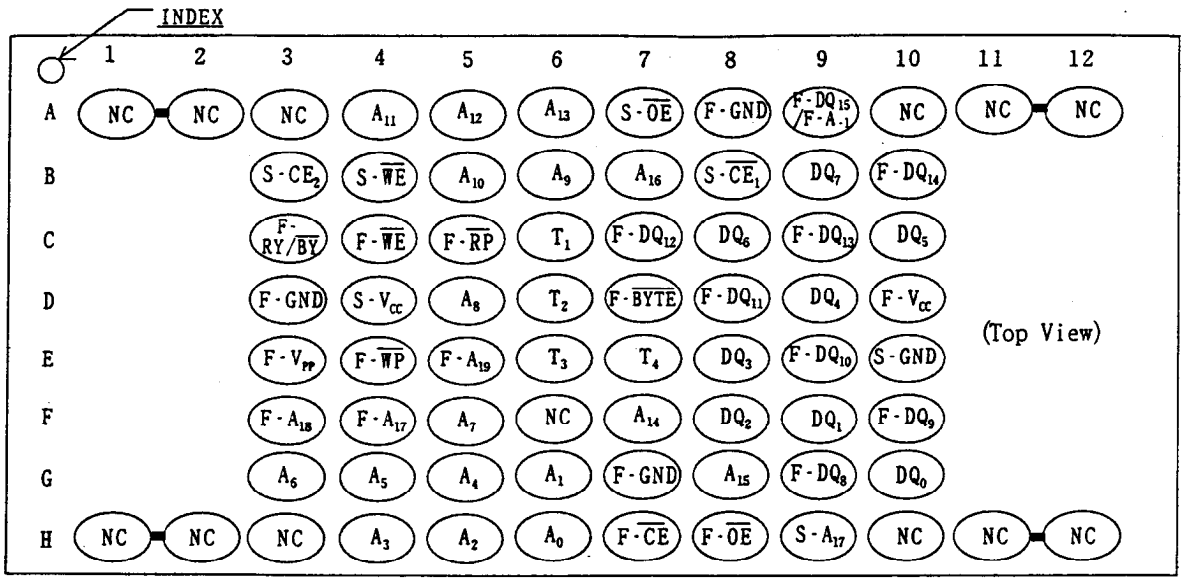
○Optimized Array Blocking Architecture
Two 4K-word/8K-byte Boot Blocks/ Six 4K-word/8K-byte Parameter Blocks/
Thirty-one 32K-word/64K-byte Main Blocks/ Top Boot Location
○ Extended Cycling Capability
100,000 Block Erase Cycles
○ Enhanced Automated Suspend Options
Word/Byte write Suspend to Read
Block Erase Suspend to Word/Byte write
Block Erase Suspend to Read

SRAM

○Access Time .... 85 ns (Max.)

○Operating current .... 30 mA (Max.)
.... 3 mA (Max. t_{RC}, t_{WC}=1 μs)
○Standby current .... 15 μA (Max.)
○Data retention current .... 15 μA (Max.)

2. Pin Configuration



Notes: All F-GND and S-GND pins must connect to GND.
Two NC pins at the corner are connected.
From T_1 to T_4 pins need to be open.

Pin	Description	
A_0 to A_{16}	Address Inputs (Common)	
F-A_{-1}, F-A_{17} to F-A_{18}	Address Inputs (Flash) F-A_{-1}: Not used in x16 mode.	
S-A_{17}	Address Input (SRAM)	
F-$\overline{CE}$	Chip Enable (Flash)	
S-$\overline{CE_1}$, S-CE_2	Chip Enable (SRAM)	
F-$\overline{WE}$	Write Enable (Flash)	
S-$\overline{WE}$	Write Enable (SRAM)	
F-$\overline{OE}$	Output Enable (Flash)	
S-$\overline{OE}$	Output Enable (SRAM)	
F-$\overline{RP}$	Reset/Deep Power Down (Flash) Block erase and Word/Byte Write : V_{IH} or V_{HH} Read : V_{IH} or V_{HH} Deep Power Down : V_{IL}	
F-$\overline{WP}$	Write Protect (Flash) Two Boot Blocks Locked : V_{IL} (With F-$\overline{RP}$=V_{HH} Erase/Write can operate to all block)	
F-$\overline{BYTE}$	Byte Enable (Flash); x8 mode: V_{IL}, x16 mode: V_{IH}	
F-RY/$\overline{BY}$	Ready/Busy (Flash) During an Erase or Write operation : V_{OL} Block Erase and Word/Byte Write Suspend : High-Z Deep Power Down : V_{OH}	
DQ_0 to DQ_7	Data Input/Outputs (Common)	
F-DQ_8 to F-DQ_{15}	Data Inputs/Outputs (Flash); Not used in x8 mode.	
F-V_{CC}	Power Supply (Flash)	
S-V_{CC}	Power Supply (SRAM)	
F-V_{PP}	Write, Erase Power Supply (Flash) Block Erase and Word/Byte Write : F-V_{PP}=V_{PPLK} All Blocks Locked : F-V_{PP}<V_{PPLK}	
F-GND	GND (Flash)	
S-GND	GND (SRAM)	
NC	No Connect	
T_1 to T_4	Test pins (Should be open)	

3. Truth Table (*1)

Flash	SRAM	Note	F-$\overline{CE}$	F-$\overline{RP}$	F-$\overline{OE}$	F-$\overline{WE}$	S-$\overline{CE_1}$	S-CE_2	S-$\overline{OE}$	S-$\overline{WE}$	F-$\overline{BYTE}$	DQ_8 to DQ_7	F-DQ_8 to F-DQ_{15}
Read	Standby	*4, 5	L	H	L	H	*7		X	X	H	DOUT	
											L	DOUT	High-Z
Output Disable					H						H	High-Z	
											L		
Write		*2, 3, 4				L					H	DIN	
											L	DIN	High-Z
Standby	Read	*6	H	H	X	X	L	H	L	H	X	DOUT	High-Z
	Output Disable	*6							H			High-Z	
	Write	*6								L		DIN	
Reset Power Down	Read	*6	X	L	X	X	L	H	L	H	X	DOUT	High-Z
	Output Disable	*6							H			High-Z	
	Write	*6								L		DIN	
Standby	Standby	*6	H	H	X	X	*7		X	X	X	High-Z	
Reset Power Down		*6	X	L									

Notes) *1. L=V_{IL}, H=V_{IH} , X=H or L . Refer to DC Characteristics.

*2. Command writes involving block erase or word/byte write are reliably executed when F-V_{PP}=V_{PPH} and F-V_{CC}=2.7V to 3.6V. Block erase or word/byte write with V_{IH}<F-$\overline{RP}$<V_{HH} produce spurious results and should not be attempted.

*3. Refer Section 5. Flash Memory Comand Definition for valid DIN during a write operation.

*4. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.

*5. F-A_{-1} set to V_{IL} or V_{IH} in byte mode (F-$\overline{BYTE}$=V_{IL}).

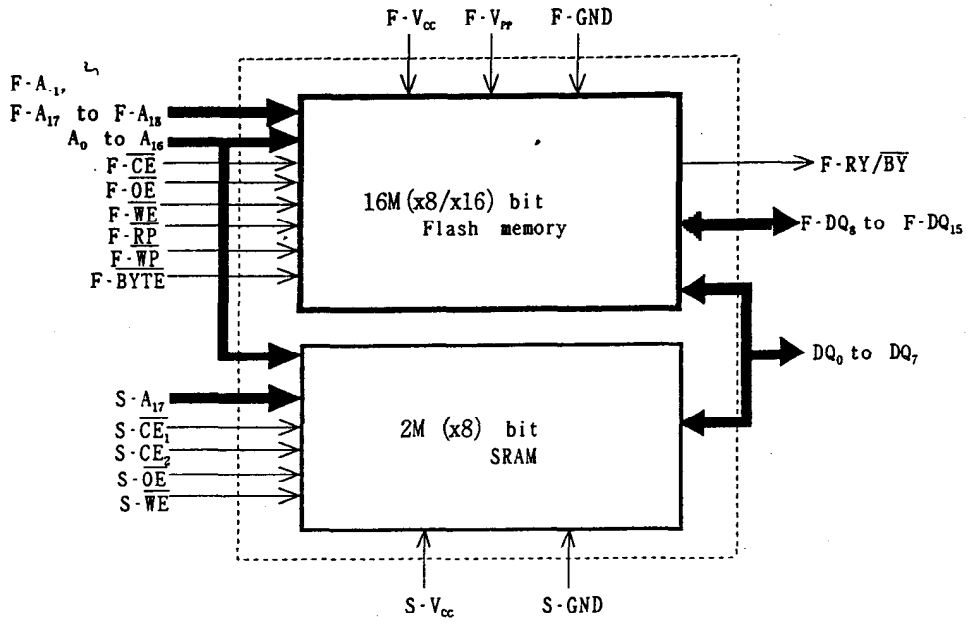
*6. F-$\overline{WP}$ set to V_{IL} or V_{IH}.

*7. See the following SRAM Standby mode.

SRAM Standby Mode

Mode	S-$\overline{CE_1}$	S-CE_2
SRAM Standby	H	X
	X	L

4. Block Diagram



5 Command Definitions for Flash Memory (*1)

Command	Bus Cycles Req'd.	Note	First Bus Cycle			Second Bus Cycle		
			Oper (*2)	Address (*3)	Data (*3)	Oper (*2)	Address (*3)	Data (*3)
Read Array/Reset	1		Write	XA	FFH			
Read Identifier Codes	≧2	*4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	*5	Write	BA	20H	Write	BA	D0H
Word/Byte Write	2	*5	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	*5	Write	XA	B0H			
Block Erase and Word/Byte Write Resume	1	*5	Write	XA	D0H			

Note)

*1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

*2. BUS operations are defined in 3. Truth Table.

*3. XA=Any valid address within the device.
IA=Identifier Code Address.
BA=Address within the block being erased.
WA=Address of memory location to be written.
SRD=Data read from status register (See the next page "Status Register Definition").
WD=Data to be written at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
ID=Data read from identifier codes.

*4. See the Following Identifier Codes.

*5. See the following Write Protection Alternatives.

Identifier Codes

Codes	Address [A_{18}-A_0]	Data [DQ_7-DQ_0]
Manufacture Code	00000H	B0H
Device Code	00001H	48H

Write Protection Alternatives

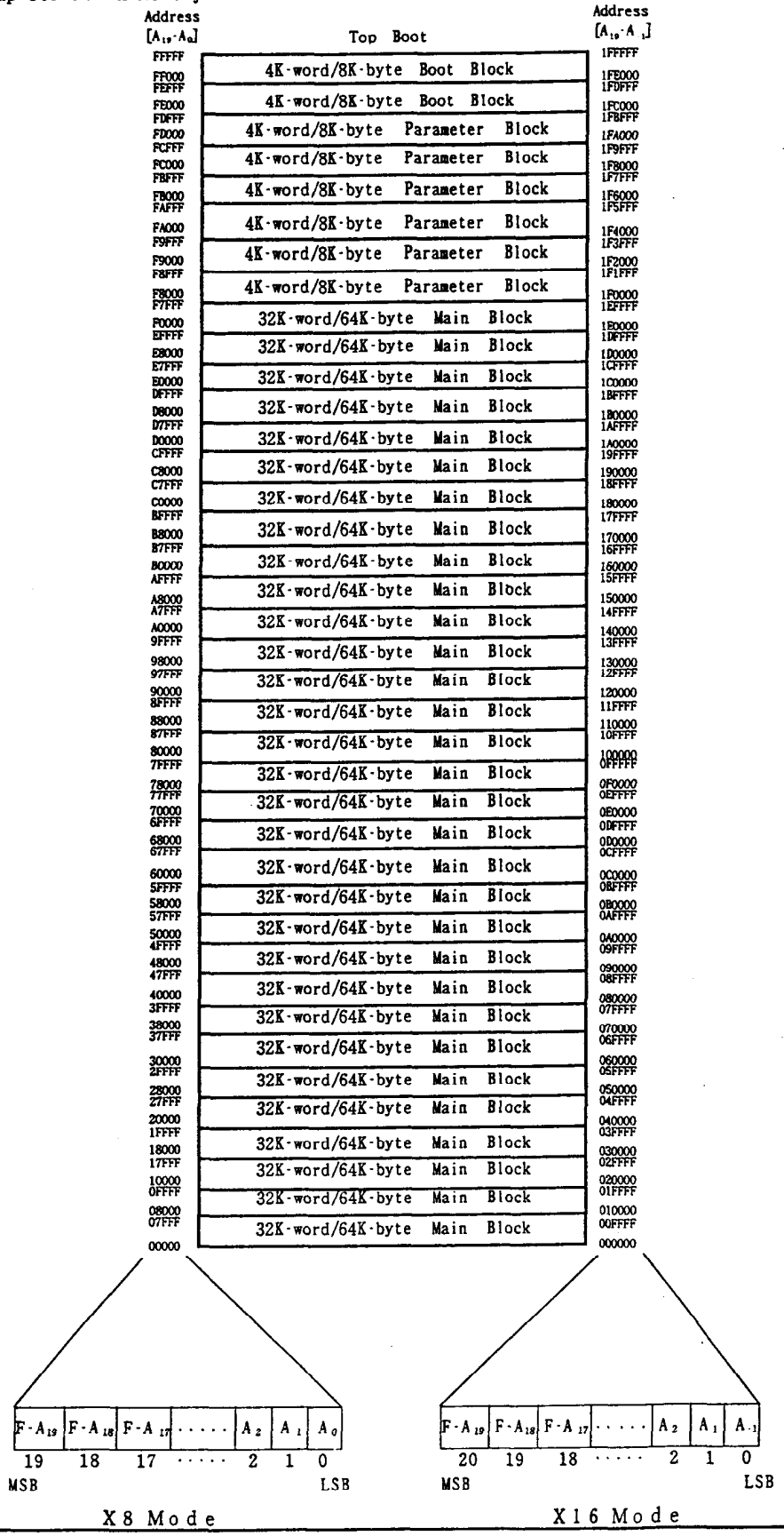
Operation	F-V_{PP}	F-$\overline{RP}$	F-$\overline{WP}$	Effect
Block Erase or Word/Byte Write	V_{IL}	X	X	All Blocks Locked.
	>V_{PPLK}	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{IH}	V_{IL}	2 Boot Blocks Locked.
		V_{IH}	V_{IH}	All Blocks Unlocks.

6. Status Register Definition

WSMS	ESS	ES	WBWS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	NOTES: Check RY/$\overline{BY}$ or SR.7 to determine block erase or word/byte write completion. SR.6-0 are invalid while SR.7="0".
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase	If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.
SR.4 = WORD/BYTE WRITE STATUS (WBWS) 1 = Error in Word/Byte Write 0 = Successful Word/Byte Write	
SR.3 = V_{PP} STATUS (VPPS) 1 = F-V_{PP} Low Detect, Operation Abort 0 = F-V_{PP} OK	SR.3 does not provide a continuous indication of F-V_{PP} level. The WSM interrogates and indicates the F-V_{PP} level only after Block Erase or Word/Byte Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-$V_{PP} \neq V_{PPH1/2}$.
SR.2 = WORD/BYTE WRITE SUSPENDED STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = F-$\overline{WP}$ or F-$\overline{RP}$ Lock Detected, Operation Abort 0 = Unlock	The WSM interrogates the F-$\overline{WP}$ and F-$\overline{RP}$ only after Block Erase or Word/Byte Write command sequences. It informs the system, depending on the attempted operation, if the F-$\overline{WP}$ is not V_{IH}, F-$\overline{RP}$ is not V_{HH}.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.

7. Memory Map for Flash Memory



8. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1, 2)	V_{CC}	−0.2 to +4.6	V
Input voltage (*1, 3)	V_{IN}	−0.2 (*4) to Vcc+0.3	V
Operating temperature	T_{opr}	−25 to +85	℃
Storage temperature	T_{stg}	−65 to +125	℃
F-V_{PP} voltage (*1)	F-V_{PP}	−0.2 (*4) to +14.0(*5)	V
F-$\overline{RP}$ voltage (*1)	F-$\overline{RP}$	−0.5 (*4) to +14.0(*5)	V

Notes) *1. The maximum applicable voltage on any pins with respect to GND.
*2. Except F-V_{PP}.
*3. Except F-$\overline{RP}$.
*4. −2.0V undershoot is allowed when the pulse width is less than 20nsec.
*5. +14.0V overshoot is allowed when the pulse width is less than 20nsec.

9. Recommended DC Operating Conditions

(T_a= −25 ℃ to +85 ℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.2		V_{CC}+0.3(*1)	V
	V_{IL}	−0.2 (*2)		0.8	V
	V_{HH} (*3)	11.4		12.6	V

Notes) *1. V_{CC} is the lower one of S-V_{CC} and F-V_{CC} .
*2. −2.0V undershoot is allowed when the pulse width is less than 20nsec.
*3. This voltage is applicable to F-$\overline{RP}$ Pin only.

10. Pin Capacitance

(T_a=25℃, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN}=0V			20	pF	*1
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V			22	pF	*1

Note) *1 Sampled but not 100% tested

11. DC Characteristics

DC Characteristics (T_a= −25℃ to +85℃, V_{CC}= 2.7 V to 3.6 V)

Parameter		Symbol	Conditions		Min.	Typ. (*1)	Max.	Unit
Input leakage current (I_{LI})		I_{LI}	V_{IN} =V_{CC} or GND		−1.5		+1.5	μA
Output leakage current (I_{LO})		I_{LO}	V_{OUT} =V_{CC} or GND		−1.5		+1.5	μA
F-V_{CC}	V_{CC} Standby Current	I_{CCS} (*2, 7)	F-$\overline{CE}$=F-$\overline{RP}$=F-V_{CC} ±0.2V F-$\overline{WP}$=F-V_{CC} ±0.2V or F-GND±0.2V			25	50	μA
			F-$\overline{CE}$=F-$\overline{RP}$=V_{IH} F-$\overline{WP}$=V_{IH} or V_{IL}			0.2	2	mA
	Deep Power-Down Current	I_{CCD} (*7)	F-$\overline{RP}$=F-GND±0.2V, I_{OUT} (F-RY/$\overline{BY}$)=0mA			5	10	μA
	V_{CC} Read Current	I_{CCR} (*3, 4)	CMOS Input F-$\overline{CE}$=F-GND, f=5MHz, I_{OUT} =0mA				25	mA
			TTL Input F-$\overline{CE}$=F-GND, f=5MHz, I_{OUT} =0mA				30	mA
	V_{CC} Word/Byte Write Current	I_{CCW}	F-V_{PP} =V_{PPH}				17	mA
	V_{CC} Block Erase Current	I_{CCE}	F-V_{PP} =V_{PPH}				17	mA
	V_{CC} Word/Byte Write Block Erase Suspend Current	I_{CCWS} I_{CCES}	F-$\overline{CE}$=V_{IH}				6	mA
F-V_{PP}	V_{PP} Standby or Read Current	I_{PPS}	F-V_{PP} = F-V_{CC}			±2	±15	μA
		I_{PPR}	F-V_{PP} > F-V_{CC}			10	200	μA
	V_{PP} Deep Power-Down Current	I_{PPD}	F-$\overline{RP}$=F-GND±0.2V			0.1	5	μA
	V_{PP} Word/Byte Write Current	I_{PPW}	F-V_{PP} =V_{PPH}			12	40	mA
	V_{PP} Block Erase Current	I_{PPE}	F-V_{PP} =V_{PPH}			8	25	mA
	V_{PP} Word/Byte Write or Block Erase Suspend Current	I_{PPWS} I_{PPES}	F-V_{PP} =V_{PPH}			10	200	μA
S-V_{CC}	Standby Current	I_{SB}	S-$\overline{CE_1}$, S-CE_2≧S-V_{CC}-0.2V or S-CE_2≦0.2V				15	μA
		I_{SB1}	S-$\overline{CE_1}$=V_{IH} or S-CE_2=V_{IL}				3.0	mA
	Operation Current	I_{CC1}	S-$\overline{CE_1}$=V_{IL}, S-CE_2=V_{IH} V_{IN}=V_{IL} or V_{IH}	t_{CYCLE}=Min. $I_{I/O}$=0mA			30	mA
		I_{CC2}	S-$\overline{CE_1}$=0.2V, S-CE_2=S-V_{CC}-0.2V V_{IN}=S-V_{CC}-0.2V or 0.2V	t_{CYCLE}=1μs $I_{I/O}$=0mA			3	mA

DC Characteristics (Continue) (T_a= −25℃ to +85℃ , V_{CC}= 2.7 V to 3.6 V)

Parameter	Symbol	Test Conditions	Min.	Typ. (*1)	Max.	Unit
Input Low Voltage	V_{IL}		−0.2		0.8	V
Input High Voltage	V_{IH}		2.2		V_{CC}+0.3	V
Output Low Voltage	V_{OL} (*2)	I_{OL} = 2.0 mA			0.4	V
Output High Voltage	V_{OH1} (*2)	I_{OH} = −1.0 mA	2.4			V
F-V_{PP} Lockout during Normal Operations	V_{PPLK} (*5)				1.5	V
F-V_{PP} Word/Byte Write or Block Erase Operations	V_{PPH}		2.7		3.6	V
F-V_{CC} Lockout Voltage	V_{LKO}		1.5			V
F-$\overline{RP}$ Unlock Voltage	V_{HH} (*6)	Unavailable F-$\overline{WP}$	11.4		12.6	V

Notes)

1. Reference values at V_{CC}=3.0V and T_a=+25°C.
2. Includes F-RY/$\overline{BY}$.
3. Automatic Power Savings (APS) for Flash Memory reduces typical I_{CCR} to 3mA at 2.7V V_{CC} in static operation.
4. CMOS inputs are either V_{CC} ±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
5. Block erases and word/byte writes are inhibited when F-V_{PP} ≦V_{PPLK} and not guaranteed in the range between V_{PPLK} (max) and V_{PPH} (min), and above V_{PPH} (max).
6. F-$\overline{RP}$ connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.
7. F-$\overline{BYTE}$ is V_{CC}±0.2V in word mode and is GND±0.2V in byte mode.
   F-$\overline{WP}$ is V_{CC}±0.2V or GND±0.2V.

12. Flash memory AC Characteristics

AC Test Condtions

Input pulse level	0 V to 2.7 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.35 V
Output load	1TTL+C_L(30pF)

Read Cycle (T_a= −25℃ to +85℃, V_{CC}= 2.7V to 3.6V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t_{AVAV}	100		ns	
Address to Output Delay	t_{AVQV}		100	ns	
F-$\overline{CE}$ to Output Delay	t_{ELQV}		100	ns	*1
F-$\overline{RP}$ High to Output Delay	t_{PHQV}		10	μs	
F-$\overline{OE}$ to Output Delay	t_{GLQV}		45	ns	*1
F-$\overline{CE}$ to Output in Low Z	t_{ELQX}	0		ns	
F-$\overline{CE}$ High to Output in High Z	t_{EHQZ}		45	ns	
F-$\overline{OE}$ to Output in Low Z	t_{GLQX}	0		ns	
F-$\overline{OE}$ High to Output in High Z	t_{GHQZ}		20	ns	
Output Hold from Address, F-$\overline{CE}$ or F-$\overline{OE}$ Change, Whichever Occurs First	t_{OH}	0		ns	
F-$\overline{BYTE}$ and A_1 to Output Delay	t_{FVQV}		90	ns	
F-$\overline{BYTE}$ Low to Output in High Z	t_{FLQZ}		30	ns	
F-$\overline{CE}$ to F-$\overline{BYTE}$ High Z or Low	t_{ELFV}		5	ns	

Notes) *1. F-$\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of F-$\overline{OE}$ without impact on t_{ELQV}.

Write Cycle (F-$\overline{WE}$ Controlled) (*2) (T_a= −25℃ to +85℃, V_{CC}= 2.7V to 3.6V)

Parameter	Sym.	Min.	Max.	Unit	
Write Cycle Time	t_{AVAV}	100		ns	
F-$\overline{RP}$ High Recovery to F-$\overline{WE}$ going to Low	t_{PHWL}	10		μs	
F-$\overline{CE}$ Setup to F-$\overline{WE}$ Going Low	t_{ELWL}	0		ns	
F-$\overline{WE}$ Pulse Width	t_{WLWH}	50		ns	
F-$\overline{RP}$ V_{HH} Setup to F-$\overline{WE}$ Going High	t_{PHHWH}	100		ns	
F-$\overline{WP}$ V_{IH} Setup to F-$\overline{WE}$ Going High	t_{SHWH}	100		ns	
F-V_{PP} Setup to F-$\overline{WE}$ Going High	t_{VPWH}	100		ns	
Address Setup to F-$\overline{WE}$ Going High	t_{AVWH}	50		ns	*3
Data Setup to F-$\overline{WE}$ Going High	t_{DVWH}	50		ns	*3
Data Hold from F-$\overline{WE}$ High	t_{WHDX}	0		ns	
Address Hold from F-$\overline{WE}$ High	t_{WHAX}	0		ns	
F-$\overline{CE}$ Hold from F-$\overline{WE}$ High	t_{WHEH}	0		ns	
F-$\overline{WE}$ Pulse Width High	t_{WHWL}	30		ns	
F-$\overline{WE}$ High to F-RY/$\overline{BY}$ Going Low	t_{WHRL}		100	ns	
Write Recovery before Read	t_{WHGL}	0		ns	
F-V_{PP} Hold from Valid SRD, F-RY/$\overline{BY}$ High Z	t_{QVVL}	0		ns	
F-$\overline{RP}$ V_{HH} Hold from Valid SRD, F-RY/$\overline{BY}$ High Z	t_{QVPH}	0		ns	
F-$\overline{WP}$ V_{IH} Hold from Valid SRD, F-RY/$\overline{BY}$ High	t_{QVSL}	0		ns	
F-$\overline{BYTE}$ Setup to F-$\overline{WE}$ Going High	t_{FVWH}	50		ns	
F-$\overline{BYTE}$ Hold from F-$\overline{WE}$ High	t_{WHFV}	100		ns	

Write Cycle (F-$\overline{CE}$ Controlled) (*2) (T_a= −25℃ to +85℃ , V_{CC}= 2.7V to 3.6V)

Parameter	Sym.	Min.	Max.	Unit	
Write Cycle Time	t_{AVAV}	100		ns	
F-$\overline{RP}$ High Recovery to F-$\overline{CE}$ going to Low	t_{PHEL}	10		μs	
F-$\overline{WE}$ Setup to F-$\overline{CE}$ Going Low	t_{WLEL}	0		ns	
F-$\overline{CE}$ Pulse Width	t_{ELEH}	70		ns	
F-$\overline{RP}$ V_{HH} Setup to F-$\overline{CE}$ Going High	t_{PHHEH}	100		ns	
F-$\overline{WP}$ V_{IH} Setup to F-$\overline{CE}$ Going High	t_{SHEH}	100		ns	
F-VPP Setup to F-$\overline{CE}$ Going High	t_{VPEH}	100		ns	
Address Setup to F-$\overline{CE}$ Going High	t_{AVEH}	50		ns	*3
Data Setup to F-$\overline{CE}$ Going High	t_{DVEH}	50		ns	*3
Data Hold from F-$\overline{CE}$ High	t_{EHDX}	0		ns	
Address Hold from F-$\overline{CE}$ High	t_{EHAX}	0		ns	
F-$\overline{WE}$ Hold from F-$\overline{CE}$ High	t_{EHWH}	0		ns	
F-$\overline{CE}$ Pulse Width High	t_{EHEL}	25		ns	
F-$\overline{CE}$ High to F-RY/$\overline{BY}$ Going Low	t_{EHRL}		100	ns	
Write Recovery before Read	t_{EHGL}	0		ns	
F-V_{PP} Hold from Valid SRD, F-RY/$\overline{BY}$ High Z	t_{QVVL}	0		ns	
F-$\overline{RP}$ V_{HH} Hold from Valid SRD, F-RY/$\overline{BY}$ High Z	t_{QVPH}	0		ns	
F-$\overline{WP}$ V_{IH} Hold from Valid SRD, F-RY/$\overline{BY}$ High	t_{QVSL}	0		ns	
F-$\overline{BYTE}$ Setup to F-$\overline{CE}$ Going High	t_{FVEH}	50		ns	
F-$\overline{BYTE}$ Hold from F-$\overline{CE}$ High	t_{EHFV}	100		ns	

Notes) *2. Read timing characteristics during block erase and word/byte write operations are the same as during read-only operations. Refer to AC Characteristics for Read Cycle.

*3. Refer to Section 5. Flash Memory Command Definition for valid AIN and DIN for block erase or word/byte write.

Block Erase and Word/Byte Write Performance

(T_a= −25℃ to +85℃, V_{CC}= 2.7 V to 3.6 V)

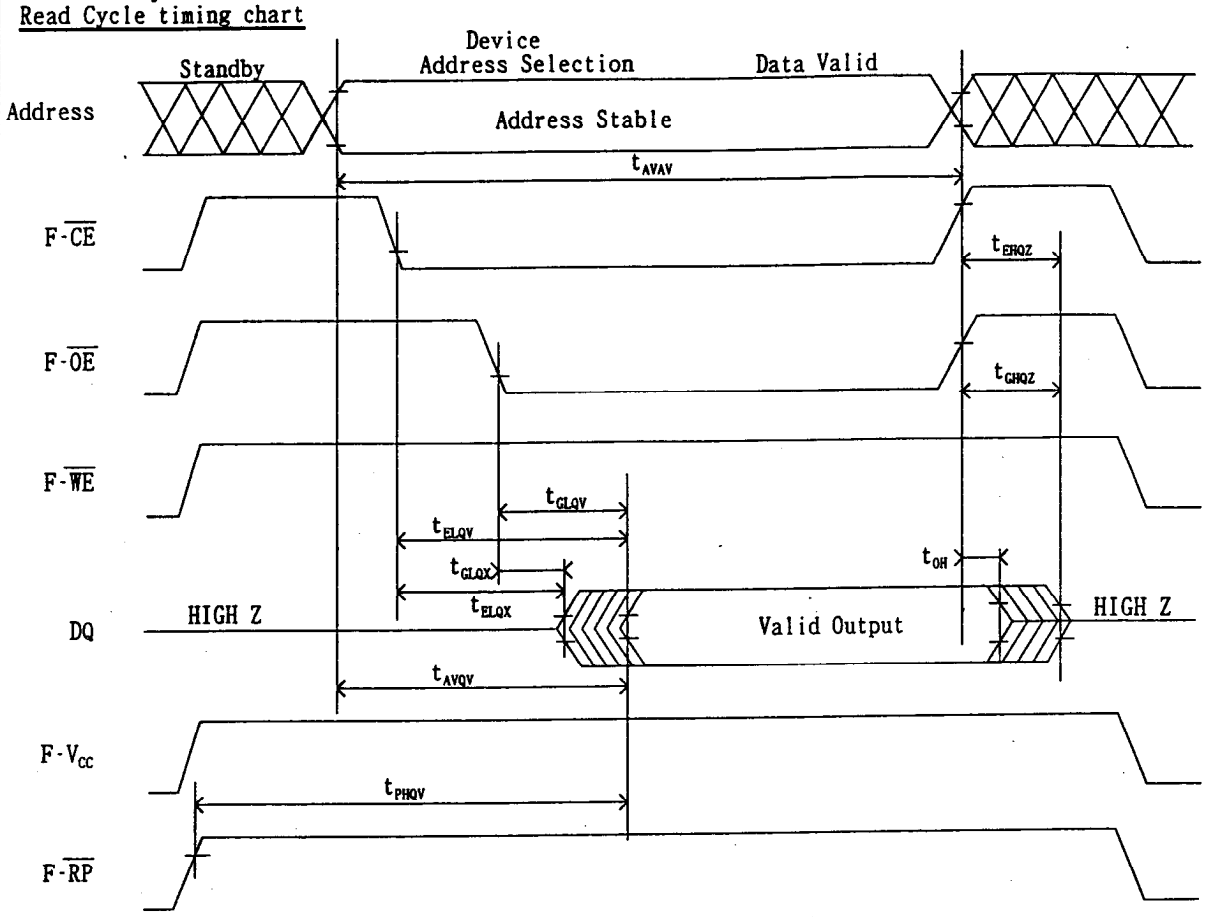
Sym.	Parameter		V_{PP}= 2.7 V to 3.6 V Min.	Typ. (*4)	Max.	Unit	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	32K-word Block /64K-byte Block		55		μs	*5
		4K-word Block /8K-byte Block		60		μs	*5
	Block Write Time (at word mode)	32K-word Blcok		1.8		s	*5
		4K-word Block		0.3			
	Block Write Time (at byte mode)	64K-byte Block		3.6		s	*5
		8K-byte Block		0.6			
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K-word Block 64K-byte Block		1.2		s	*5
		4K-word Block 8K-byte Block		0.5		s	*5
t_{WHRZ1} t_{EHRZ1}	Word/Byte Write Suspend Latency Time to Read			7.5	8.6	μs	
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read			19.3	23.6	μs	

Notes) *4. Reference values at T_a= +25℃ and V_{CC}=3.0V, V_{PP}=3.0V.

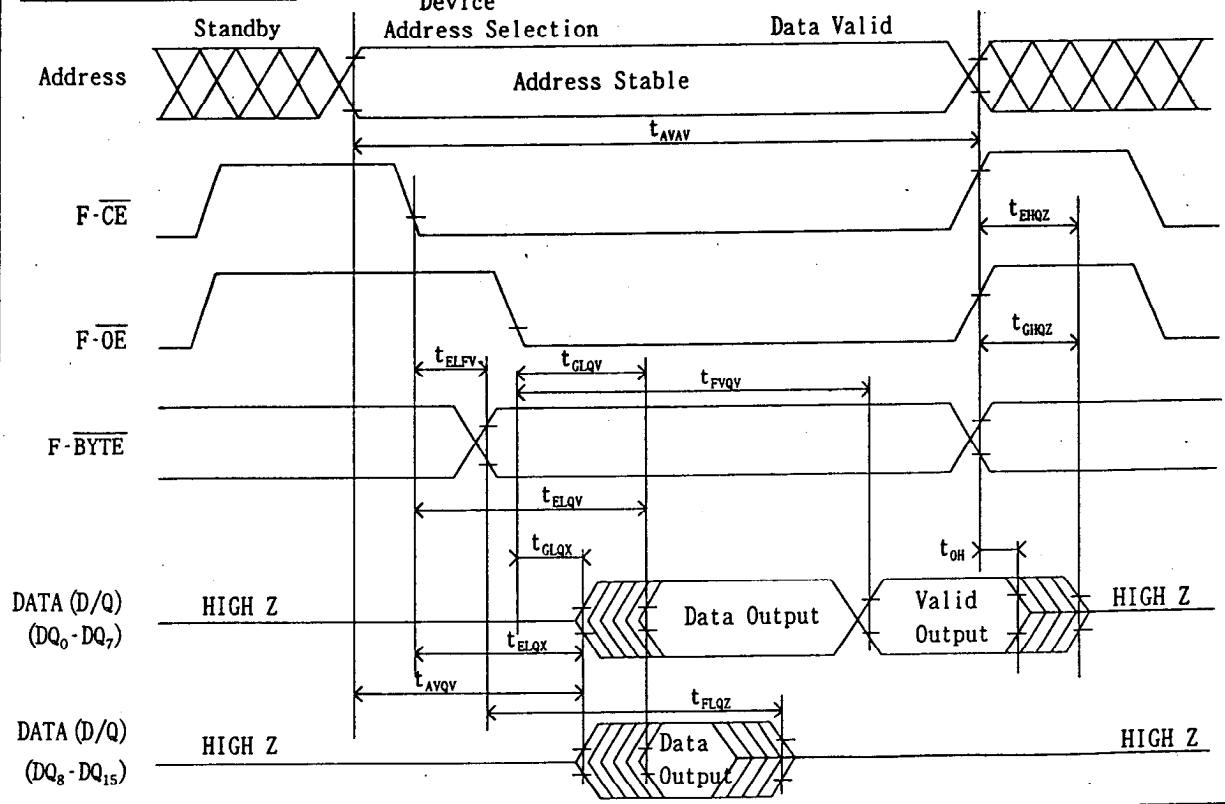
*5. Excludes system-lebel overhead.

Flash Memory AC Characteristic Timing Chart

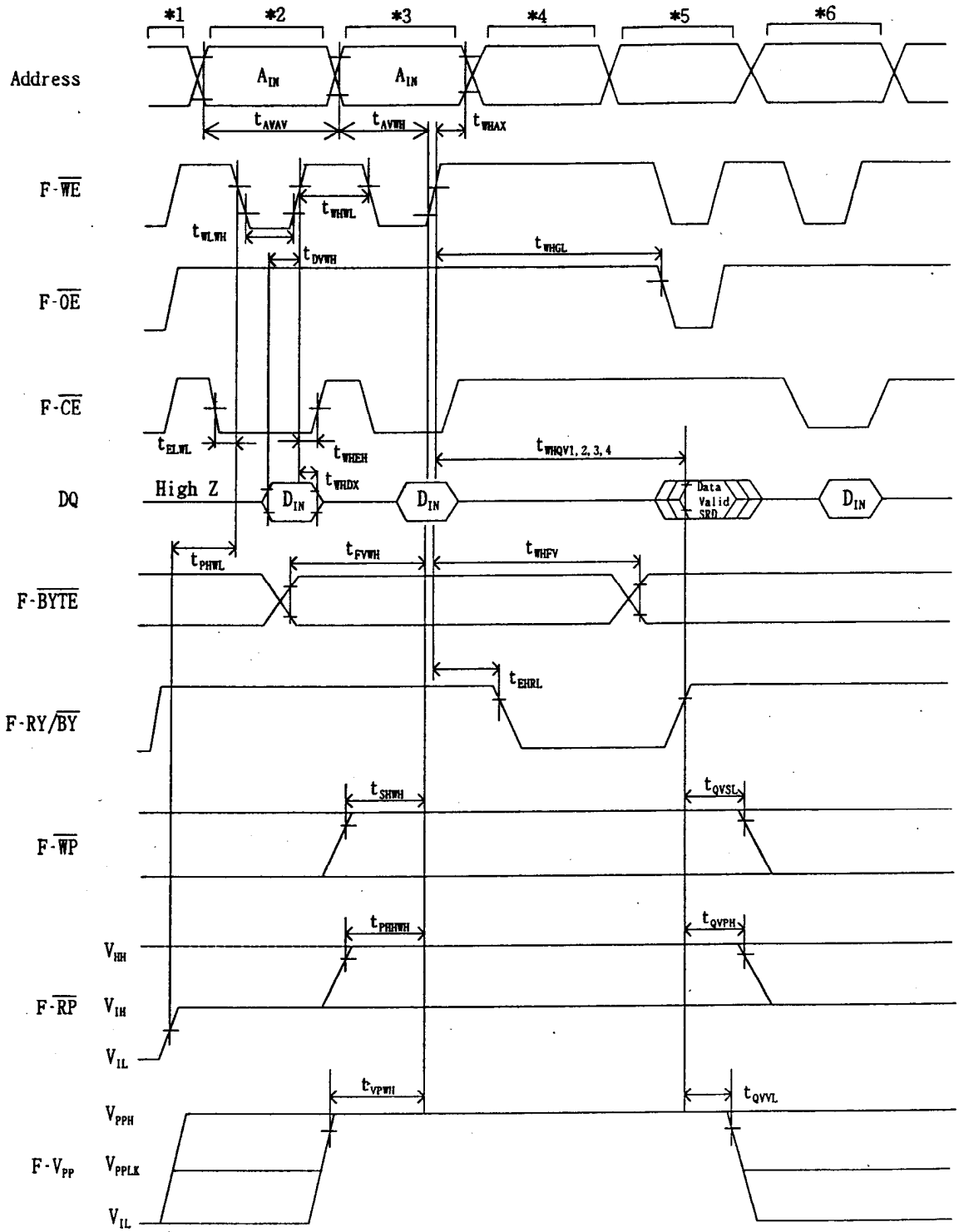
Read Cycle timing chart



F-$\overline{BYTE}$ timing Waveform



Write cycle timeng chart (F-$\overline{WE}$ controlled)



Notes:

*1. V_{CC} Power-up and standby.

*2. Write block erase or word/byte write setup.

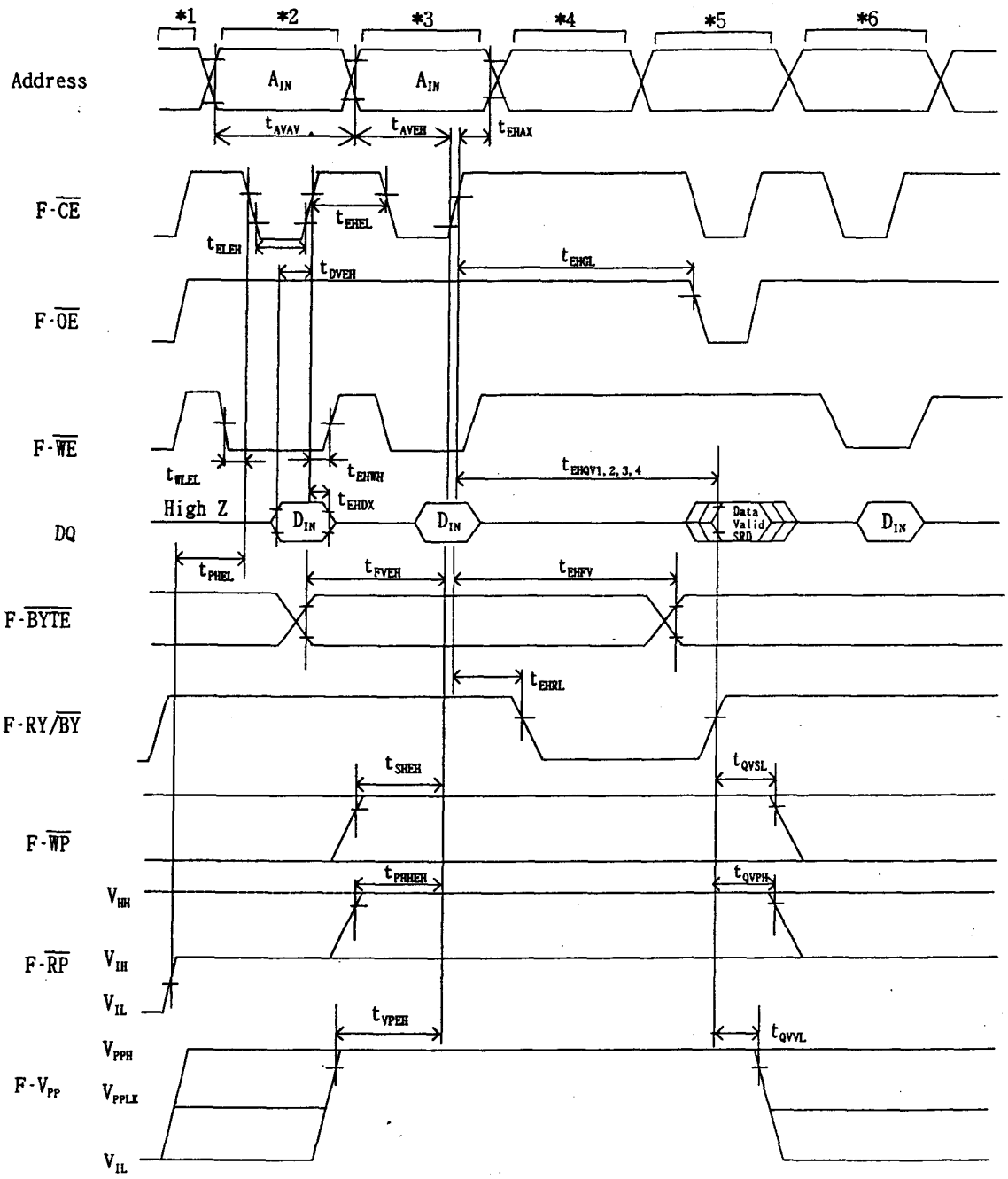
*3. Write block erase confirm or valid address and data.

*4. Automated erase or program delay.

*5. Read status register data.

*6. Write Read Array command.

Write cycle timing chart (F-$\overline{CE}$ controlled)



Notes:

*1. V_{CC} Power-up and standby.

*2. Write block erase or word/byte write setup.

*3. Write block erase confirm or valid address and data.

*4. Automated erase or program delay.

*5. Read status register data.

*6. Write Read Array command.

Reset Operations (T_a= −25℃ to +85℃, V_{CC}= 2.7V to 3.6V)

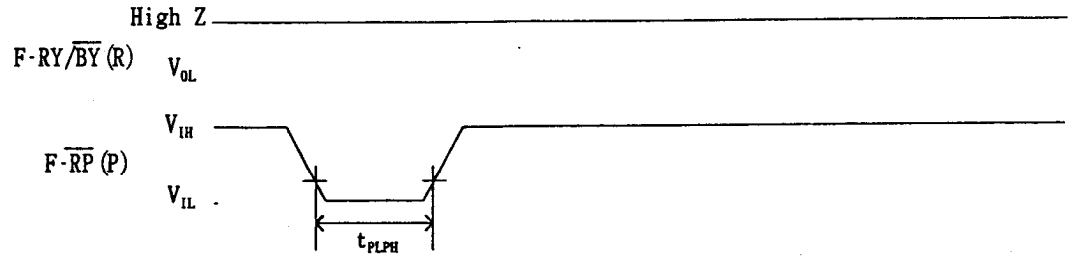
Parameter	Sym.	Min.	Max.	Unit	
F-$\overline{RP}$ Pulse Low Time (If F-$\overline{RP}$ is tied to Vcc, this specification is not applicable.)	t_{PLPH}	100		ns	
F-$\overline{RP}$ Low to Reset during Block Erase or Write	t_{PLRZ}		23.6	μs	*1, 2
F-V_{CC} 2.7V to F-$\overline{RP}$ High	t_{VPH}	100		ns	*3

Notes) *1. If F-$\overline{RP}$ is asserted while a block erase or word/byte write operation is not executing, the reset will complete with 100ns.

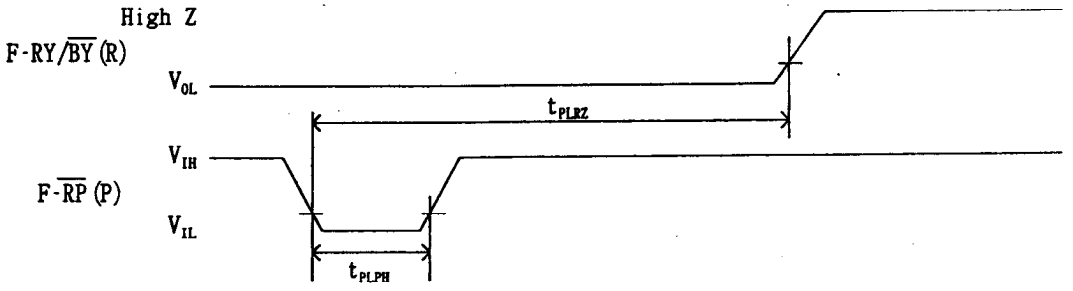
*2. A reset time, t_{PHQV}, is required from the later of F-RY/$\overline{BY}$ going High Z of F-$\overline{RP}$ going high until outputs are valid.

*3. When the device power-up, holding F-$\overline{RP}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

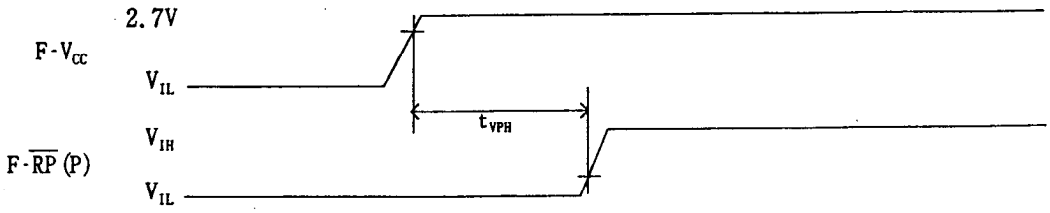
AC Waveform for Reset Operation



(A) Reset During Read Array Mode



(B) Reset During Block Erase or Word/Byte Write



(C) F-$\overline{RP}$ Rising Timing

13. SRAM AC Electrical Characteristics

SRAM AC Test Conditions

Input pulse level	0.4 V to 2.2 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.5 V
Output load	1TTL+C_L (30pF) (*1)

Note) *1. Including scope and jig capacitance.

Read Cycle

(T_a= −25 ℃ to +85 ℃ , V_{CC}= 2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t_{RC}	85		ns	
Address access time	t_{AA}		85	ns	
Chip enable access time ($S\text{-}\overline{CE_1}$)	t_{ACE1}		85	ns	
($S\text{-}CE_2$)	t_{ACE2}		85	ns	
Output enable to output valid	t_{OE}		40	ns	
Output hold from address change	t_{OH}	10		ns	
$S\text{-}\overline{CE_1}$, $S\text{-}CE_2$ Low ($S\text{-}\overline{CE_1}$)	t_{LZ1}	10		ns	*2
to output active ($S\text{-}CE_2$)	t_{LZ2}	10		ns	*2
$S\text{-}\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*2
$S\text{-}\overline{CE_1}$, $S\text{-}CE_2$ High to ($S\text{-}\overline{CE_1}$)	t_{HZ1}	-0	25	ns	*2
output in High impedance ($S\text{-}CE_2$)	t_{HZ2}	0	25	ns	*2
$S\text{-}\overline{OE}$ High to output in High impedance	t_{OHZ}	0	25	ns	*2

Write Cycle

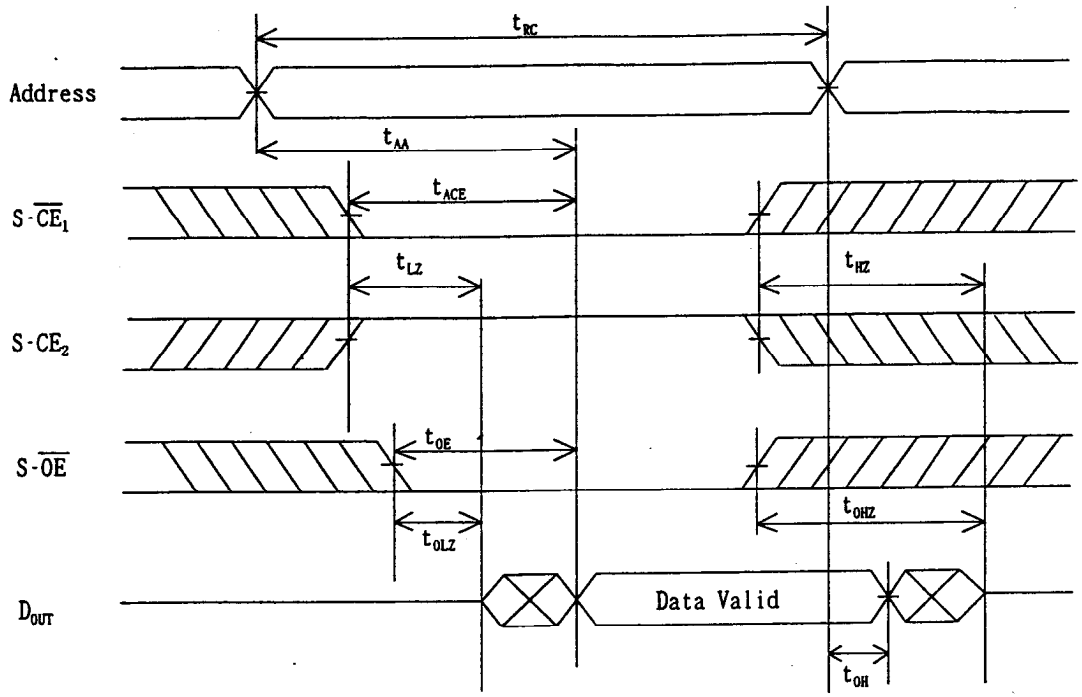
(T_a= −25 ℃ to +85 ℃ , V_{CC}=2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Write cycle time	t_{WC}	85		ns	
Chip enable to end of write	t_{CW}	70		ns	
Address valid to end of write	t_{AW}	70		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	55		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	35		ns	
Input data hold time	t_{DH}	0		ns	
$S\text{-}\overline{WE}$ High to output active	t_{OW}	5		ns	*2
$S\text{-}\overline{WE}$ Low to output in High impedance	t_{WZ}	0	25	ns	*2

*2. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

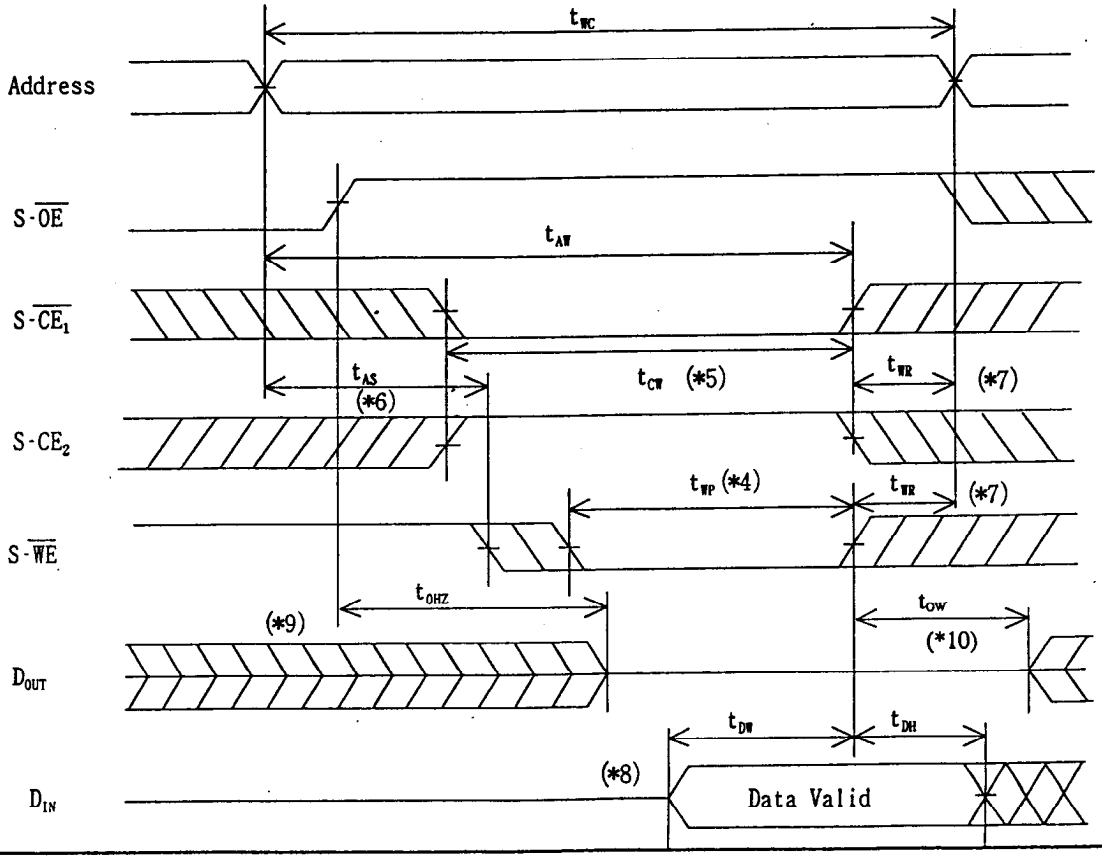
SRAM AC Charateristics Timing Chart

Read cycle timing chart — (*3)

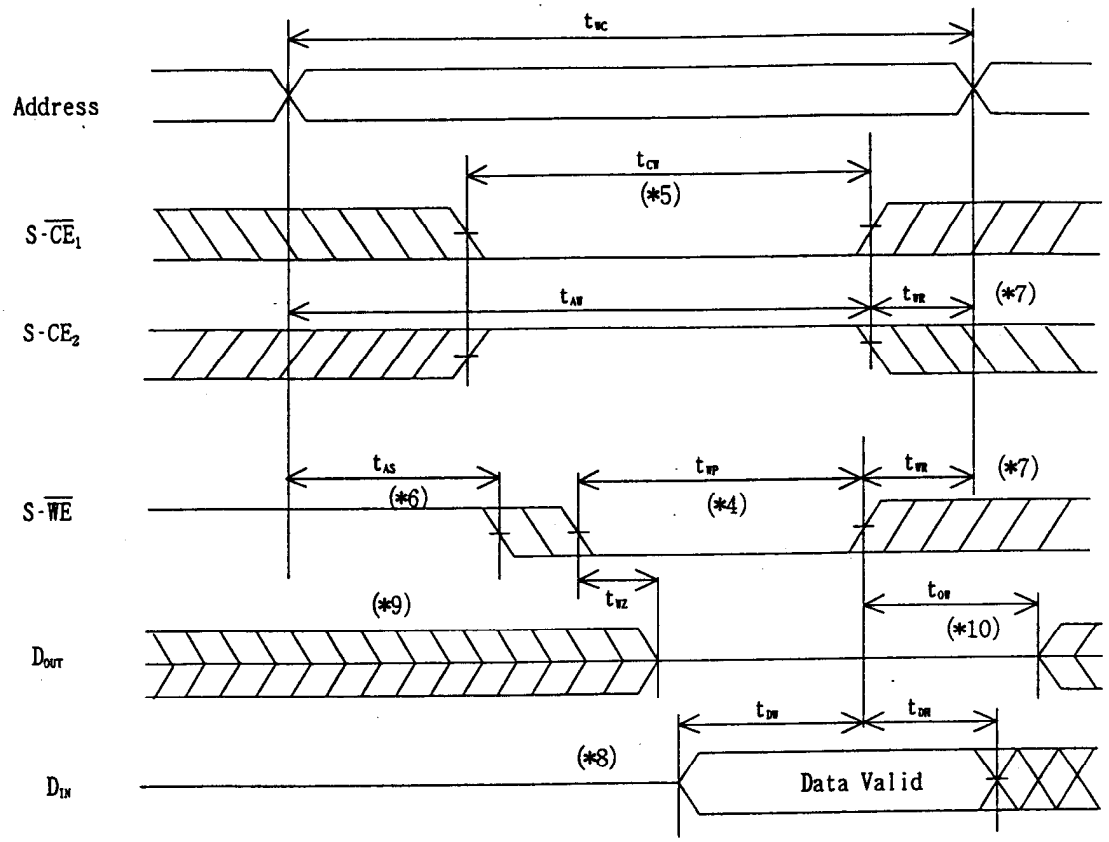


*3 S-$\overline{WE}$ is high for Read cycle.

Write cycle timing chart — (S-$\overline{OE}$ Controlled)



Write cycle timing chart — (S-$\overline{OE}$ Low fixed)



Notes)

*4. A write occurs during the overlap of a low S-$\overline{CE_1}$, a high S-CE_2 and a low S-$\overline{WE}$, A write begins at the latest transition among S-$\overline{CE_1}$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
A write ends at the earliest transition among S-$\overline{CE_1}$ going high, S-CE_2 going low and S-$\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*5. t_{CW} is measured from the later of S-$\overline{CE_1}$ going low or S-CE_2 going high to the end of write.

*6. t_{AS} is measured from the address valid to the beginning of write.

*7. t_{WR} is measured from the end of write to the address change.

*8. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

*9. If S-$\overline{CE_1}$ goes low or S-CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.

*10. If S-$\overline{CE_1}$ goes high or S-CE_2 goes low simultaneously with S-$\overline{WE}$ going high or S-$\overline{WE}$ going high, the outputs remain in high impedance state.

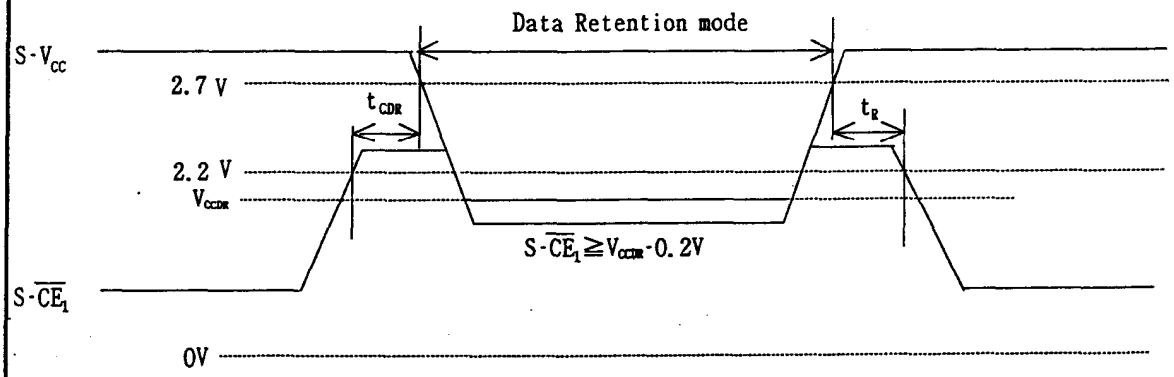
14. SRAM Data Retention Characteristics

(T_a= −25℃ to +85℃)

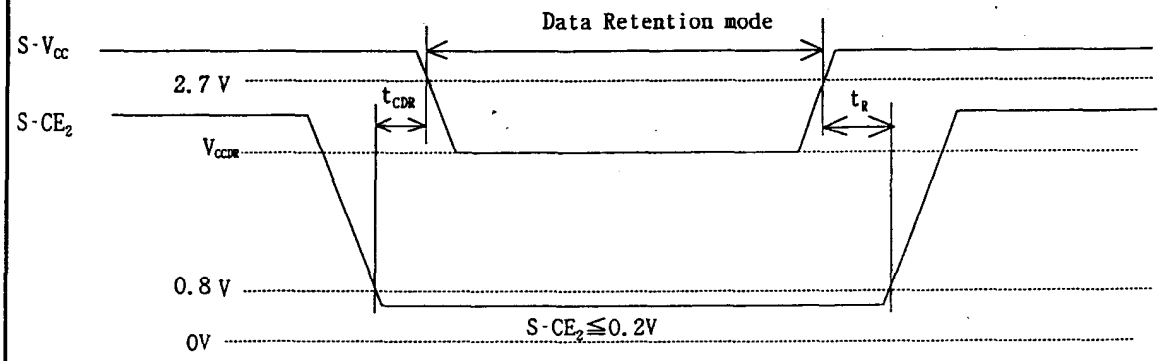
Parameter	Sym.	Conditions	Min.	Typ. (*1)	Max.	Unit
Data Retention Supply volotage	V_{CCDR}	S-CE_2 ≦0.2V or S-$\overline{CE_1}$≧V_{CCDR}-0.2V (*2)	2.0		3.6	V
Data Retention Supply current	I_{CCDR}	V_{CCDR}=3V S-CE_2≦0.2V or S-$\overline{CE_1}$ ≧V_{CCDR}-0.2V (*2)		0.2	15	μA
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		5			ms

Notes) *1. Reference value at T_a=25℃, S-V_{CC}=3.0V.
*2. S-$\overline{CE_1}$≧V_{CC}-0.2V, S-CE_2≧V_{CC}-0.2V (S-$\overline{CE_1}$ controlled) or S-CE_2≦0.2V (S-CE_2 controlled)

Data Retention timing chart (S-$\overline{CE_1}$ Controlled) (*3)



Data Retention timing chart (S-CE_2 Controlled)



Note) *3. To control the data retention mode at S-$\overline{CE_1}$, fix the input level of S-CE_2 between V_{CCDR} and V_{CCDR}-0.2V or 0V or 0.2V and during the data retetion mode.

15. Notes

This product is a stacked CSP package that a 16M(x8/x16) bit Flash Memory and a 2M (x8) bit SRAM are assembled into.

Supply Power

Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

Power Supply and Chip Enable of Flash Memory and SRAM

S-$\overline{CE_1}$ should not be LOW and S-CE_2 should not be HIGH when F-$\overline{CE}$ is LOW simulataneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

Power UP Sequence

When turning on Flash memory power supply, keep F-$\overline{RP}$ LOW. After F-V_{CC} reaches over 2.7V, keep F-$\overline{RP}$ LOW for more than 100nsec.

Device Decoupling

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F-$\overline{CE}$, S-$\overline{CE_1}$, S-CE_2).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.
Such noises, when induced onto F-$\overline{WE}$ signal or power supply may be interpreted as false commands, causing undesired memory updating.
To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block
By setting a F-$\overline{WP}$ to low, only the boot block can be protected against overwriting.
Parameter and main blocks cannot be locked.
System program, etc., can be locked by storing them in the boot block.
When a high voltage is applied to F-$\overline{RP}$, overwrite operation is enabled for all blocks.
For further information on setting/resetting of block bit, and controlling of F-$\overline{WP}$ and F-$\overline{RP}$, refer to the specification. (See 5. Command Definitions P. 5)

2) Data protection through Vpp
When the level of Vpp is lower than VPPLK (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.
For the lockout voltage, refer to the specification. (See Chapter 11. DC Characteristics P. 10)

Data protection during voltage transition
1) Data protection thorough F-$\overline{RP}$
When the F-$\overline{RP}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
For the details of F-$\overline{RP}$ control, refer to the specification. (See chapter 12. Flash Memory AC Electrical Characteristics)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1μF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit.
In case of reprogramming "0" to the data which has been programed "1".

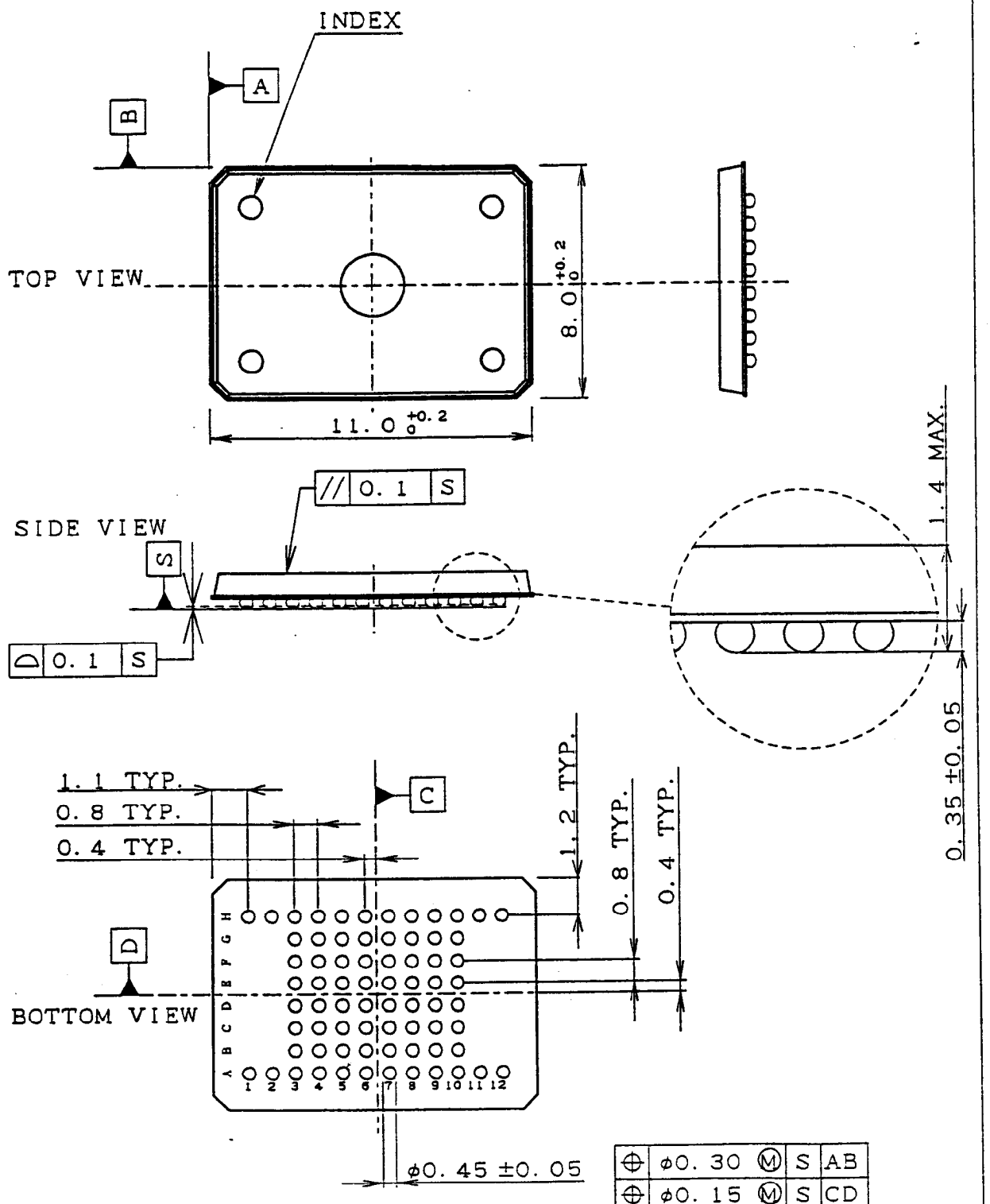
- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "1110111111111110" programming.

4. Power Supply

Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid V_{PP} (See 11. DC Characteristics) produce spurious results and should not be attempted.
Device operations at invalid Vcc voltage (see 11. DC Characteristics) produce spurious results and should not be attempted.

SHARP



改訂 DATE	改訂記事 REVISE		担当 CHARGE		
日付 DATE	1998. 2. 10				
設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE	
SOTA	SOTA				

尺度 SCALE	5/1
単位 UNIT	1=1/1mm
端子マトリクス MATRIX	12 X 8
端子数 COUNTS	72
端子ピッチ PITCH	0.8

シャープ株式会社 SHARP CORPORATION
IC天理事業本部 TENRI IC GROUP
超LSI開発研究所 VLSI DEVELOPMENT LABORATORIES
生産技術開発部 PRODUCTION ENGINEERING DEPT.

適用機種 APPLICABLE MODEL	16M FLASH MEMORY(X16B8) +2M SRAM (X8)
名称 NAME	LCSP072-P-0811 (LFBGA072-P-0811)
コード CODE	LCSP-GR-072-1 -0811
図番 DRAWING No.	AA2078