· •

SPEC No.         E L 0 7 Y 0 0 5           I S S U E:         Nov.         6. 1995
<u>To;</u>
REQUEST FOR CONFIRMATION
SPECIFICATIONS
Product TypeDrive IC (190K/220K pixels single voltage B/W CCD)
Nodel No. LZ9GG32M
· · · · · · · · · · · · · · · · · · ·
%This specifications contains <u>30</u> pages including the cover and appendix. If you have any objections, please contact us before issuing purchasing order.
CUSTONERS ACCEPTANCE
DATE:
BY: PRESENTED
BY: Husenco
X. KUSANO Dept. General Manager
REVIEWED BY: PREPARED BY:
A. Tokimo R. Yoshizawa
Engineering Dept.3 Logic IC Engineering Center
Tenri Integrated Circuits Group
SHARP CORPORATION

- Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.
- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
  - (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
    - Office electronics
    - •Instrumentation and measuring equipment
    - •Machine tools
    - •Audiovisual equipment
    - •Home appliances
    - •Communication equipment other than for trunk lines
  - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
    - •Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
    - •Mainframe computers
    - •Traffic control systems
    - •Gas leak detectors and automatic cutoff devices
    - Rescue and security equipment
    - •Other safety devices and safety equipment, etc.
  - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
    - •Aerospace equipment

e de s

- •Communications equipment for trunk lines
- •Control equipment for the nuclear power industry
- •Medical equipment related to life support, etc.
- (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

Please direct all queries regarding the products covered herein to a sales representative of the company.

### L Z 9 G G 3 2 M

1

·

### CONTENTS

<ol> <li>General         <ol> <li>Features             </li> <li>Functions</li> </ol> </li> </ol>	·····	P. 2
2. Pin Assignment	••••••	P. 3
3. Block Diagram	••••••	P. 4
4. Pin Description	••••••	P. 5
5. Electrical Characteria 5-1. Absolute Maximum Ra 5-2. DC Characteristics	stics •••••• atings	P: 11
6. Pulse Timing	•••••	P. 12
7. Package Outline	• • • • • • • • • • • • • • • • • • • •	P. 25

1. General

The LZ9GG32M is a CMOS gate array LSI. It generates timing pulses for driving a CCD area sensor, and synchronous pulses for TV signals and processing pulses for video signals.

1-1. Features

- \* The package material is plastic.
- \* A p-type silicon circuit board is used.
- \* The package type is 48-pin QFP (0.5mm pin-pitch)
- \* The process (structure) is CMOS.
- \* The delay time per 1 gate is 0.9ns.
- \* Not designed or rated as radiation hardened.

1-2. Functions

. i .

\* Designed for single +5V power supply CCD monochrome area sensor with 190,000 or 220,000 pixels on 1/5 inch size. \*Switchable between EIA and CCIR mode. \*Single +5V power supply. \*Electronic shutter or EE control is possible.

#### LZ9GG32M

2. Pin Assignment

PIN NO.	1/0	SIGNAL	PIN NO.	I/0	SIGNAL
1	ICD	TST1			
	· · · · · · · · · · · · · · · · · · ·		25	ICU	EEST
2	ICSU	VINT	26	0	WIND
3	ICSU	VRI	27	0	OFDX
4	ICU	TVMD	28	06MA2	V 1
5	0	CSYN	29	06MA2	V 2
6	-	V D D	30	—	V D D
7	_	GND	31	-	GND
8	0	CBLK	32	06MA2	V 3
9	0	H D	33	06MA2	V 4
10	0	V D	34	0 6 M A	VTGX
11	0	HBLK	35	0 6 M A	OFD
12	0	PBLK	36	0 6 M A	LOFX
13	0	ВСР	37	ΙC	FCDI
14	ICD	TST2	38	06MA2	FCDO
15	ΙCD	TST3	39	ΙC	FSI
16	0	FΙ	40	06MA2	FSO
17	ICU	ACLX	41	O 6 M A 3	FR
18	ICU	SLBK	42	06MA3	F H ~ 2
19	ICU	FLMD	43		GND
20	ICU	EEMD	44	06MA3	FH1
21	ΙC	EEUD	4 5	ICD	TST4
22	ΙC	EENR	46	OSCI	СКІ
23	06MA2	FCDS	47	OSCO	СКО
24	06MA2	F S	48	ICU	NINT

I C : Input (CMOS level)

I C U : Input (CMOS level with pull-up resister)

I C S U : Schmitt-trigger Input (CMOS level with pull-up resister)

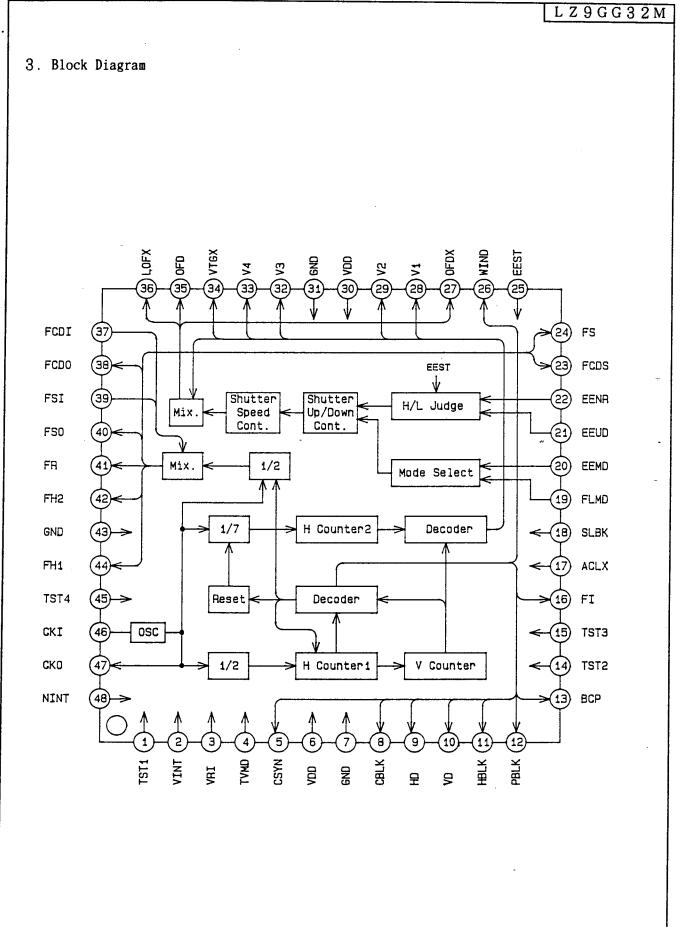
I C D : Input (CMOS level with pull-down resister)

- O : Output
- O 6 M A : Output
- $O\,\,6\,M\,A\,\,2\,\,:\,0 \text{utput}$
- O 6 M A 3 : Output

- OSCI : Input pin for oscillation
- OSCO : Output pin for oscillation

• <sup>11</sup> 2

L Z 9 G G 3 2 M



•

L Z 9 G G 3 2 M

LZ9GG32M

4. Pin Description

TST1 VINT VRI	ICD ICSU ICSU		Test terminal 1 Initialize input Vertical reset input	A test pin. Set open or to L level in the normal mode. An input pin for initializing circuit. It can be used Field-reset input, and the circuit is initialized with the 1/2 dividing pulse of VINT. The frequency of VINT is 60Hz in EIA or 50Hz in CCIR. It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced, at EIA mode, 0~148ns from the start of 0DD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay from ver. sync. start point, because VRI is
	-		input Vertical	An input pin for initializing circuit. It can be used Field-reset input, and the circuit is initialized with the 1/2 dividing pulse of VINT. The frequency of VINT is 60Hz in EIA or 50Hz in CCIR. It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced. at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
	-		input Vertical	It can be used Field-reset input, and the circuit is initialized with the 1/2 dividing pulse of VINT. The frequency of VINT is 60Hz in EIA or 50Hz in CCIR. It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced. at EIA mode, 0~148ns from the start of 0DD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU		Vertical	<pre>is initialized with the 1/2 dividing pulse of VINT. The frequency of VINT is 60Hz in EIA or 50Hz in CCIR. It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced. at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay</pre>
VRI	ICSU			VINT. The frequency of VINT is 60Hz in EIA or 50Hz in CCIR. It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced. at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU			50Hz in CCIR. It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced, at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU			It may be occured jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced. at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU	-		<pre>pulse with the 1/2 dividing pulse of CKI(pin 46). The point of resetting is following, the trailing edge of VINT is advanced, at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay</pre>
VRI	ICSU	-		The point of resetting is following, the trailing edge of VINT is advanced, at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU			<pre>edge of VINT is advanced, at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay</pre>
VRI	ICSU	-		at EIA mode, 0~148ns from the start of ODD field at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU	-		at CCIR mode, 0~148ns from the start of 1st field Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU	-		Set open or H level when internal sync. mode or no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU	-		no intilizing. An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VRI	ICSU	-		An input pin for resetting internal Ver. counter. The input pulse ic necessary 1/2 Hor. max delay
VKI	1030			The input pulse ic necessary 1/2 Hor. max delay
			reset input	· · · · ·
				from ver. sync. start point, because var is
				counted 2 times Hor. frequency.
				The point of resetting is following,
				at EIA mode, 3.5H from the start of VD,
				at CCIR mode, 3H from the start of VD.
	Ì			Set open or H level when internal sync. or using
				VINT(pin 2).
TVND	ICU	-	TV mode select	An input pin to select TV standards.
	[			L level; EIA mode
				H level or open; CCIR mode
CSYN	0	υŢ	Composite	Composite sync. signal output pin.
			syncronizing	
			pulse	
VDD	-			Supply +5 V power.
GND		_		A grounding pin.
CBLK	0		- 1	Composite blanking pulse.
			-	When SLBK(pin 18) is L level,
			pulse	at EIA mode ; H:10.52ns, V:20H period,
				at CCIR mode ; H:11.26ns, V:25H period.
				When SLBK(pin 18) is H level,
				at EIA mode ; H:10.81ns, V:20H period,
HD	0	$\frac{1}{n}$	Hor drive	at CCIR mode ; H:12.15ns, V:25H period.
	Ĭ		1	The pulse occurs at the start of lines.
VD	0			The pulse occurs at the start of every fields.
· • 1	Ĭ	_		the purse occurs at the start of every fields.
H	/DD IND IBLK	/DD – ND – CBLK O	/DD     -     -       ND     -     -       SBLK     0     1       D     0     1	Image: Syncronizing pulse       /DD     -       /D     0       /D     0       /D     0       /D     0       /D     0

٠

-

### L Z 9 G G 3 2 M

LZ9GG32M

No.		_		Pin Name	Description				
11	HBLK	0	1	Hor. blanking	A pulse that correspondes to the cease period of				
		L		pulse	the Hor. transfer pulse.				
12	PBLK	0		Pre-blanking	Equivalent to CBLK(pin 8) pulse except for short				
				pulse	pulse width with cut-off trailing edge.				
13	BCP	0	Л	Optical	A pulse to clamp the optical black signal.				
				black clamp	This pulse stays low during the absence of				
				pulse	effective pixels within the ver. blanking.				
14	TST2	ICD	-	Test terminal 2	A test pin. Set open or to L level in the normal				
					mode.				
15	TST3	ICD	-	Test terminal 3	A test pin. Set open or to L level in the normal				
					mode.				
16	FI	0		Field index	The pulse is used for detecting field.				
					at EIA mode ; ODD field : LOW				
	i				EVEN field : HIGH				
					at CCIR mode ; 1st and 3rd fields : LOW				
17		TOU		411 1	2nd and 4th fields : HIGH				
17 18	ACLX SLBK	ICU		All clear input	An input pin for resetting all internal circuit.				
10	SLDV	ICU	-	CBLK width	An input pin to select the Hor. period of CBLK.				
				select	L level; at EIA mode ; H:10.52ns, V:20H perio				
- 1					at CCIR mode ; H:11.26ns, V:25H period				
					H level; at EIA mode ; H:10.81ns, V:20H period				
					or open at CCIR mode ; H:12.15ns, V:25H perio				
19	FLND	ICU	_	Flickerless	at power on.				
13	I LMD	100		select	An input pin to select Flickerless shutter mode,				
20	EEMD	ICU	_	Electronic	with using EEMD(pin 20). An input pin to select Electronic Exposure mode,				
20	DEMD	100			with using FLMD(pin 19).				
1				DAPOSUIC SCICCU	FLMD EEND Shutter speed(s)				
					EIA CCIR				
					L L $1/60$ $1/50$				
i					$\begin{array}{c c c c c c c c c c c c c c c c c c c $				
	ĺ				L H 1/31, 320max 1/30, 890max				
					H H 1/109, 890max 1/109, 890max				
21	EEUD	IC	-1	Electronic	An input pin to control Electronic Exposure, with				
			[	Exposure	using EENR(pin 22).				
				control 1	<b>- · · · · · · · · · ·</b>				
22	EENR	IC	- 1	Electronic	An input pin to control Electronic Exposure, with				
				Exposure	using EEUD(pin 21).				
				control 2					
23		06MA2	Л	CDS pulse 1	A pulse to clamp the feed-through level from CCD.				
24		06MA2	ΓŢ	CDS pulse 2	A pulse to sample-hold the signal from CCD.				
25	EEST	ICU	- T	Electronic	An input pin to control Electronic Exposure, with				
	Í			Exposure	using EEUD(pin 21) and EENR(pin 22).				
				control 3	L level : Electronic Exposure is stopped.				
		·			H level or open : Electronic Exposure is				
	1								

6

,

.

• · · ·

### L Z 9 G G 3 2 M

LZ9GG32M

No.	Symbo1		Po1	· · · · · · · · · · · · · · · · · · ·	Description			
26	WIND	0	11	Wind pulse	A pulse for wind pulse. When connected to EEST(pi			
	ĺ				38), the operation of Electronic Exposure can be			
					stopped at the upper side of monitor.			
27	OFDX	D6MA	L L	Inverse OFD	A pulse that is used for pulse additinal circuit			
				PULSE output	of electronic shutter.			
28	<b>V</b> 1	D6MA2	T	Ver. transfer				
		1		pulse 1	Connect to \$V1 pin of CCD.			
29	V2	D6MA2	J	Ver. transfer	A vertical transfer pulse for CCD.			
				pulse 2	Connect to $\phi V2$ pin of CCD.			
30	VDD	-	-	Power supply	Supply +5 V power.			
31	GND	-	-	Ground	A grounding pin.			
32	V3	D6MA2	In	Ver. transfer				
	:			pulse 3	Connect to \$V3 pin of CCD.			
33	<b>V</b> 4	D6MA2	П	Ver. transfer	A vertical transfer pulse for CCD.			
		1		pulse 4	Connect to $\phi V4$ pin of CCD.			
34	VTGX	D6MA	חר	Read out	A pulse that transfers the charge of the			
				pulse	photodiode to the vertical shift resister.			
i				pullo	Connect to \$TG pin of CCD.			
35	OFD	D6MA	Л	OFD pulse				
	01 D	00mm	1	output	A pulse that sweeps the charge of the photodiode			
	·			οαιμαί	for electronic shutter. Connect to OFD pin of CCD			
36	LOFX	D6MA	1	LOFX pulse	through the D.C. offset circuit.			
30	LOFA	DOWN	U		A last pulse that sweeps the charge of the			
				output	photodiode for electronic shutter.			
37	FCDI	IC		ECDC -1	Connect to LOFX pin of CCD.			
31	rcDi		-	FCDS phase	Pins to control the phase between FH1(pin 44) and			
20	ECDO	00110		control input	FCDS(pin 23).			
38	FCDO	D6MA2	-	FCDS phase	A pulse to control pulse timing of FCDS, connect			
20	Pot	TO		control output				
39	FSI	IC	-	FS phase	Pins to control the phase between FH1(pin 44) and			
	Foc			control inout	FS(pin 24).			
40	FS0	06MA2	-	FS phase	A pulse to control pulse timing of fs, connect to			
-		0.011 - 0		control output	FSI(pin 39) pin through the CR ddelay circuit.			
41	FR	06NA2	JL	Reset pulse	A reset pulse for CCD.			
					Connect to $\phi RS$ of CCD through the D.C. offset			
					circuit.			
42	FH2	OGMA3	Ul	Hor. transfer	A horizontal transfer pulse for CCD.			
_				pulse 2	Connect to #H2 of CCD.			
43	GND	-	-	Ground	A grounding pin.			
14	FH1	D6MA3	ЛГ	Hor. transfer	A horizontal transfer pulse for CCD.			
				pulse 1	Connect to #H1 of CCD.			
15	TST4	ICD	- 1	Test terminal 4	A test pin. Set open or to L level in the normal			
					mode.			

7

: •

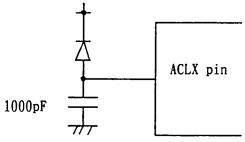
### L Z 9 G G 3 2 M

LZ9GG32M

No.	Symbol	I/0		Pin Name	Description
46	CKI	OSCI	Л	Clock input	An input pin for reference clock oscillation.
					The frequencies are as follows :
					at EIA mode : 13.500MHz (858fH)
					at CCIR mode : 13.500MHz (864fH)
					fH=Hor. frequency
47	CKO	0SC0	Ul	Clock output	An output pin for reference clock oscillation.
					The output is the inverse CKI(pin 46).
48	NINT	ICU	-	Non-interlace	An input pin to select non-interlace mode.
				select	L level : Interlace mode
					H level or open : Non-interlace mode
					At non-interlace mode, the field is ODD field and
	· · · ·				262H period at EIA mode, and 1st field and 312H
					period at CCIR mode.

9

4-2. How to use ACLX pin.



4-3. Fixed shutter mode

۰<sup>1</sup> -

	FLMD	Shutter speed (s)			
(pin 20)	(pin 19)	EIA	A	СС	IR
L	L	appro.	1/ 60	appro.	1/ 50
L	H	appro.	1/ 100	appro.	1/ 120

4-4. Electoronic Exposur control

EEMD		Start shutter speed (s)		
(pin 20)	(pin 19)	EIA	CCIR	
H	L	1/ 31,320max	1/ 30,890max	
Н	Н	1/109, 890max	1/109, 890max	

E E M D (pin 20)		E E U D (pin 21)		Electoronic Exposur control
H	H	H	(piii 22) L	Shutter speed up
Н	Н	Н	H	Control stopped
Н	Н	L	Н	Shutter speed down
Н	L	×	×	Control stopped

2 6 7 2

### L Z 9 G G 3 2 M

### LZ9GG32M

-5.	Shutter speed c	hanges at Electoror	ic E	xposure control	
	E	ΙΑ		CC	
	Charge time	Shutter speed	1	Charge time	Shutter speed
0		≒1/ 60s	0	322H, 323H	⇒1/ 50s
1	252H+0. 209H	≒1/ 62s	1	302H+0. 207H	$\Rightarrow 1/52s$
	( by 10H ste	p )	1	( by 10H ste	
18		≒1/ 191s	23	82H+0. 207H	≒1/ 190s
19		≒1/ 218s	24	72H+0. 207H	≒1/ 216s
20		≒1/ 231s	25	68H+0. 207H	≒1/ 230s
	( by 4H step	)		( by 4H step	)
29	32H+0. 209H	≒1/ 490s	34	32H+0. 207H	≒1/ 485s
30	28H+0. 209H	≒1/ 560s	35	28H+0. 207H	≒1/ 555s
31	26H+0. 209H	≒1/ 600s	36	26H+0. 207H	≒1/ 595s
	( by 2H step	)		( by 2H step	
36	16H+0. 209H	≒1/ 970s	41	16H+0. 207H	≒1/ 965s
37	14H+0. 209H	≒1/ 1,110s	42	14H+0. 207H	≒1/ 1,100s
38	13H+0. 209H	≒1/ 1,190s	43	13H+0. 207H	≒1/ 1,180s
	( by 1H step	)	1	( by 1H step	
43	8H+0. 209H	= 1/ 1, 920	48	8H+0. 207H	≒1/ 1,900s
44	7H+0. 209H	<b>≒</b> 1/ 2, 180	49	7H+0. 207H	≒1/ 2,170s
45	6. 5H+0. 209H	<b>≒</b> 1/ 2,350	50	6. 5H+0. 207H	≒1/ 2,335s
L	( by 0.500H s			( by 0.500H	
49	4. 5H+0. 209H	≒1/ 3.360s	54	4. 5H+0. 207H	≒1/ 3, 330s
50	4H+0. 209H	≒1/ 3,740s	55	4H+0. 207H	≒1/ 3,715s
51	3. 75H+0. 209H	≒1/ 3.980s	56	3. 75H+0. 207H	≒1/ 3,960s
	( by 0.250H s	tep )		( BY 0.250H	
61	1.25H+0.209H	≒1/11,040s	66	1. 25H+0. 207H	≒1/10, 930s
62	1H+0. 209H	≒1/13,020s	67	1H+0. 207H	≒1/12,945s
63	0.875H+0.209H	≒1/14,600s	68	0.875H+0.207H	≒1/14,500s
	( by 0.125H s			( by 0.125H	
69	0. 294H	≒1/53,360s	69	0. 300H	≒1/52, 120s
70	0. 209H	≒1/75, 420s	75	0. 207H	≒1/75, 420s
71	0. 151H	≒1/103, 850s	76	0.150H	≒1/103,850s

10

•

 $L\ Z\ 9\ G\ G\ 3\ 2\ M$ 

5. Electorical Characteristics

#### 5-1. Absolute Maximum Ratings

Parameter	Symbo1	Rating	Unit
Supply voltage	V dd	$-0.3 \sim 6.0$	V
Input voltage	V I	$-0.3 \sim V_{DD}+0.3$	V
Output voltage	V o	$-0.3 \sim V_{DD} + 0.3$	V
Operation temperature	Topr	$-20 \sim +70$	°C
Storage tempetature	Tstg	$-55 \sim +150$	°C

5-2. DC Characteristics

 $(V_{DD} = +5V \pm 10\%, T_{opr} = -20 + 70\%)$ 

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	V IL				1.5	V	1
Input "High" voltage	VIH		3.5			V	1
Input "High"	V <sub>T +</sub>				3.7	V	2
Input "Low"	V т -		1.0			V	1
Hysterisis voltage	$V_{T+} - V_{T-}$		0.2			V	1
Input "Low" current	$ I_{IL1} $	$V_{I} = 0 V$			-1.0	μΑ	3
	I 1 L 2	$V_{I} = 0 V$	8.0		75	μA	+
Input "High" current		$V_I = V_{DD}$			1.0	μΑ	2,5
	I I H2	$V_{I} = V_{DD}$	8.0		75	μΑ	
Output "High" voltage	V <sub>oH1</sub>	$I_{oH} = -2mA$	4.0			V	7
Output "Low" voltage	V <sub>ol1</sub>	$I_{ol} = 4mA$			0.4	V	
Output "High" voltage	V <sub>oH2</sub>	$I_{OH} = -3mA$	4.0			v	8
Output "Low" voltage	V <sub>OL2</sub>	$I_{ol} = 4mA$			0.4	v	
Output "High" voltage	V <sub>OH2</sub>	$I_{OH} = -6 m A$	4.0			V	9
Output "Low" voltage	V <sub>OL2</sub>	$I_{oL} = 8 m A$			0.4	v	
Output "High" voltage	V <sub>онз</sub>	$I_{oH} = -9mA$	4.0			V	10
Output "Low" voltage	V ol 3	$I_{oL} = 12 \text{m A}$			0.4	V	

Note1 : Applied to Inputs(IC, ICD, ICU, OSCI).

Note 2 : Applied to Inputs(ICSU).

Note 3 : Applied to Inputs(IC, ICD, OSCI).

Note 4 : Applied to Input(ICU).

· · · ·

Note 5 : Applied to Inputs(IC, ICU, OSCI).

Note6 : Applied to Input(ICD).

Note 7 : Applied to (0,0SCO).

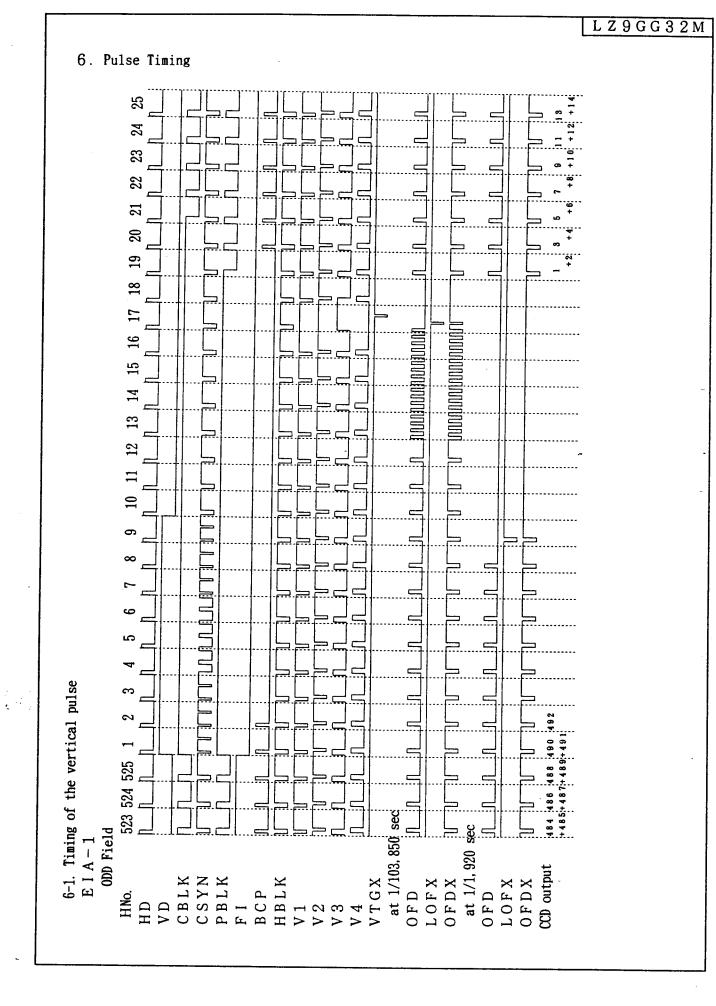
(Output(OSCO) measures on conditions that input(OSCI) level is OV or  $V_{\text{DD.}}$  )

Note 8 : Applied to Output(06MA).

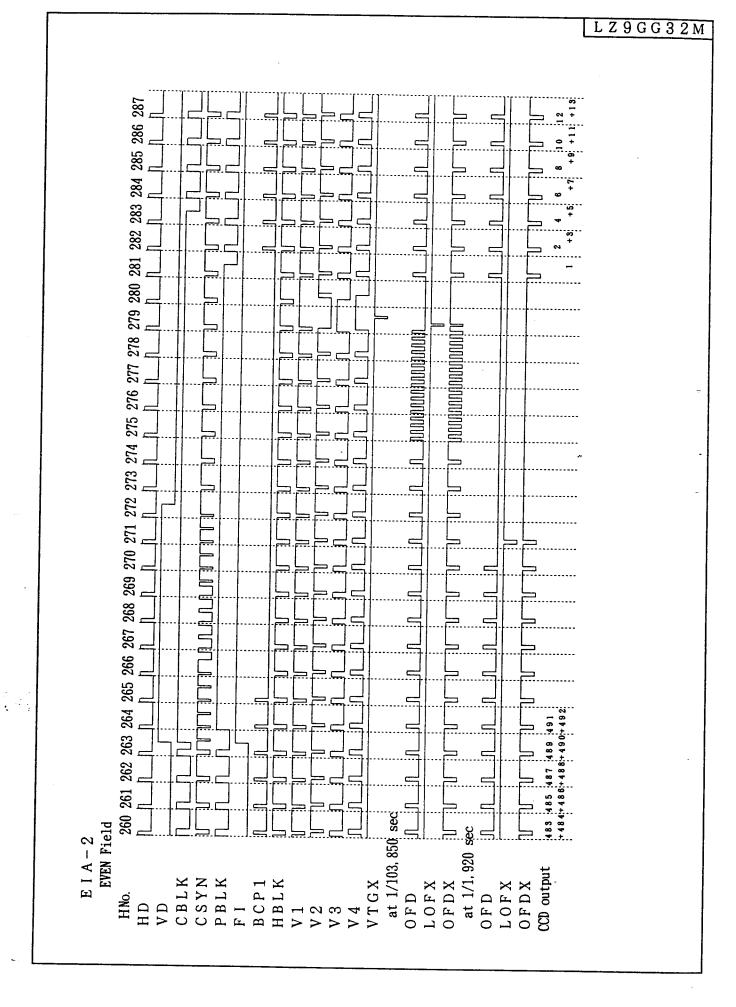
Note 9 : Applied to Output(06MA2).

Note1 0 : Applied to Output(06MA3).

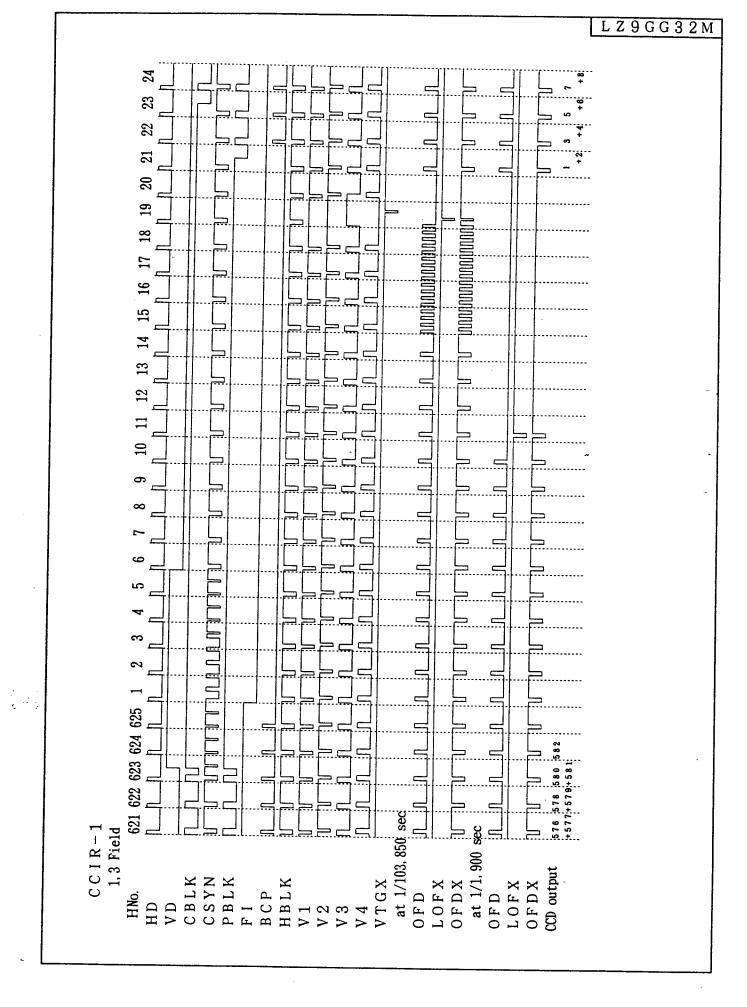
#### L Z 9 G G 3 2 M



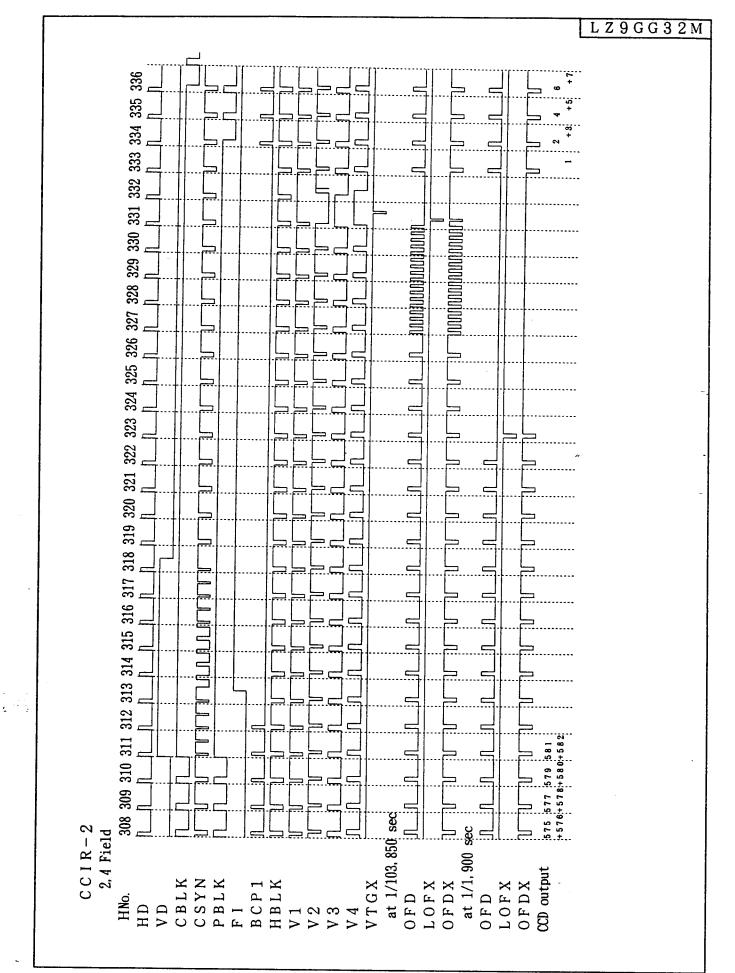
· -•

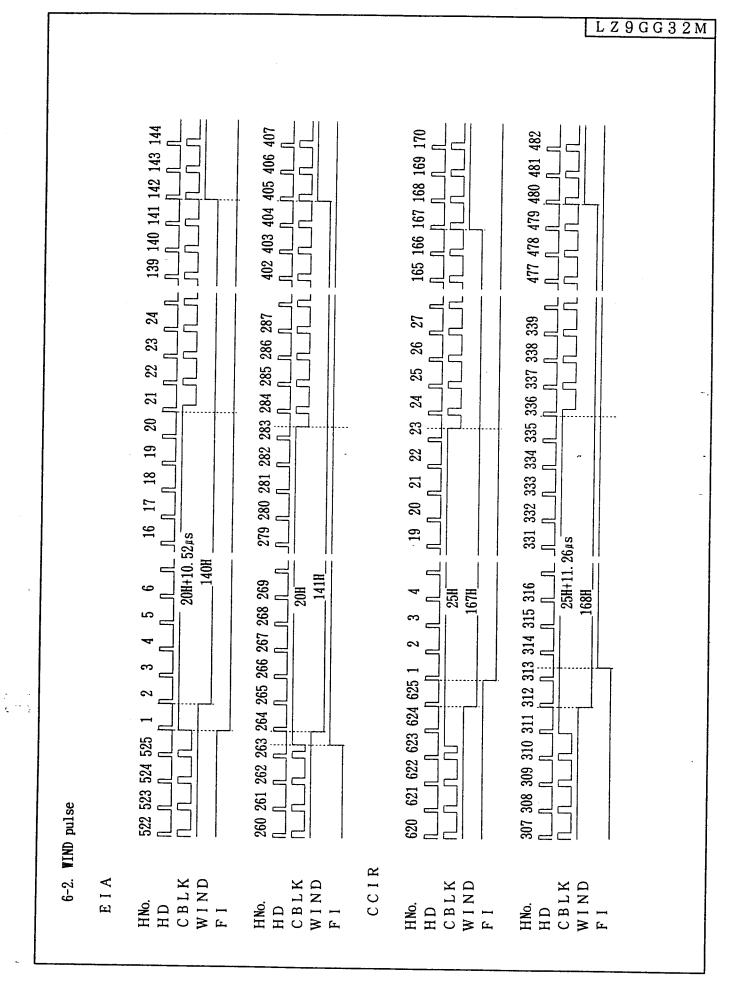


### L Z 9 G G 3 2 M



### L Z 9 G G 3 2 M





L Z 9 G G 3 2 M

110					
Timing of the Fast pulse (1) 858,0 14 30 38 40 47 54 61 75 82 86 89 96 99 110					
1ck=74. 07ns 96 99					
1ck					
86 89 000000000000000000000000000000000000					
82 82					
75 000100			Ţ		
61 החחחח					
54 1000011					"
47 100000					
38 40 Duhuhan					
38 38					<b>.</b>
30 30					
uuuu uuuuu					
t puls 14					
le Fas					
ig of th 858, 0 0000000		59 362081 วันในปันโนโนโนโนโนโนโนโนโน มันโนโนโนนโนโนโนโนโนโนโนโนโนโนโนโนโนโนโน	·		
Timing of the Fast pulse (1) 858,0 14		359 362081 1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1			
6-4. Timin E I A (1) I [UUU00	HD CBLK - PBLK - FH1   FH2	FR FCDS V1 I	V 2 V 3 V 4 O F D	UCFX LOFX OFDX BCP HBLK	-

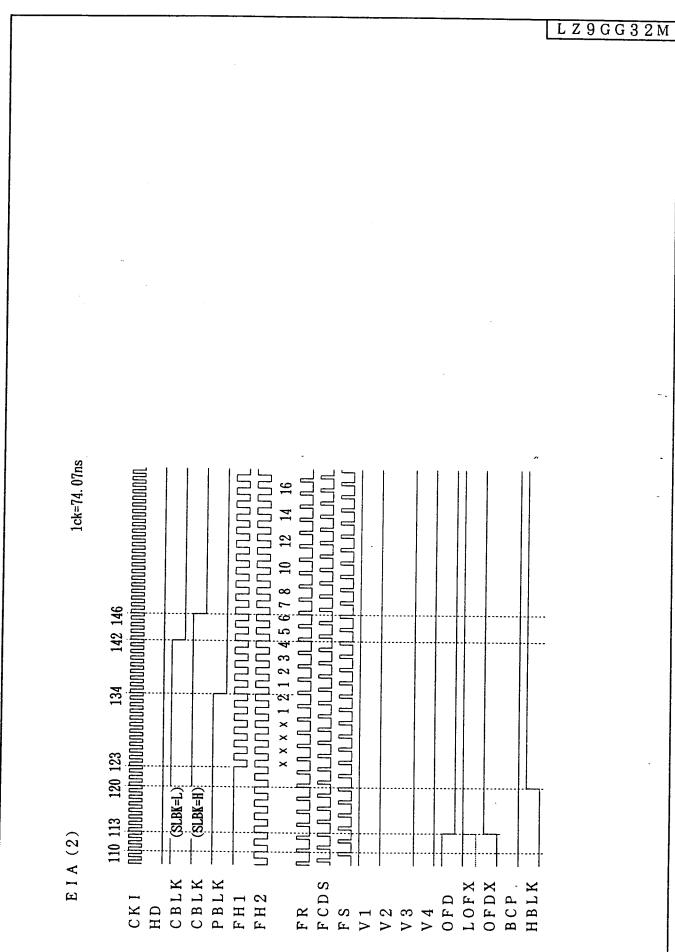
3

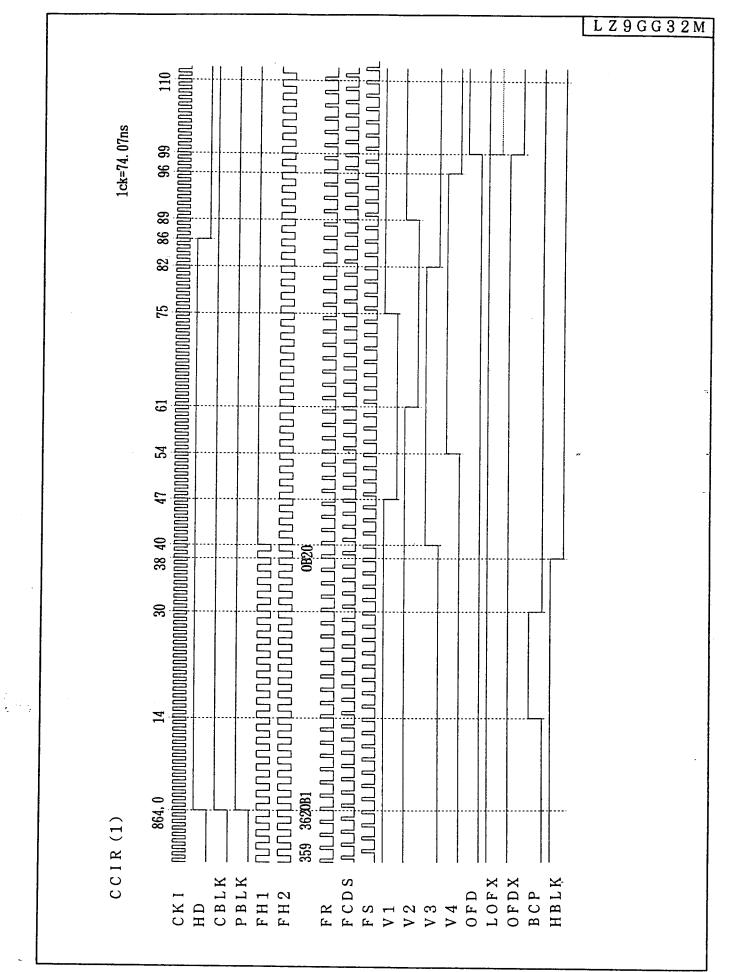
### L Z 9 G G 3 2 M

17

. . .

#### L Z 9 G G 3 2 M



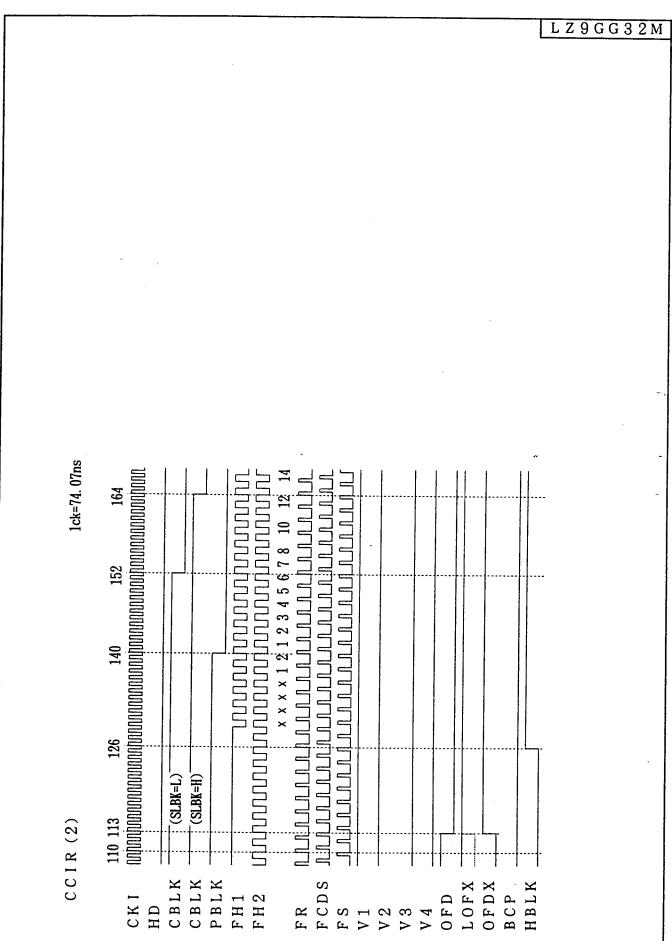


L Z 9 G G 3 2 M

. ,

•

#### L Z 9 G G 3 2 M



,

LZ9GG32M

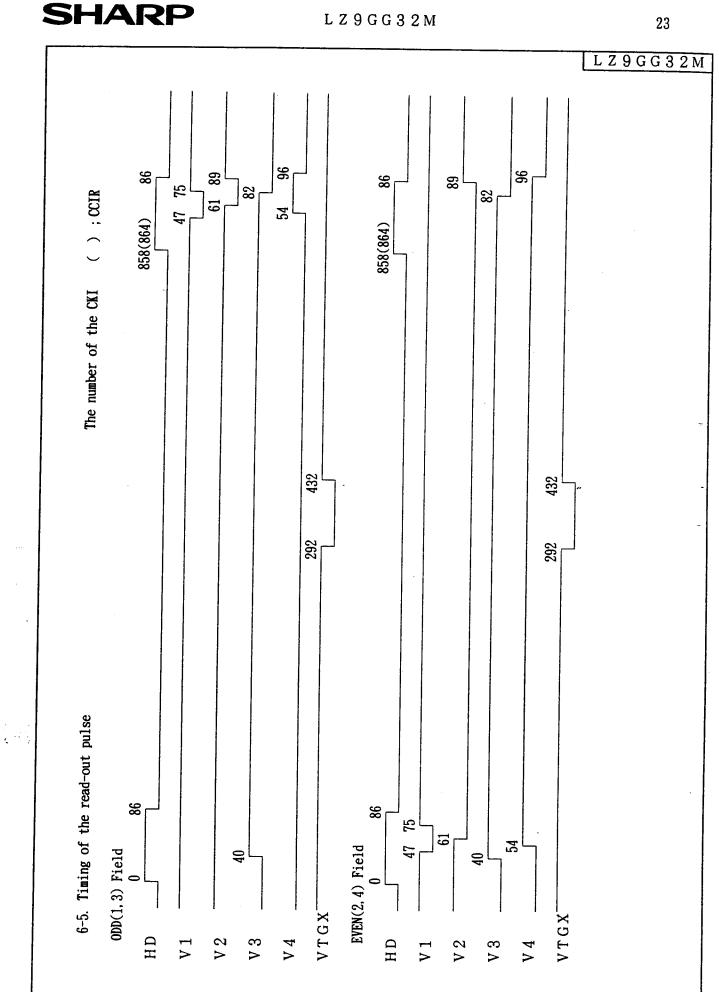
		Unit;µs (	); Number of the CKI
HD	0. 858	6. 37(86)	
CSYN H	1. 48(20)	6. 37(86)	
EQ	1. 48(20) 3	. 93(53)	
-3	. 41(-46) 1. 48(20)	J	
SAW			10. 52(142)
C B L K (SLBK=L)	0		10. 81(146)
C B L K (SLBK=H)	0	9	93(134)
P B L K	1. 04(14) 2. 22(30		7
ВСР	2. 81(38		<i>*</i>
HBLK			(20)
0(858	31.7	78(429)	63. 56(858)
V D (ODD74-146)			
V D (EVEN74-14K)		¥	
	······································	/:\	

н. . Э

LZ9GG32M

			Unit;µs	( ); Numb	er of the CKI
HD	0, 8	864	6. 37(86)		
CSYN H		1. 48(20)	6. 37(86)	······································	
EQ	······	1. 48(20) 3. 93	3(53)		
	. 41(-46)	1. 48(20)			
C B L K (SLBK=L)	0			11.	26(152)
C B L K (SLBK=H)	0		<u> </u>		12. 15(164)
PBLK	0			10. 37(140)	)
BCP	1. 0	4(14) 2.22(30)		L	
HBLK		2. 81(38)		9. 33(126)	
HD VD(1, 374-MK)	1)	32.00(	432)		64. 00(864)
VD(2,471-NK)	······································			······································	·····
				۰ ۱	
				,	

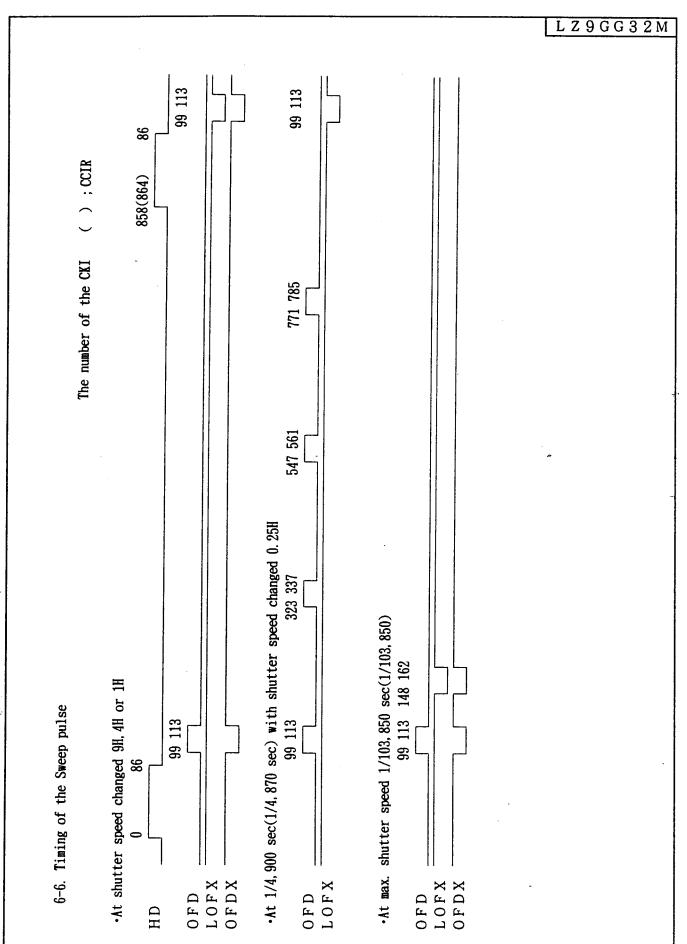
22



.

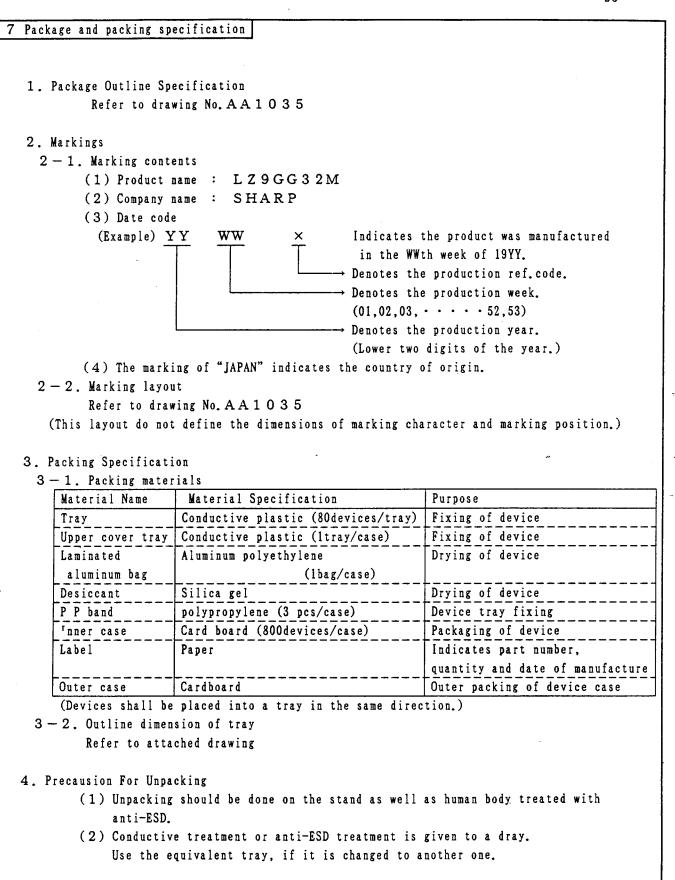
LZ9GG32M

•



L Z 9 G G 3 2 M

¢,



.

5. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

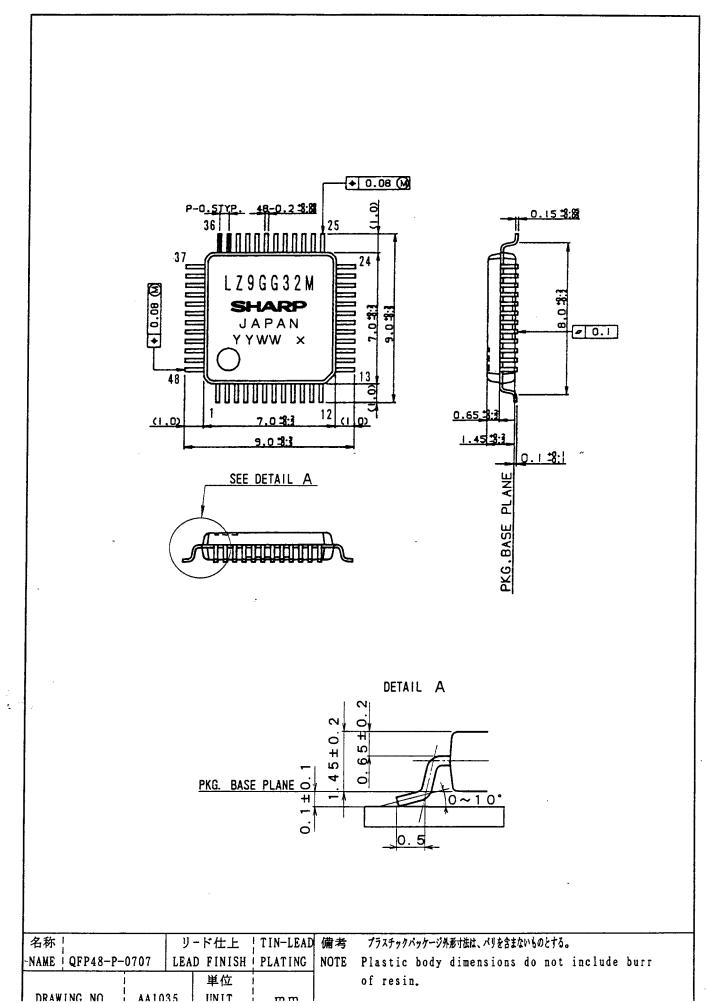
5-1. Soldering conditions (The following conditions are valid only for one time soldering.)

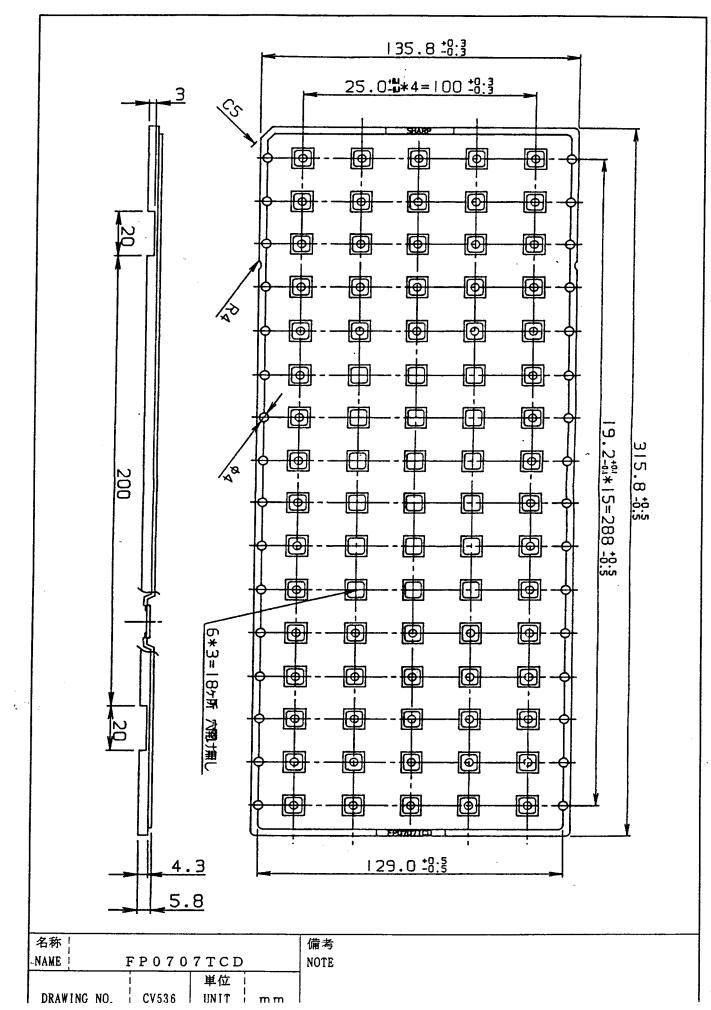
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering	Peak temperature of 240°C,	IC surface
(air)	duration less than 15 seconds	
	above 230℃, temperature	
	increase rate of $1 \sim 4^{\circ}$ C/second	
Vapor phase	215°C or less, duration less	Steam
solderring	than 40 seconds above $200^\circ\!\!\mathbb{C}$	
Manual soldering	260°C or less, duration less	IC outer lead surface
(soldering iron)	than 10 seconds	

5-2. Conditions for removal of residual flux

(1)	Ultrasonic washing power	: 25 Watts/liter or less
(2)	Washing time	: Total 1 minute maximum
(3)	Solvent temperature	: 15∼40°C







CCD, sensor, imaging, area sensor, pattern recognition, timing generator, vertical driver, white balance, LSI, LZ9GG32M