PC911

Ultra-high Speed Response and High CMR OPIC Photocoupler

❋ Lead forming type（I type ）and taping reel type （P type ）are also available. （**PC911I/PC911P** ）

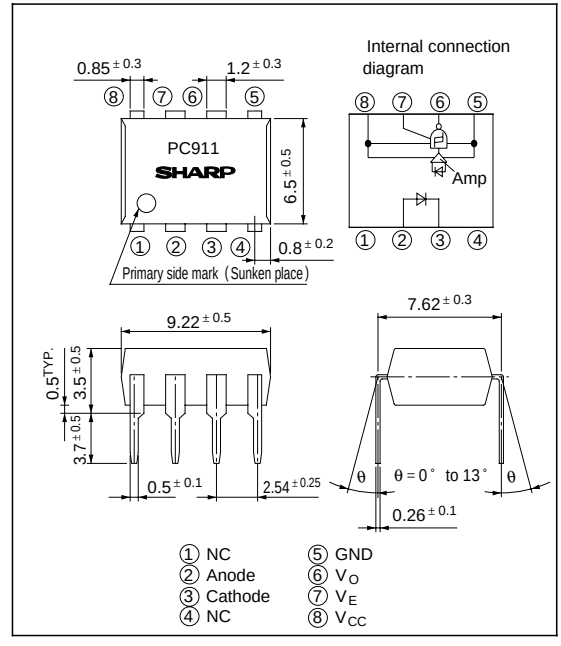
■ Features

1. Ultra-high speed response
（t_{PHL} , t_{PLH} : TYP. 50ns ）
2. High instantaneous common mode rejection voltage（CM_H : TYP. 10kV/μs）
3. High isolation voltage
（V_{iso} : 4 000V_{rms}）
4. Recognized by UL, file No. E64380

■ Applications

1. High speed interfaces for computer peripherals and microcomputer systems
2. High speed line receivers
3. Interfaces with various data transmission equipment

■ Outline Dimensions （Unit : mm）



* "OPIC"（Optical IC ）is a trademark of the SHARP Corporation.
An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Absolute Maximum Ratings （Ta= 25˚C）

Parameter		Symbol	Rating	Unit
Input	*1Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	*1Power dissipation	P	40	mW
Output	Supply voltage	V_{CC}	7	V
	*2Enable voltage	V_E	7	V
	High level output current	V_{OH}	- 8	mA
	Low level output current	I_{OL}	25	mA
	*1 *3Power dissipation	P	40	mW
*4Isolation voltage		V_{iso}	4 000	V_{rms}
Operating temperature		T_{opr}	0 to + 70	˚C
Storage temperature		T_{stg}	- 55 to + 125	˚C
*5Soldering temperature		T_{sol}	260	˚C

*1 Ta= 0 to 70˚C
*2 Shall not exceed 500mV from supply voltage(Vcc).
*3 Applicable to output terminal(V_o)
*4 AC for 1 minute, 40 to 60% RH
*5 For 10 seconds at the position of 2mm or more from root of lead pins.

■ Electro-optical Characteristics

(Ta= 0 to 70˚C unless specified)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	Ta= 25˚C, I_F = 10mA	-	1.6	1.9	V
	Reverse current		I_R	Ta= 25˚C, V_R = 5V	-	-	10	μA
	Terminal capacitance		C_t	Ta= 25˚C, V= 0, f= 1MHz	-	60	120	pF
Output	High level output voltage		V_{OH}	V_{CC} = 4.5V, I_{OH} = - 2mA, I_F = 0.25mA, V_E = 0.2V	2.4	-	-	V
	Low level output voltage		V_{OL}	V_{CC} = 4.5V, V_E = 2.0V, I_F = 5mA, I_{OL} = 13mA	-	0.3	0.6	V
	High level enable voltage		V_{EH}	V_{CC} = 5.5V	2.0	-	-	V
	Low level enable voltage		V_{EL}	V_{CC} = 5.5V	-	-	0.8	V
	High level enable current		I_{EH}	V_{CC} = 5.5V, V_E = 5.5V	-	-	100	μA
	Low level enable current		I_{EL}	V_{CC} = 5.5V, V_E = 0.5V	-	- 0.2	- 0.4	mA
	High level supply current		I_{CCH}	V_{CC} = 5.5V, I_F = 0, V_E = 2.0V	-	13	23	mA
	Low level supply current		I_{CCL}	V_{CC} = 5.5V, I_F = 10mA, V_E = 2.0V	-	15	25	mA
	High impedance supply current		I_{CCZ}	V_{CC} = 5.5V, V_E = 0	-	16	26	mA
	Output leak current		I_{OH}	V_{CC} = 5.5V, V_E = 2.0V, V_O = 5.5V, I_F = 0.25mA	-	-	100	μA
	High impedance output current		I_{OZH}	V_{CC} = 5.5V, V_E = 0.4V	-	-	100	μA
	Output short-circuit current		I_{OS}	V_{CC} = 5.5V, V_O = 0, I_F = 0, within 10ms.	- 10	-	- 50	mA
Transfer charac-teristics	"High→Low" threshold input current		I_{FHL}	V_{CC} = 5V, V_E = 2.0V	-	2.5	5	mA
	"Low→High" threshold input current		I_{FLH}	V_{CC} = 5V, V_E = 2.0V	0.5	1.9	-	mA
	Hysteresis		I_{FLH} /I_{FHL}	V_{CC} = 5V, V_E = 2.0V	0.55	-	0.95	-
	Isolation resistance		R_{ISO}	Ta= 25˚C, DC500V, 40 to 60% RH	5 x 10^{10}	10^{11}	-	Ω
	Floating capacitance		C_f	Ta= 25˚C, V= 0, f= 1MHz	-	0.6	5	pF
	Rsponse characteristics	"High→Low" propagation delay time	t_{PHL}	Ta= 25˚C, V_{CC}= 5V, C_L= 15pF, I_F = 7.5mA, Fig. 1	-	50	75	ns
		"Low→High" propagation delay time	t_{PLH}		-	50	75	ns
		*6 Pulse width distortion	ΔT_W		-	-	35	ns
		Rise time, Fall time	t_r , t_f		-	15	30	ns
		"High→Low" enable propagation delay time	t_{EHL}	Ta= 25˚C, V_{CC}= 5V, R_L = 350Ω, C_L = 15pF, I_F = 7.5mA, V_{EH} = 3V, V_{EL} = 0, Fig. 2	-	40	70	ns
		"Low→High" enable propagation delay time	t_{ELH}		-	40	70	ns
	CMR	Instantaneous common mode rejection voltage "output : High level"	CM_H	Ta= 25˚C, V_{CC}= 5V, V_{CM}= 50V, I_F = 0mA, $V_{O(MIN.)}$= 2V, Fig. 3	3 000	10 000	-	V/μs
		Instantaneous common mode rejection voltage "output : Low level"	CM_L	Ta= 25˚C, V_{CC}= 5V, V_{CM}= 50V, I_F = 5mA, $V_{O(MAX.)}$= 0.8V, Fig. 3	- 3 000	- 10 000	-	V/μs

*6 $\Delta T_W = t_{PHL} - t_{PLH}$

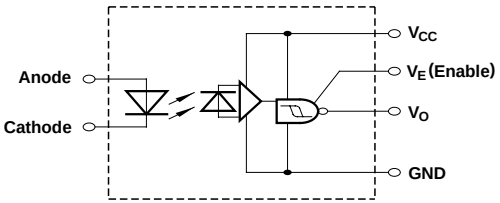
All typical values : at Ta= 25˚C, V_{cc}= 5V

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	MAX.	Unit
Low level input current	I_{FL}	0	250	μA
High level input current	I_{FH}	7	15	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage	V_{EL}	0	0.8	V
Supply voltage	V_{CC}	4.5	5.5	V
Fanout (TTL load)	N	-	8	-
Operating temperature	T_{opr}	0	70	˚C

1. When the enable input is not used, please connect to V_{CC}.
2. In order to stabilize power supply line, connect a by-pass ceramic capacitor (0.01 to 0.1μF) between V_{CC} and GND at the position within 1cm from pin.

Block Diagram

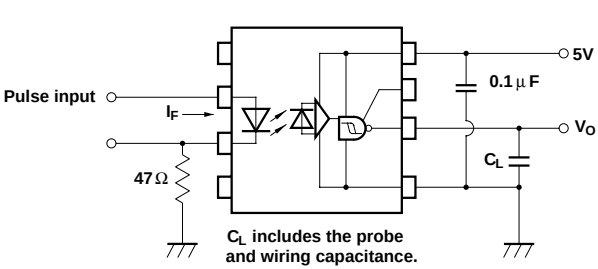


Truth table

Input	Enable	Output
H	H	L
L	H	H
H	L	Z
L	L	Z

L : Logic (0)
H : Logic (1)
Z : High impedance

Fig. 1 Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f



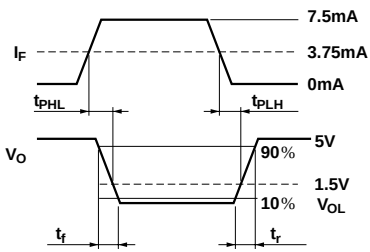
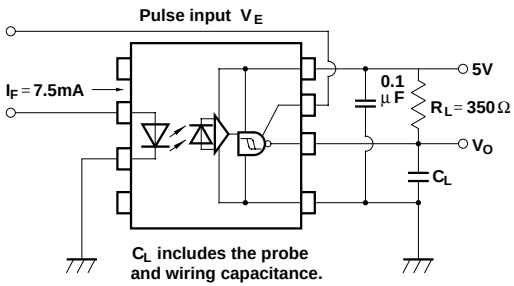


Fig. 2 Test Circuit for t_{EHL} and t_{ELH}



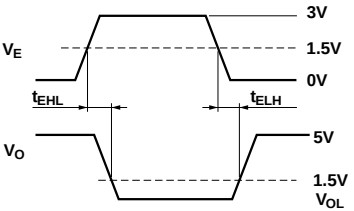


Fig. 3 Test Circuit for CM_H and CM_L

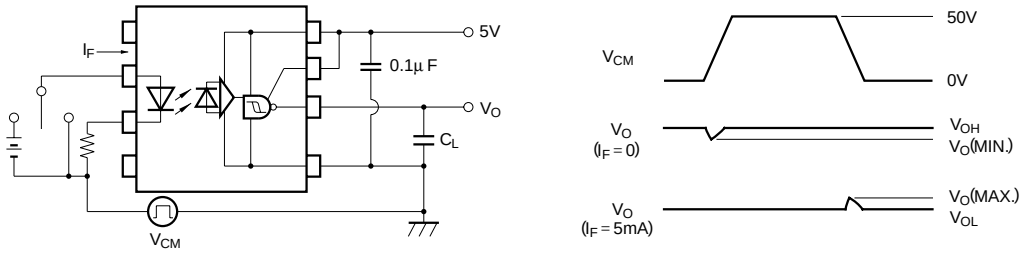


Fig. 4 Forward Current vs. Forward Voltage

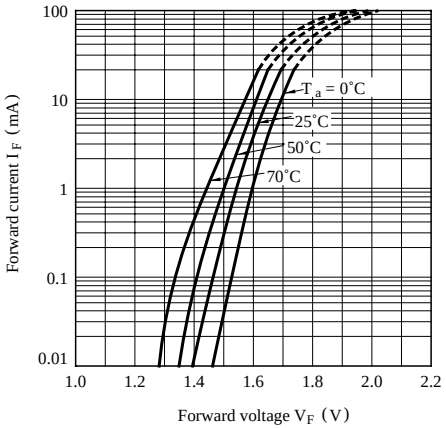


Fig. 5 Low Level Output Voltage vs. Low Level Output Current

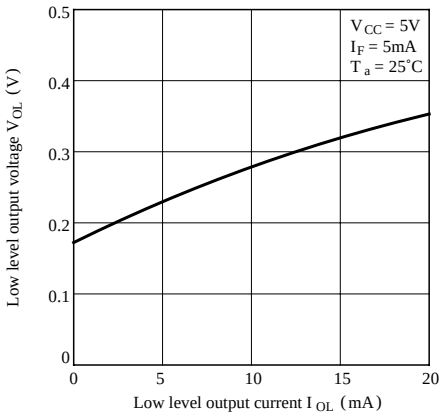


Fig. 6 High Level Output Voltage vs. High Level Output Current

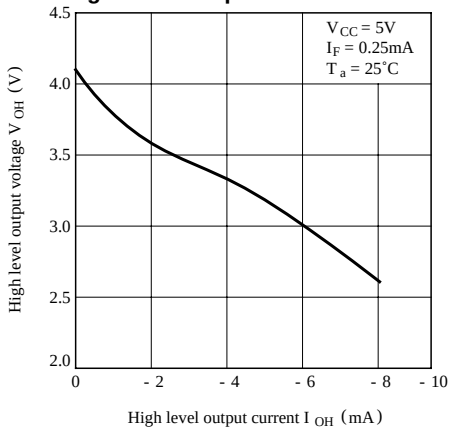


Fig. 7 Propagation Delay Time vs. Ambient Temperature

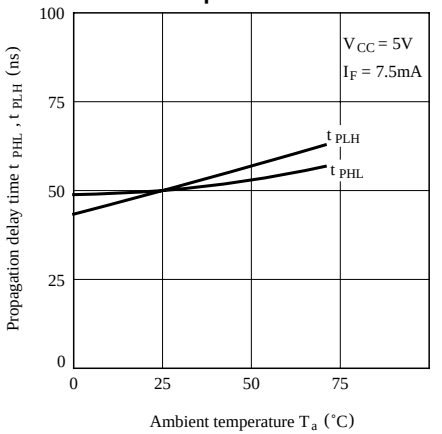
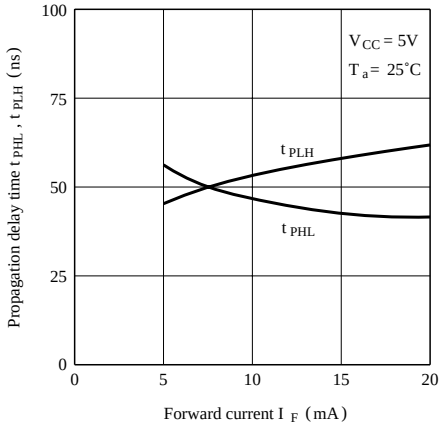


Fig. 8 Propagation Delay Time vs. Forward Current



● Please refer to the chapter "Precautions for Use"