PC912X

Ultra-high Speed Response OPIC Photocoupler

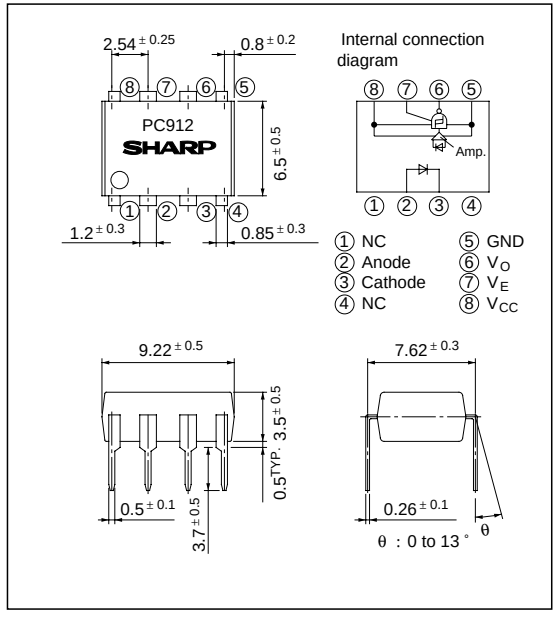
■ Features

1. Ultra-high speed response
   (t_{PHL}, t_{PLH} : TYP. 40ns)
2. High instantaneous common mode rejection voltage (CM$_H$: MIN. 3kV/ μs)
3. Capable of high speed digital transmission
   (Transmission speed : MAX. 20Mb/s)
   (NRZ signal)

■ Applications

1. Personal computers
2. Electrical music instruments

■ Outline Dimensions (Unit : mm)



* "OPIC" (Optical IC) is a trademark of the SHARP Corporation.
An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Absolute Maximum Ratings (Ta= 25°C)

Parameter		Symbol	Rating	Unit
Input	*1 Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	*1 Power dissipation	P	40	mW
Output	Supply voltage	V_{CC}	7	V
	*2 Enable voltage	V_E	7	V
	High level output current	I_{OH}	- 8	mA
	Low level output current	I_{OL}	25	mA
	*1, 3 Collector power dissipation	P_O	40	mW
*4 Isolation voltage		V_{iso}	2.5	kV rms
Operating temperature		T_{opr}	0 to + 70	°C
Storage temperature		T_{stg}	- 55 to + 125	°C
*5 Soldering temperature		T_{sol}	260	°C

*1 Ta= 0 to 70°C
*2 It shall not exceed 500mV or more over supply voltage (V_{CC}).
*3 Applied to output terminal (V_O)
*4 AC for 1 minute, 40 to 60% RH
*5 For 10 seconds

■ Electro-optical Characteristics

(Unless specified : Ta= 0 to 70˚C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	Ta= 25˚C, I_F = 10mA	-	1.6	1.9	V
	Reverse current		I_R	Ta= 25˚C, V_R = 5V	-	-	10	μA
	Terminal capacitance		C_t	Ta= 25˚C, V_F = 0V f= 1MHz	-	60	120	pF
Output	High level output voltage		V_{OH}	V_{CC}= 4.5V, I_{OH} = - 2mA I_F = 0.25mA, V_E = 2.0V	2.4	-	-	V
	Low level output voltage		V_{OL}	V_{CC}= 4.5V, V_E = 2.0V I_F = 5mA, I_{OL}= 13mA	-	0.3	0.6	V
	High level enable voltage		V_{EH}	V_{CC}= 5.5V	2.0	-	-	V
	Low level enable voltage		V_{EL}	V_{CC}= 5.5V	-	-	0.8	V
	High level enable current		I_{EH}	V_{CC}= 5.5V, V_E= 5.5V	-	-	100	μA
	Low level enable current		I_{EL}	V_{CC}= 5.5V, V_E= 0.5V	-	- 0.2	- 0.4	mA
	High level supply current		I_{CCH}	V_{CC}= 5.5V, I_F = 0mA V_E = 2.0V	-	13	23	mA
	Low level supply current		I_{CCL}	V_{CC}= 5.5V, I_F = 10mA V_E = 2.0V	-	15	25	mA
	High impedance supply current		I_{CCZ}	V_{CC}= 5.5V, V_E= 0V	-	16	26	mA
	Output leak current		I_{OH}	V_{CC}= 5.5V, V_E= 2.0V V_O= 5.5V, I_F = 0.25mA	-	-	100	μA
	High impedance output current		I_{OZH}	V_{CC}= 5.5V, V_E= 0.4V	-	-	100	μA
	Output short-circuit current		I_{OS}	V_{CC}= 5.5V, V_O= 0V I_F = 0mA 10ms or less	- 10	-	- 50	mA
Transfer characteristics	"High→Low" threshold input current		I_{FHL}	V_{CC}= 5V V_E = 2.0V	-	2.5	5	mA
	"Low→High" threshold input current		I_{FLH}		0.5	1.9	-	mA
	Hysteresis		I_{FLH}/I_{FHL}		0.55	-	0.95	-
	Isolation resistance		R_{ISO}	Ta= 25˚C, DC= 500V 40 to 60% RH	5×10^{10}	10^{11}	-	Ω
	Floating capacitance		C_f	Ta= 25˚C, V= 0V f=1MHz	-	0.6	5	pF
	Response time	"High→Low" propagation delay time	t_{PHL}	Ta= 25˚C V_{CC}= 5V C_L = 15pF I_F = 7.5mA *6	-	40	55	ns
		"Low→High" propagation delay time	t_{PLH}		-	40	55	ns
		Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ΔT_w		-	-	15	ns
		Rise/fall time	t_r, t_f		-	15	30	ns
		"High→Low" enable propagation delay time	t_{EHL}	Ta= 25˚C, V_{CC}= 5V R_L = 350Ω, C_L = 15pF I_F = 7.5mA, V_{EH} = 3V V_{EL} = 0V, *7	-	40	70	ns
		"Low→High" enable propagation delay time	t_{ELH}		-	40	70	ns
	CMR	Instantaneous common mode rejection voltage (High level output)	CM_H	Ta= 25˚C, V_{CC}= 5V V_{CM} = 50V, I_F = 0mA V_O(Min) = 2V, *8	3 000	10 000	-	V/μs
		Instantaneous common mode rejection voltage (Low level output)	CM_L	Ta= 25˚C, V_{CC}= 5V V_{CM} = 50V, I_F = 5mA V_O(Max) = 0.8V, *8	- 3 000	10 000	-	V/μs

*6 Refer to Fig. 1 *7 Refer to Fig. 2 *8 Refer to Fig. 3

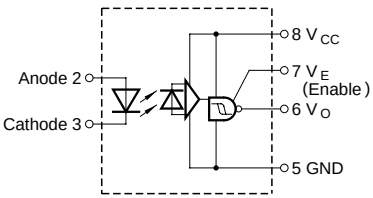
All typical values are at Ta= 25˚C, V_{CC}= 5V.

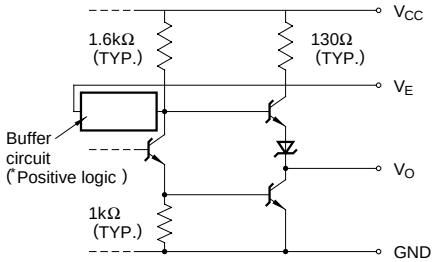
■ Recommended Operating Conditions

Parameter	Symbol	MIN.	MAX.	Unit
Low level input current	I_{FL}	0	250	μA
High level input current	I_{FH}	7	15	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage	V_{EL}	0	0.8	V
Supply voltage	V_{CC}	4.5	5.5	V
Fan out （TTL load ）	N	-	8	-
Operating temperature	Topr	0	70	˚C

1. When the enable input is not used, please connect to Vcc.
2. It is necessary to connect a by-pass ceramic capacitor （0.01 to 0.1μF） between Vcc and GND at the position within 1cm from pin.

■ Block Diagram





* Positive logic:

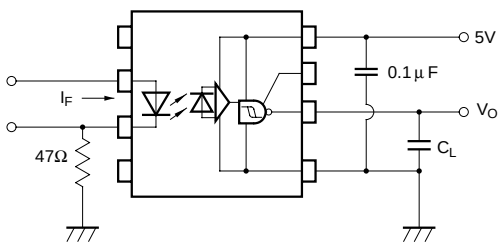
V_E	Buffer output
L	L
H	H

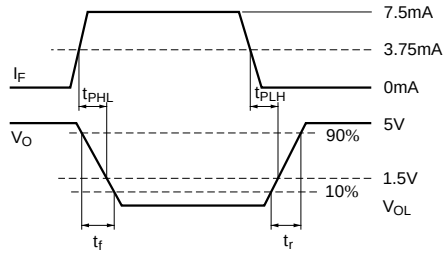
■ Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	Z
L	L	Z

L : Logic （0）
H : Logic （1）
Z : High impedance

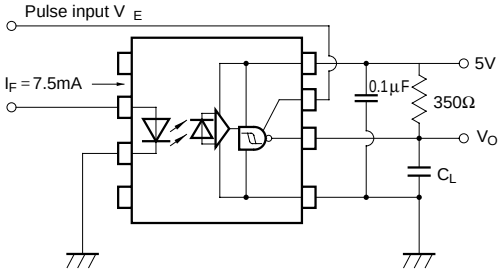
Fig. 1 Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f





* C_L includes the probe and wiring capacitance.

Fig. 2 Test Circuit for t_{EHL} and t_{ELH}



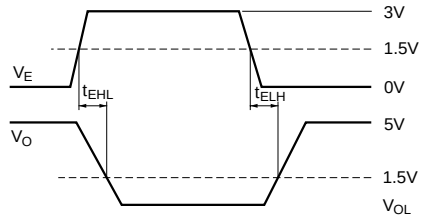
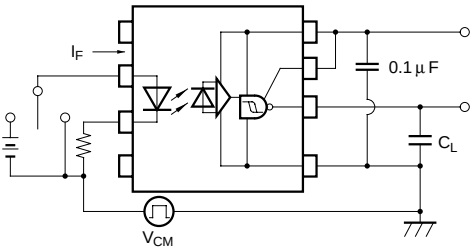


Fig. 3 Test Circuit for CM_H and CM_L



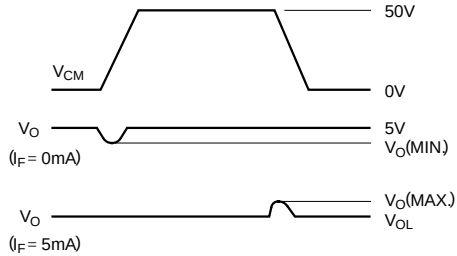


Fig. 4 Forward Current vs. Forward Voltage

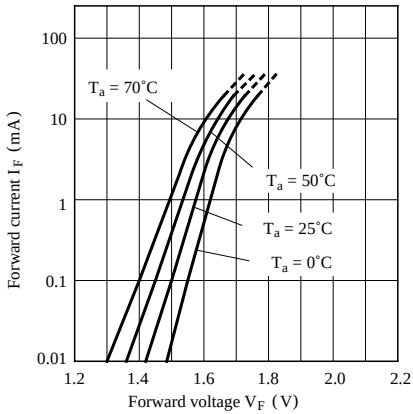


Fig. 5 Low Level Output Voltage vs. Low Level Output Current

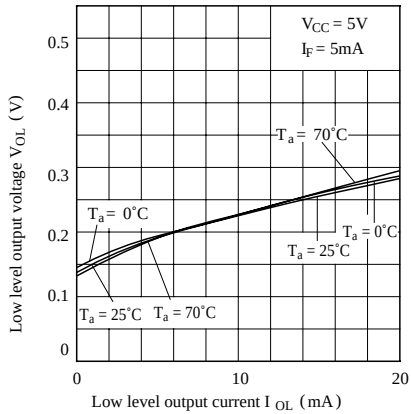


Fig. 6 High Level Output Voltage vs. High Level Output Current

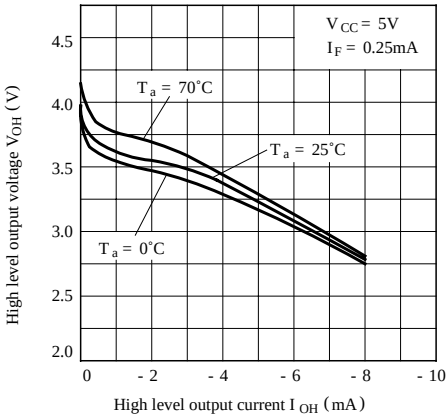


Fig. 7 Propagation Delay Time vs. Ambient Temperature

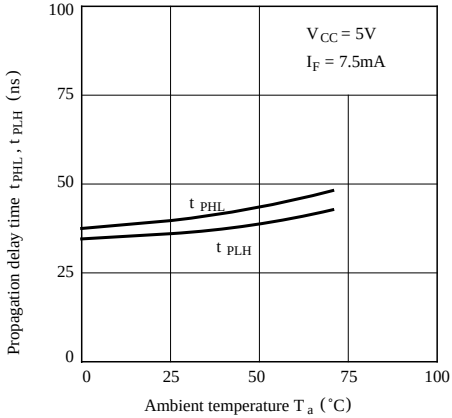
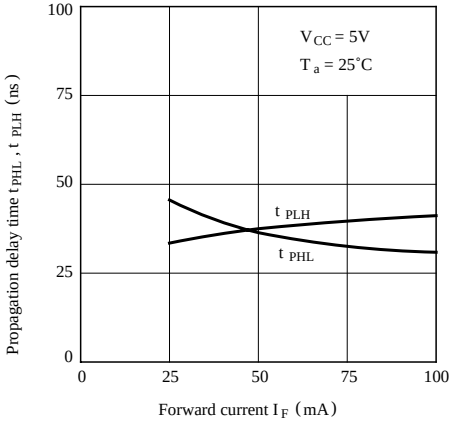


Fig. 8 Propagation Delay Time vs. Forward Current



● Please refer to the chapter "Precautions for Use"