LH532000B-1

CMOS 2M (256K × 8/128K × 16) MROM

FEATURES

- 262,144 words × 8 bit organization
  (Byte mode)
  131,072 words × 16 bit organization
  (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 μW (MAX.)
- Mask-programmable control pin
  (for 40-pin DIP/40-pin SOP):
  Pin 1 = $OE_1/\overline{OE_1}/DC$
  Pin 12 = $OE/\overline{OE}$
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH532000B-1 is a CMOS 2M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

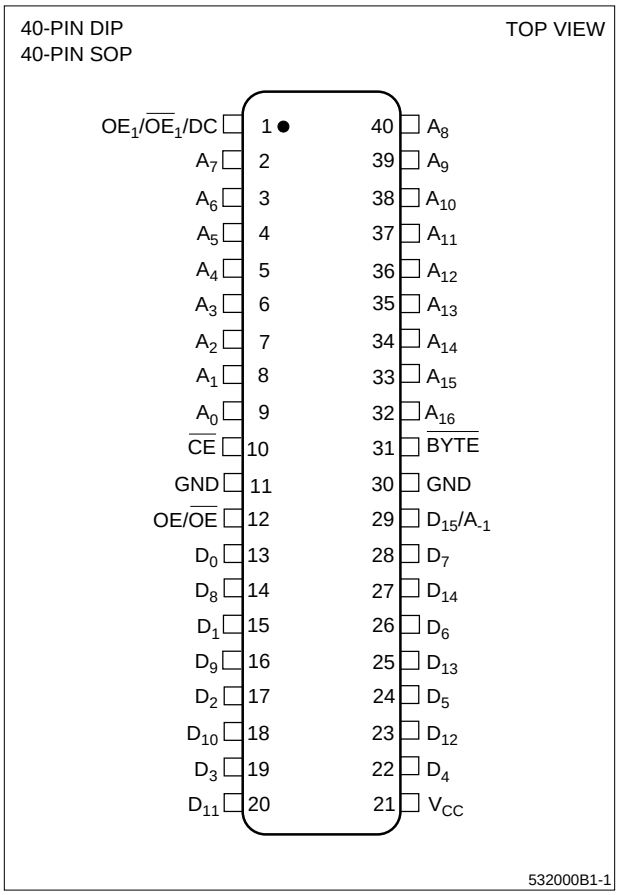


Figure 1. Pin Connections for DIP and SOP Packages

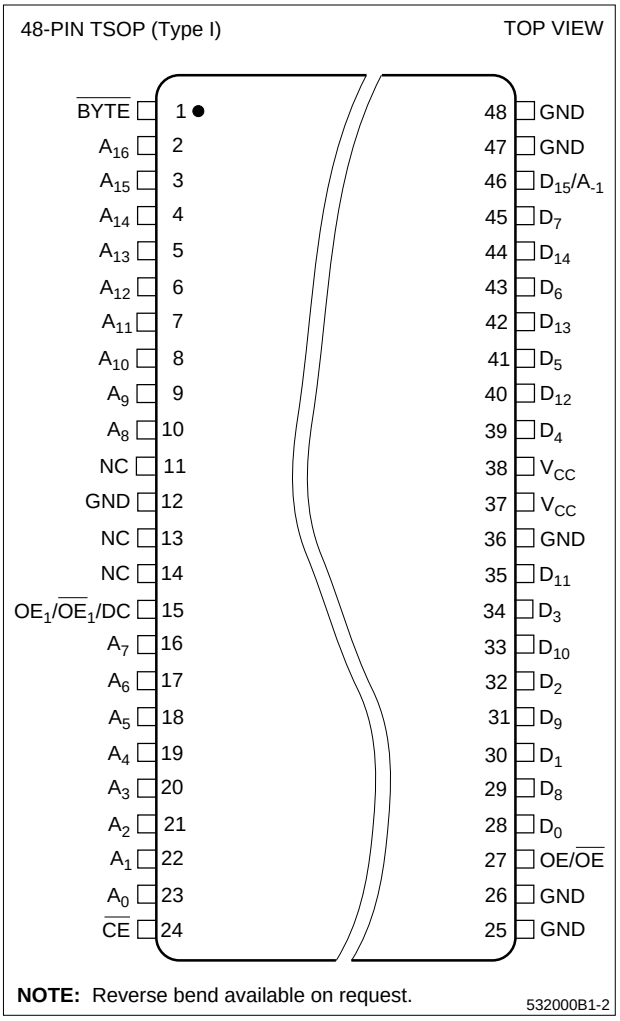


Figure 2. Pin Connections for TSOP Package

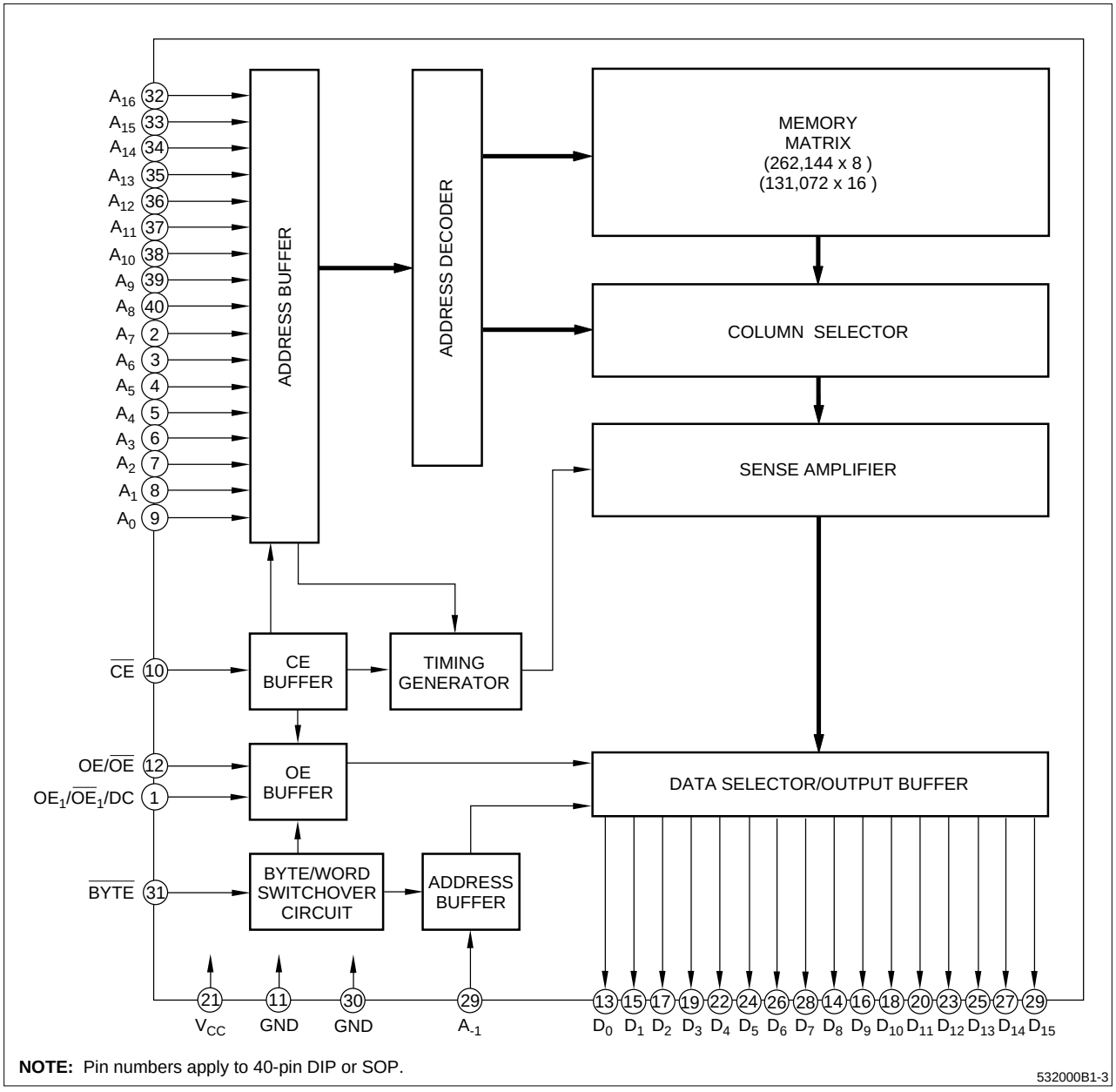


Figure 3. LH532000B-1 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
$A_{-1} - A_{16}$	Address input	1
$D_0 - D_{15}$	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	2
$OE_1/\overline{OE_1}$/DC	Output enable input	2
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be LOW in byte mode, and data output (D_{15}) when set to be HIGH in word mode.
2. The active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC are mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	L/H	X	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	H/L	H/L	H	–	$D_0 - D_7$	$D_8 - D_{15}$	A_0	A_{16}	Operating (I_{CC})
L	H/L	H/L	L	L	$D_0 - D_7$	High-Z	A_{-1}	A_{16}	Operating (I_{CC})
L	H/L	H/L	L	H	$D_8 - D_{15}$	High-Z	A_{-1}	A_{16}	Operating (I_{CC})

NOTE:
1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		–0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45	mA	2
	I_{CC3}	t_{RC} = 120 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40	mA	3
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz			10	pF	
Output capacitance	C_{OUT}	T_A = 25°C			10	pF	

NOTES:
1. $\overline{CE}$/OE/$\overline{OE_1}$ = V_{IH}, OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable access time	t_{ACE}		120	ns	
Output enable delay time	t_{OE}		55	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		55	ns	1
OE to output in High-Z	t_{OHZ}		55	ns	

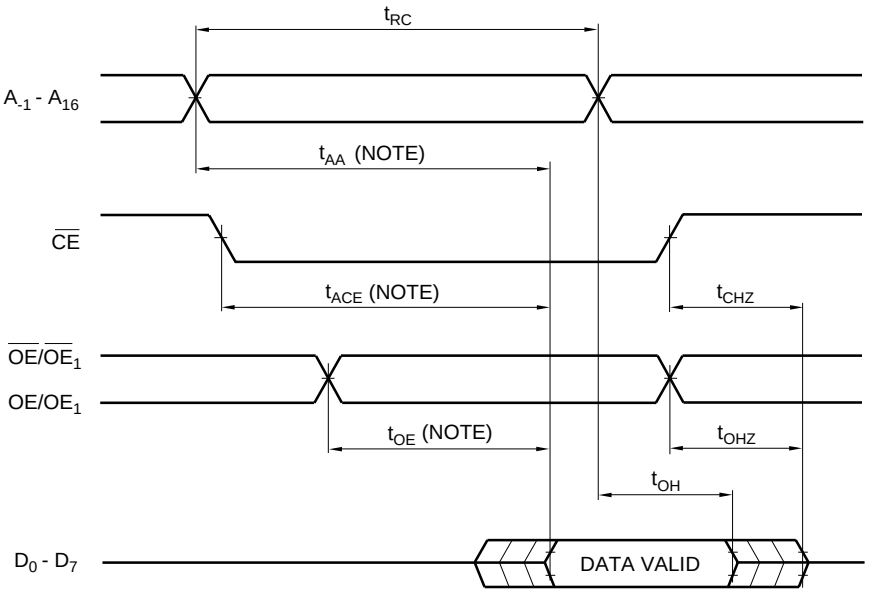
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1 TTL + 100 pF

CAUTION

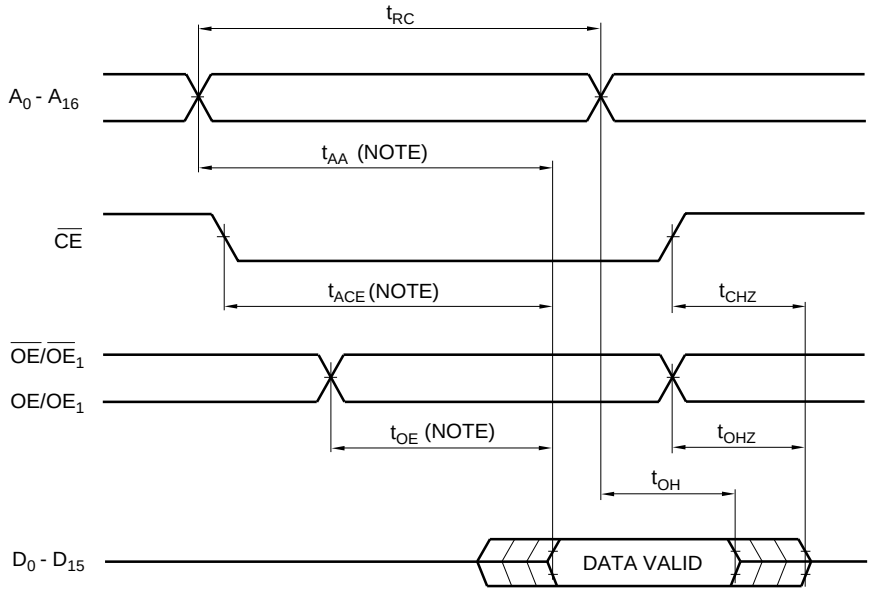
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE} have concluded.

532000B1-4

Figure 4. Byte Mode ($\overline{BYTE}$ = V_{IL})



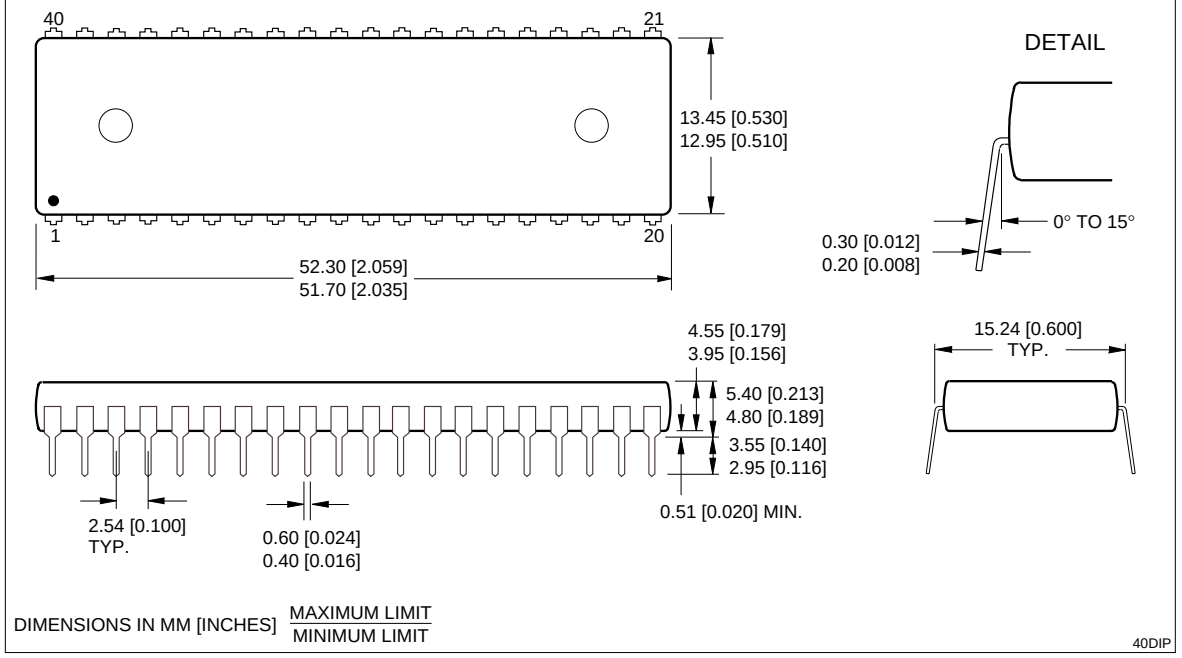
NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE} have concluded.

532000B1-5

Figure 5. Word Mode ($\overline{BYTE}$ = V_{IH})

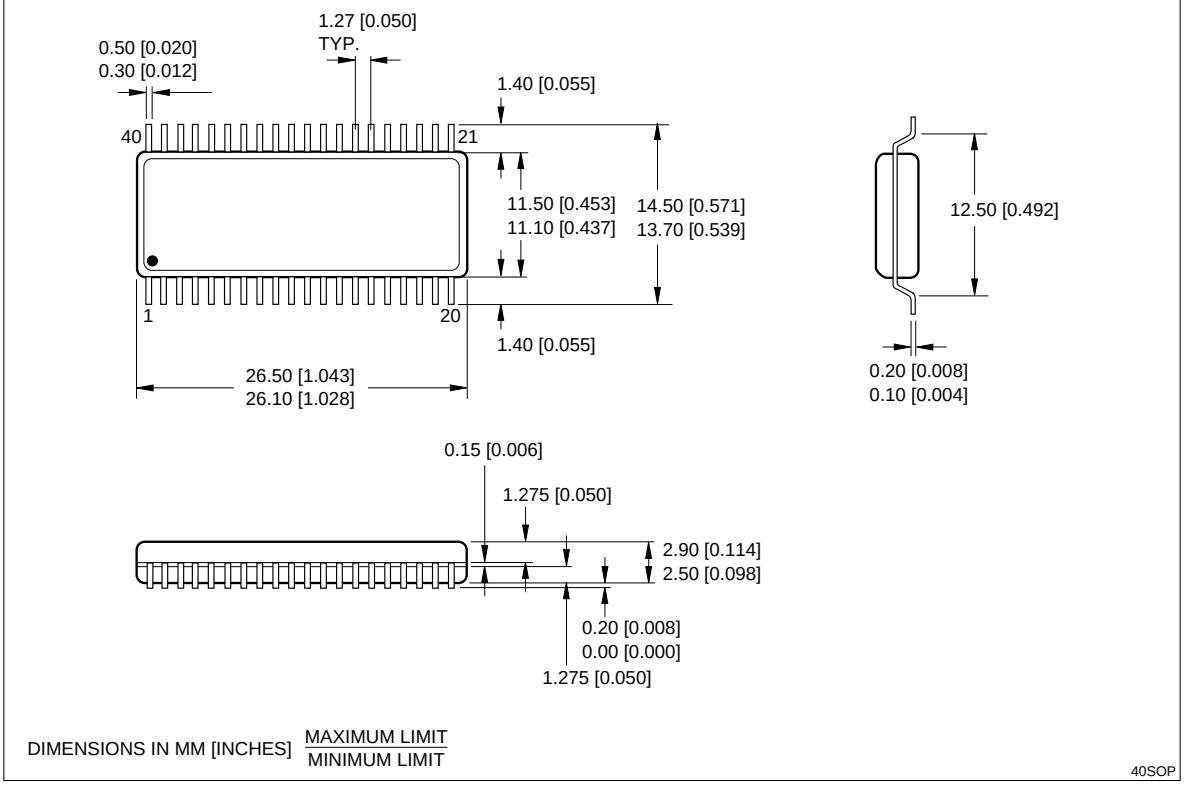
PACKAGE DIAGRAMS

40DIP (DIP040-P-0600)



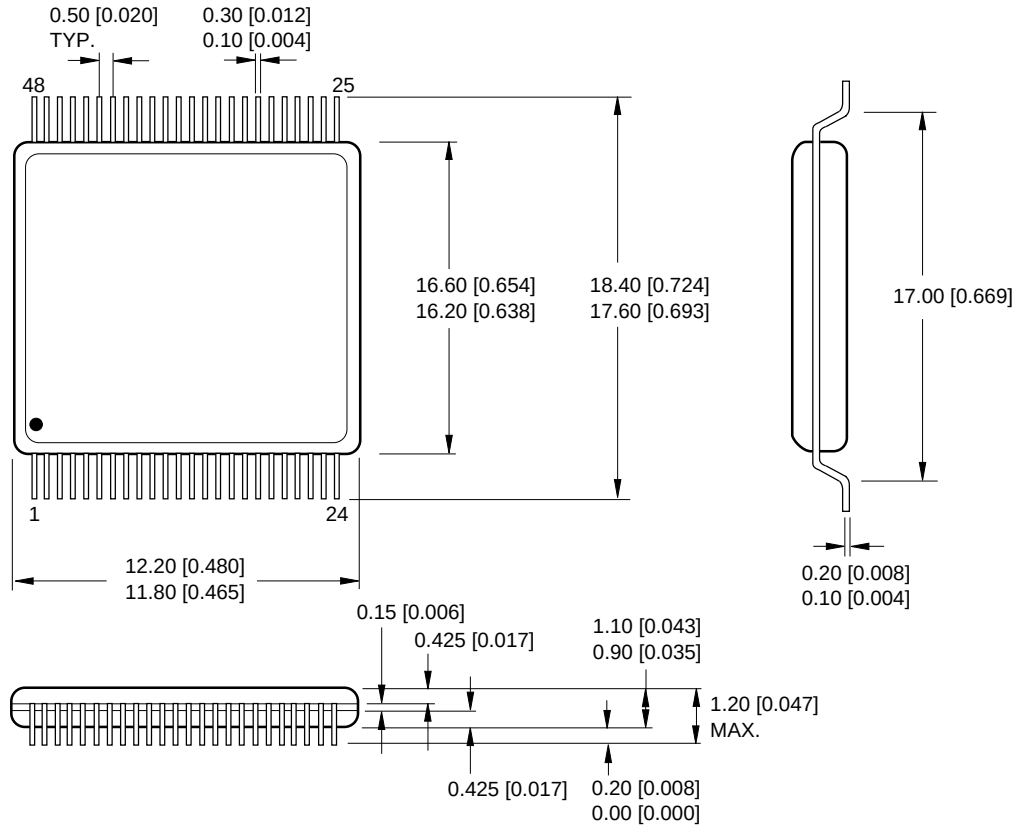
40-pin, 600-mil DIP

40SOP (SOP040-P-0525)



40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH532000B	X	-1
Device Type	Package	120 ns Version

- D 40-pin, 600-mil DIP (DIP040-P-0600)
- N 40-pin, 525-mil SOP (SOP040-P-0525)
- T 48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM

Example: LH532000BD-1 (CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM, 40-pin, 600-mil DIP)

532000B1-6