

LH5164AZ8

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access time:
200 ns ($V_{CC} = 3.0\text{ V MAX.}$)
- Power consumption:
Operating:
60 mW (MAX.) @ 3 V
Standby (to 60°C):
3 μW (MAX.) @ 3 V
Data hold
0.6 μA ($V_{CC} = 3\text{ V}$, $T_A = 60^\circ\text{C}$)
- Operating voltage range:
3.0 V to 3.6 V
- Wide operating temperature range:
-30 to 60°C
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Package: 28-pin, 450-mil SOP

DESCRIPTION

The LH5164AZ8 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

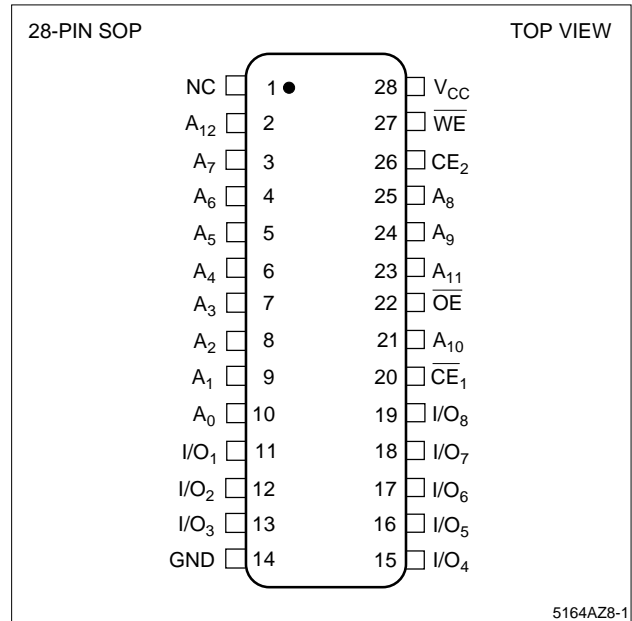


Figure 1. Pin Connections for SOP Package

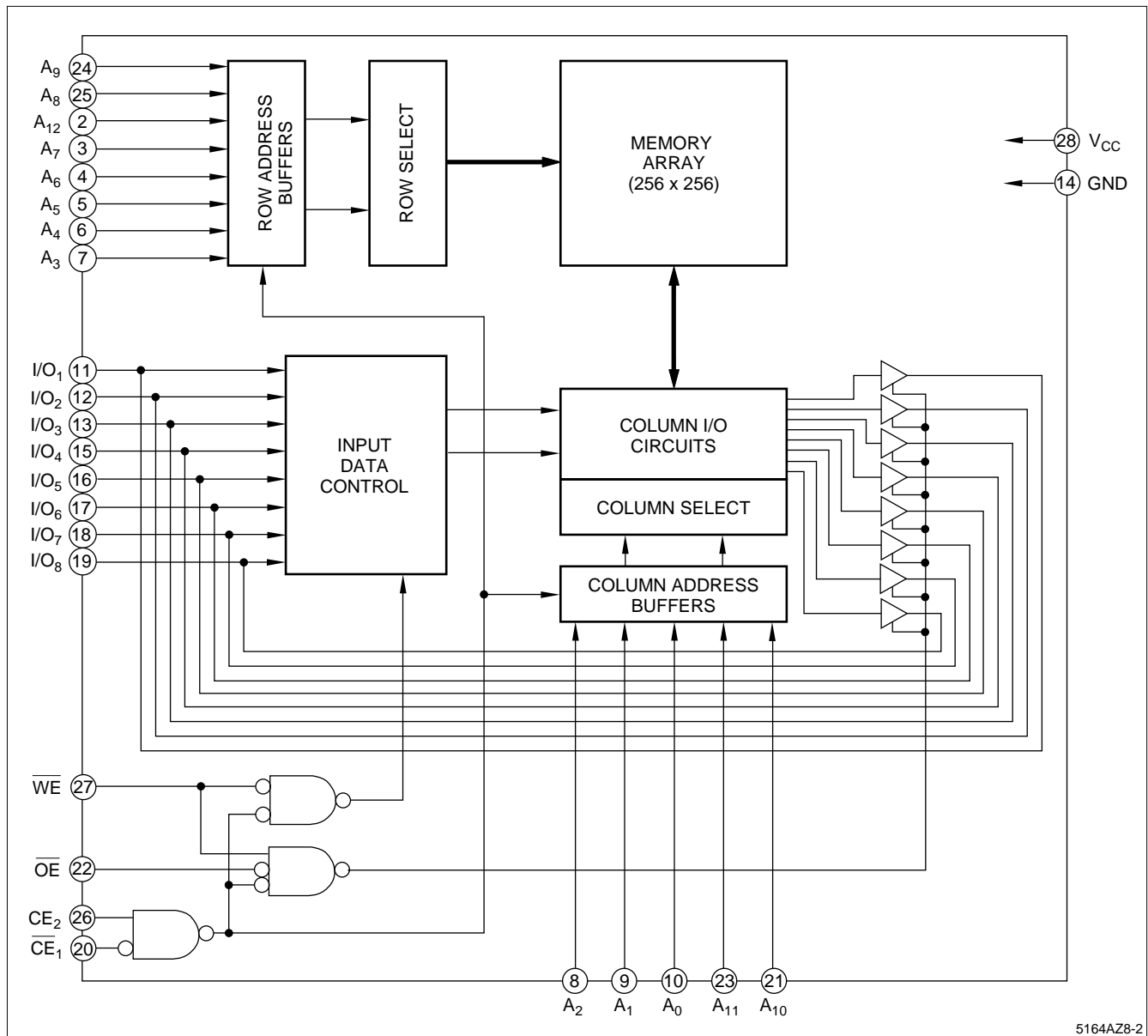


Figure 2. LH5164AZ8 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₂	Address inputs
CE ₁ - CE ₂	Chip Enable input
WE	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data inputs and outputs
V _{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I _{SB})	1
X	L	X	X	Standby	High-Z	Standby (I _{SB})	1
L	H	L	X	Write	D _{IN}	Operating (I _{CC})	1
L	H	H	L	Read	D _{OUT}	Operating (I _{CC})	
L	H	H	H	Output deselect	High-Z	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V	1
Operating temperature	T _{opr}	-30 to +60	°C	
Storage temperature	T _{stg}	-65 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -30 to +60°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	3.0		3.6	V
Input voltage (V _{CC} = 3.0 to 3.6 V)	V _{IH}	V _{CC} - 0.5		V _{CC} + 0.3	V
	V _{IL}	-0.3		0.2	V

DC CHARACTERISTICS (T_A = -30 to +60°C, V_{CC} = 3.0 to 3.6 V)

ADD TABLE

NOTE:

1. CE₂ should be $\geq V_{CC} - 0.2$ V or ≤ 0.2 V.

AC CHARACTERISTICS

(1) READ CYCLE ($T_A = -30$ to $+60^\circ\text{C}$, $V_{CC} = 3.0$ to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	
Read cycle	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable access time	(CE_1)	t_{ACE1}		200	ns
	(CE_2)	t_{ACE2}		200	ns
Output enable access time	t_{OE}		150	ns	
Output hold time	t_{OH}	10		ns	
Chip enable to output in Low-Z	(\overline{CE}_1)	t_{LZ1}	20		ns
	(CE_2)	t_{LZ2}	20		ns
Output enable to output in Low-Z	t_{OLZ}	10		ns	
Chip enable to output in High-Z	(CE_1)	t_{HZ1}	0	60	ns
	(CE_2)	t_{HZ2}	0	60	ns
Output disable to output in High-Z	t_{OHZ}	0	40	ns	

(2) WRITE CYCLE ($T_A = -30$ to $+60^\circ\text{C}$, $V_{CC} = 3.0$ to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	200		ns
Chip enable to end of write	t_{CW}	180		ns
Address valid to end of write	t_{AW}	180		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	0		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Output active from end of write	t_{OW}	20		ns
WE to output in High-Z	t_{WZ}	0	60	ns
OE to output in High-Z	t_{OHZ}	0	40	ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1$ MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0$ V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{IO} = 0$ V			10	pF

NOTE:

This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -30 to +60°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V _{CCDR}	CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CCDR} - 0.2 V	2.0	5.5	V	1
Data retention supply current	I _{CCDR}	V _{CCDR} = 3.0 V, CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CCDR} - 0.2 V		0.2 0.6	μA	1
Chip disable to data retention	t _{CDR}		0		ns	
Recovery time	t _R		t _{RC}		ns	2

NOTES:

1. CE₂ should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V.
2. t_{RC} = Read cycle time

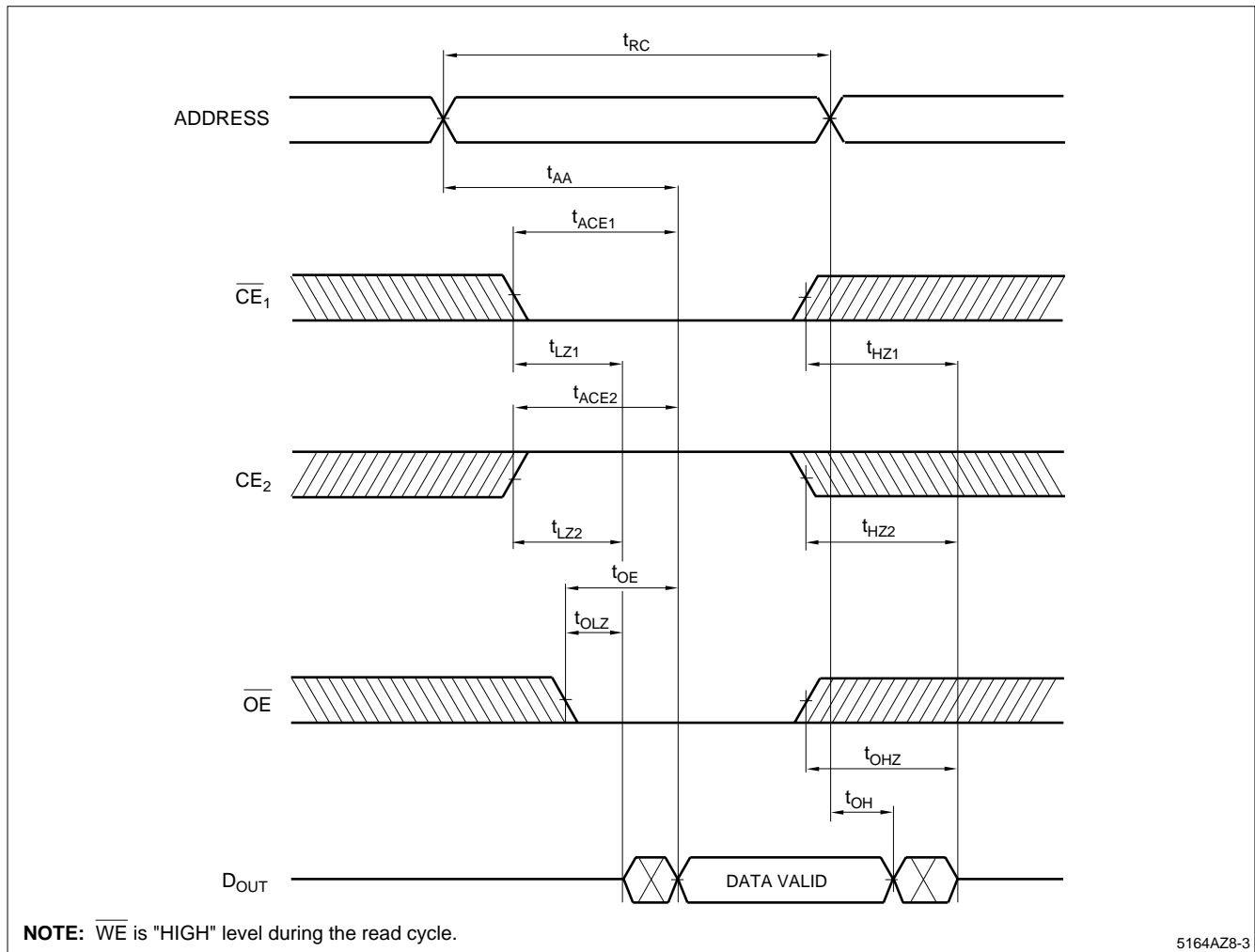
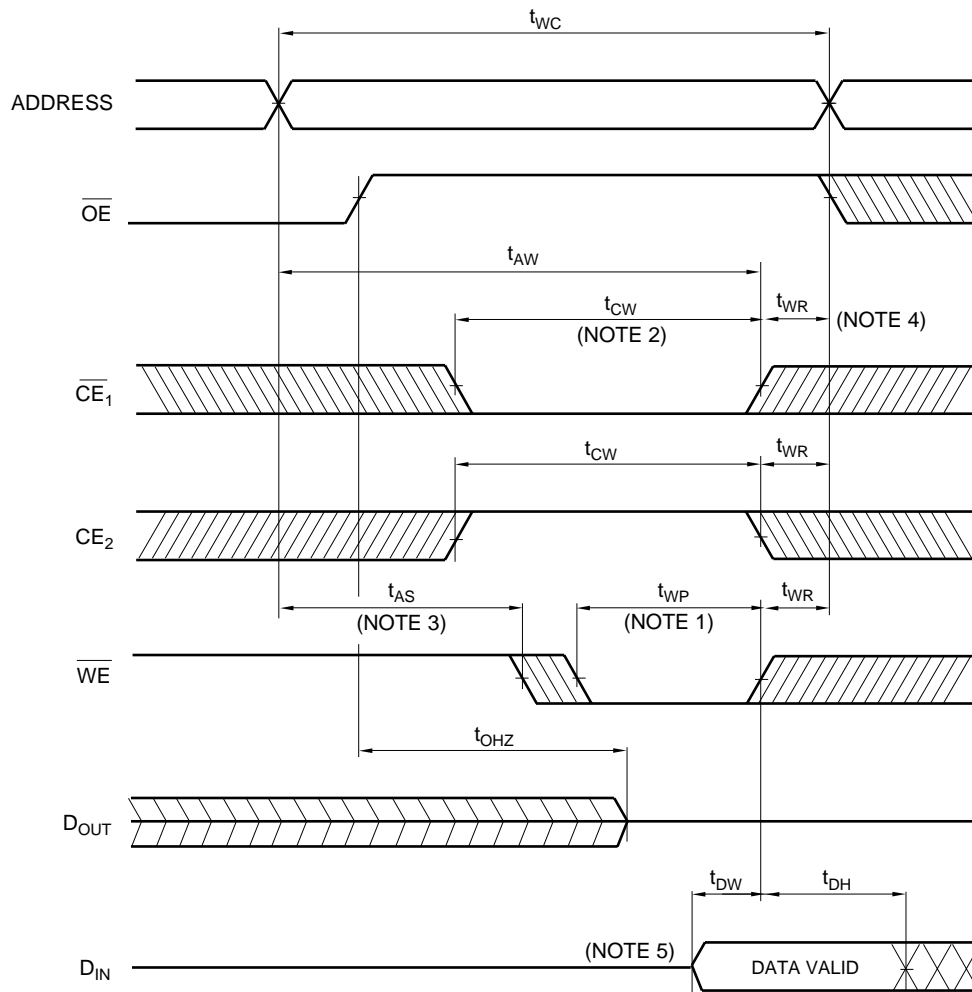


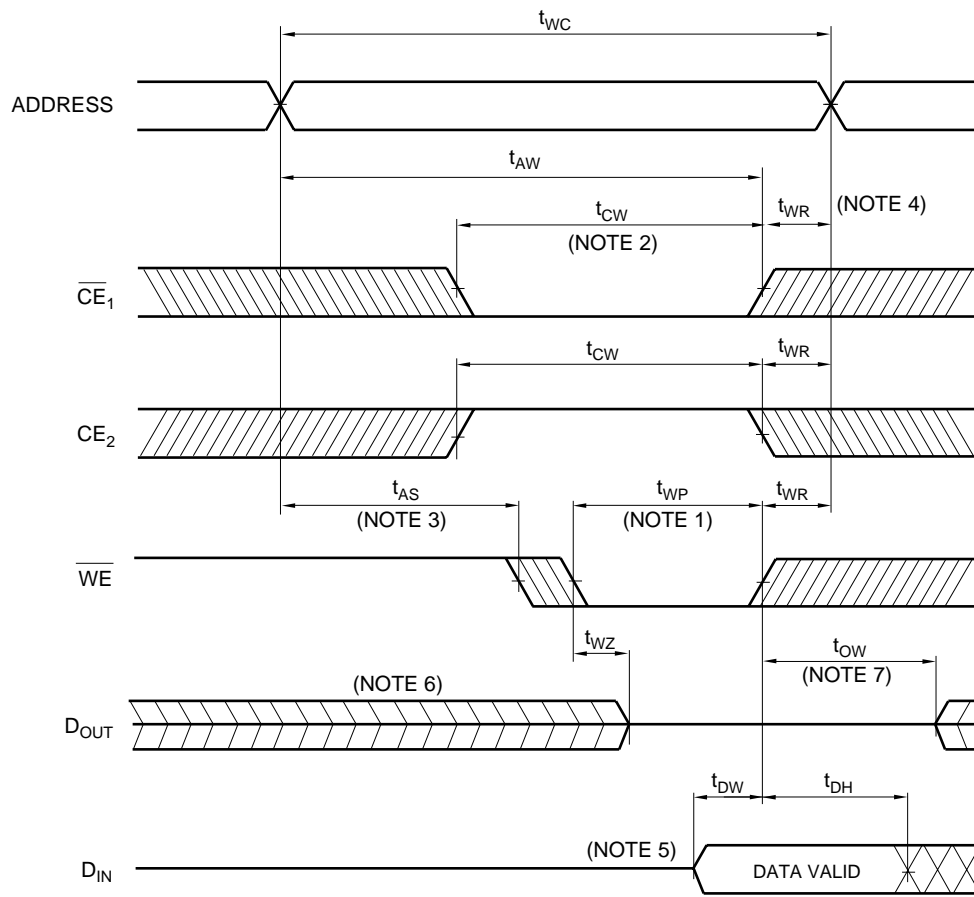
Figure 3. Read Cycle

**NOTES:**

1. The writing occurs during an overlapping period of $\overline{CE}_1 = \text{"LOW"}$, $CE_2 = \text{"HIGH"}$, and $\overline{WE} = \text{"LOW"}$ (t_{WP}).
2. t_{CW} is defined as the time from the last occurring transit, either \overline{CE}_1 LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.

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Figure 4. Write Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}_1 = \text{"LOW,"}$ $CE_2 = \text{"HIGH,"}$ and $\overline{WE} = \text{"LOW"}$ (t_{WP}).
2. t_{CW} is defined as the time from the last occurring transit, either \overline{CE}_1 LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.
6. If \overline{CE}_1 LOW transit or CE_2 HIGH transit occurs at the same time or after \overline{WE} LOW transit, the output will remain high-impedance.
7. If \overline{CE}_1 HIGH transit or CE_2 LOW transit occurs at the same time or before \overline{WE} HIGH transit, the output will remain high-impedance.

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Figure 5. OE Low Fixed

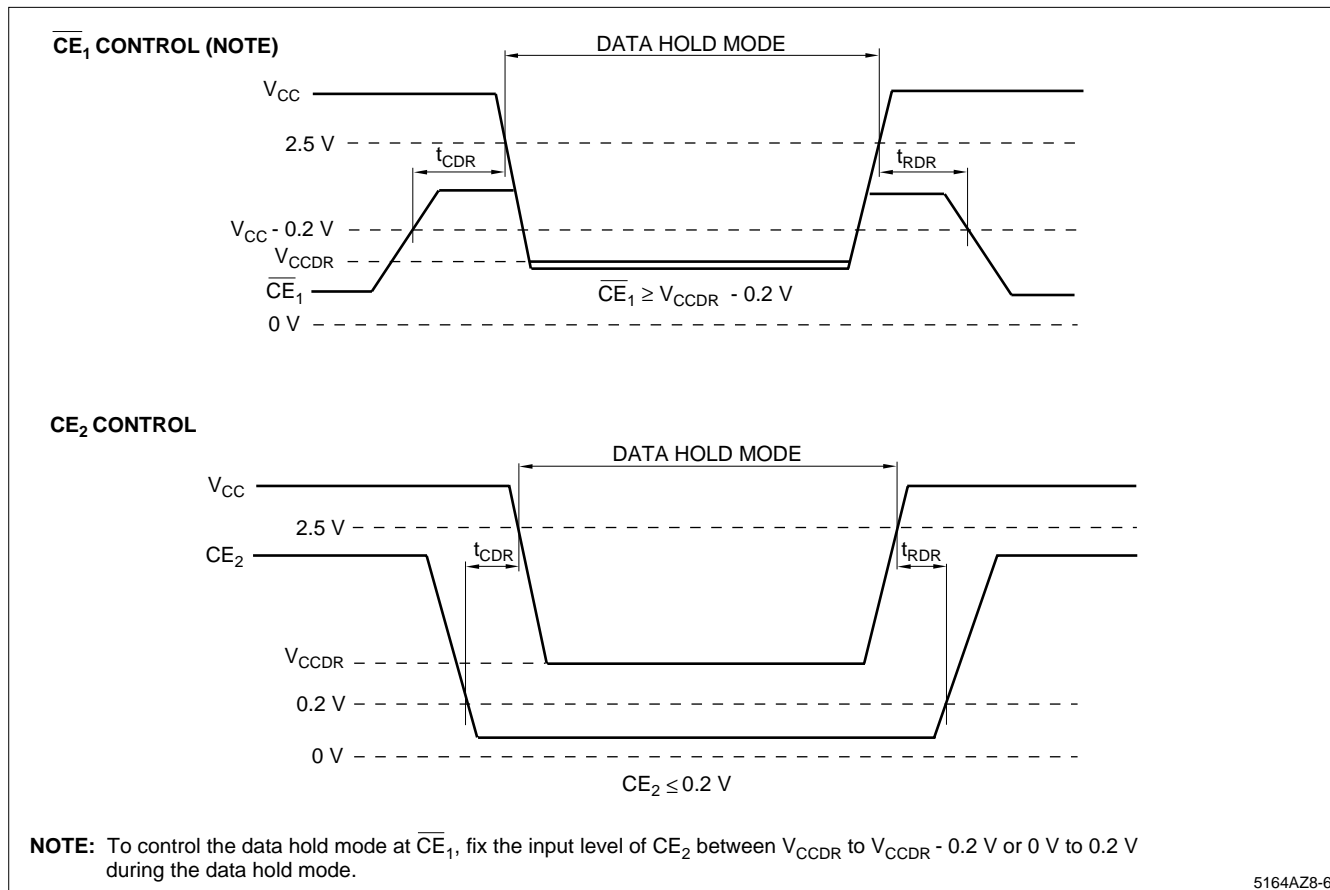
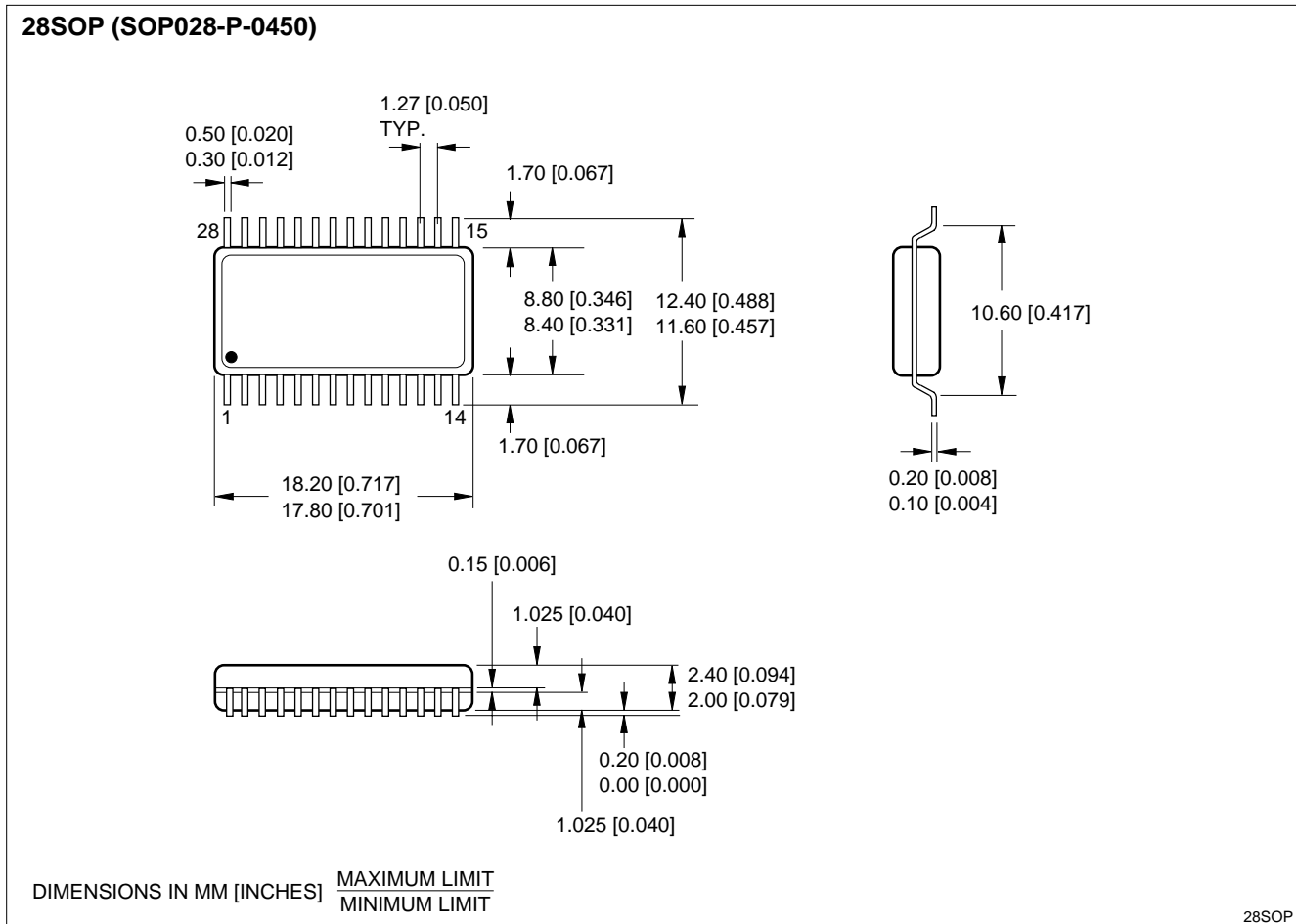


Figure 6. Low Voltage Data Retention

PACKAGE DIAGRAM



28-pin, 450-mil SOP

ORDERING INFORMATION

