

LH530800A

CMOS 1M (128K × 8) MROM

FEATURES

- 131,072 words × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
 - Operating: 192.5 mW (MAX.)
 - Standby: 550 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
 - 32-pin, 600-mil DIP
 - 32-pin, 525-mil SOP
 - 32-pin, 450-mil QFJ (PLCC)
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH530800A is a mask-programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

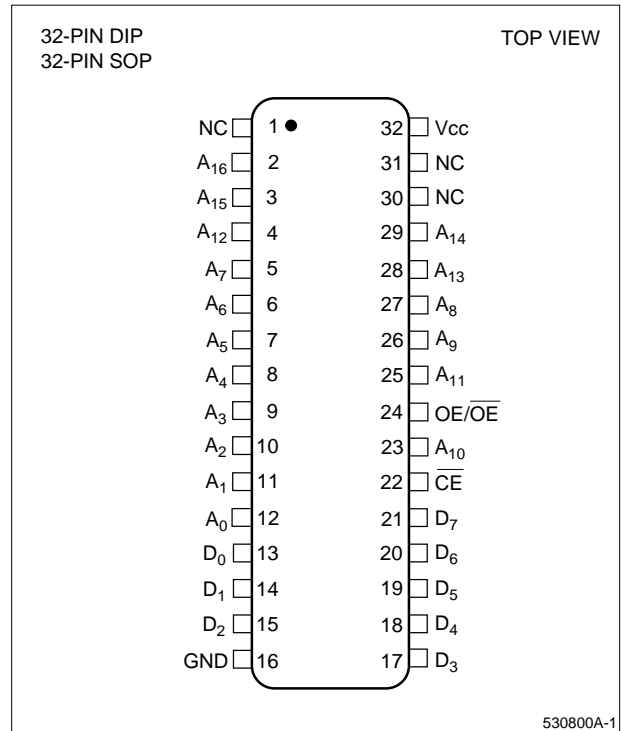


Figure 1. Pin Connections for DIP and SOP Packages

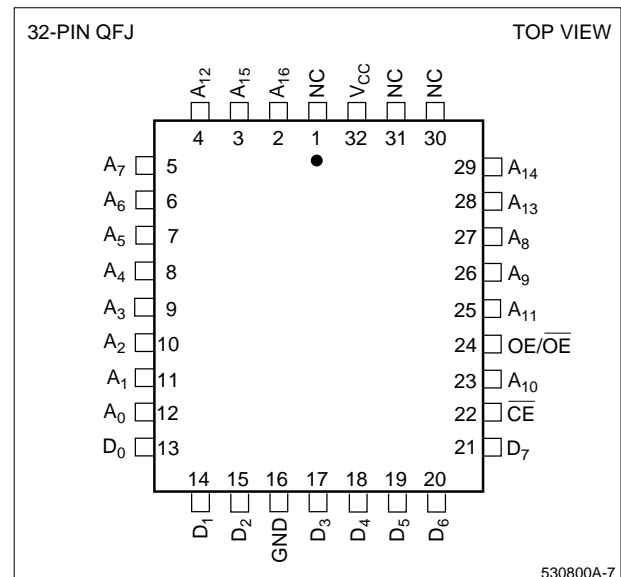


Figure 2. Pin Connections for QFJ (PLCC) Package

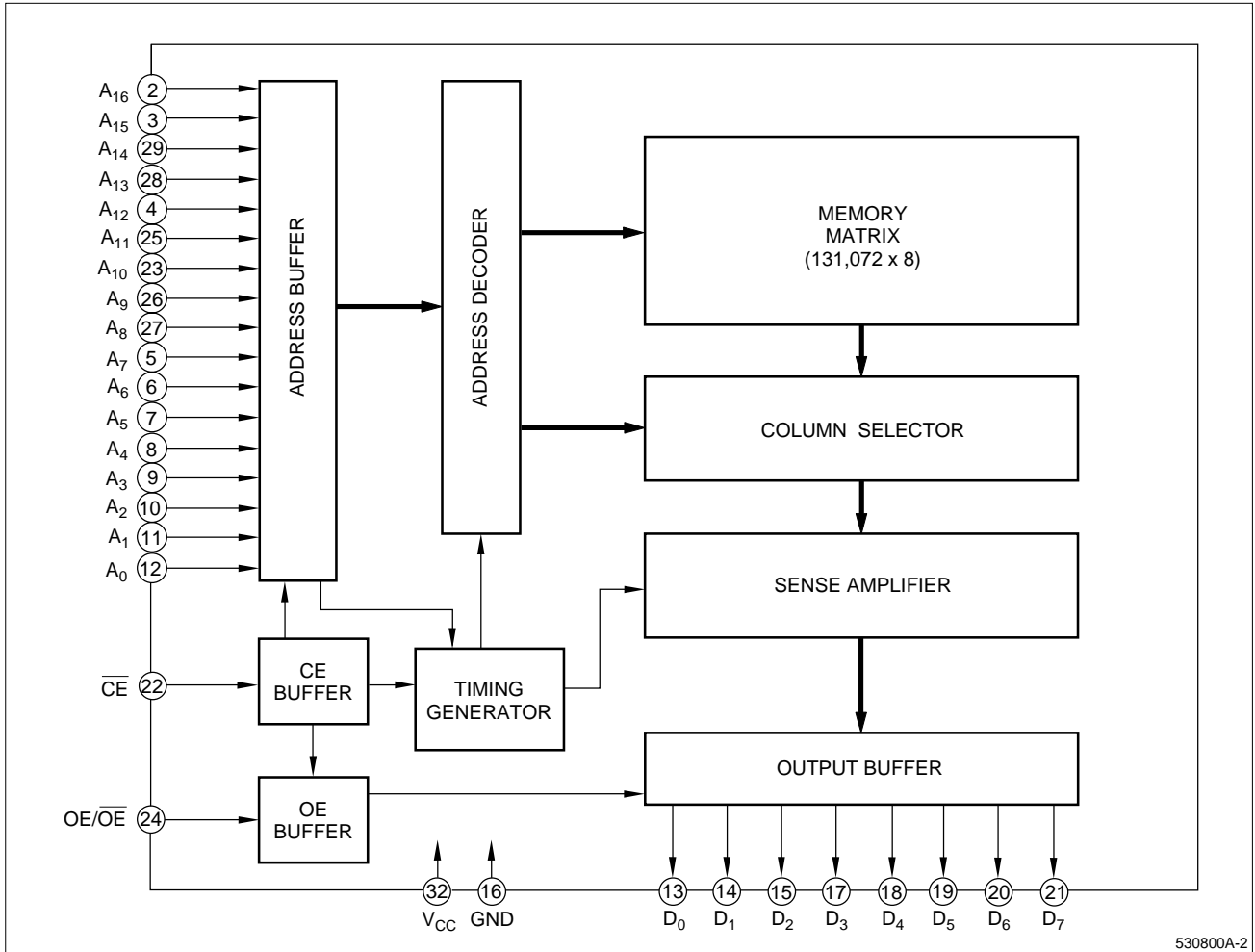


Figure 3. LH530800A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₀ - A ₁₆	Address input	
D ₀ - D ₇	Data Output	
CE	Chip enable input	1
OE/OE	Output enable input	1

SIGNAL	PIN NAME	NOTE
V _{CC}	Power supply (+5 V)	
GND	Ground	
NC	No connection	

NOTE:

1. Active level of OE/OE is mask-programmable.

TRUTH TABLE

CE	OE/OE	MODE	D ₀ - D ₇	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I _{SB})	1
L	L/H	Non selected	High-Z	Operating (I _{CC})	
L	H/L	Selected	D _{OUT}	Operating (I _{CC})	

NOTE:

1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		$V_{CC} + 0.3$	V	
Output 'Low' voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$			0.4	V	
Output 'High' voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4			V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{CC}$			10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$			10	μA	1
Operating current	I_{CC1}	$t_{RC} = 150\text{ ns}$			35	mA	2
	I_{CC2}	$t_{RC} = 1\text{ }\mu\text{s}$			25		
	I_{CC3}	$t_{RC} = 150\text{ ns}$			30	mA	3
	I_{CC4}	$t_{RC} = 1\text{ }\mu\text{s}$			20		
Standby current	I_{SB1}	$CE = V_{IH}$			2	mA	
	I_{SB2}	$CE = V_{CC} - 0.2\text{ V}$			100		
Input capacitance	C_{IN}	$f = 1\text{ MHz}$			10	pF	
Output capacitance	C_{OUT}	$T_A = 25^\circ\text{C}$			10		

NOTES:

1. $CE/OE = V_{IH}$ or $OE = V_{IL}$
2. $V_{IN} = V_{IH}$ or V_{IL} , $CE = V_{IL}$, outputs open
3. $V_{IN} = (V_{CC} - 0.2\text{ V})$ or 0.2 V , $CE = 0.2\text{ V}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable time	t_{ACE}			150	ns	
Output enable time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:

1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

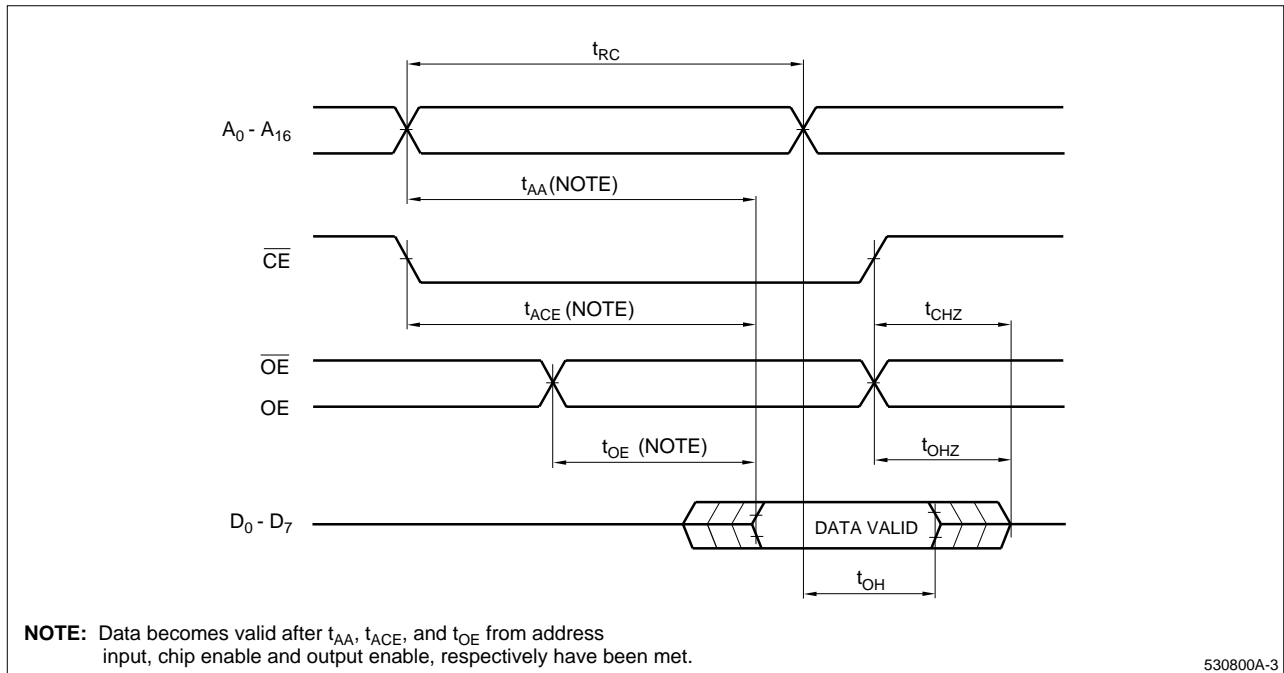
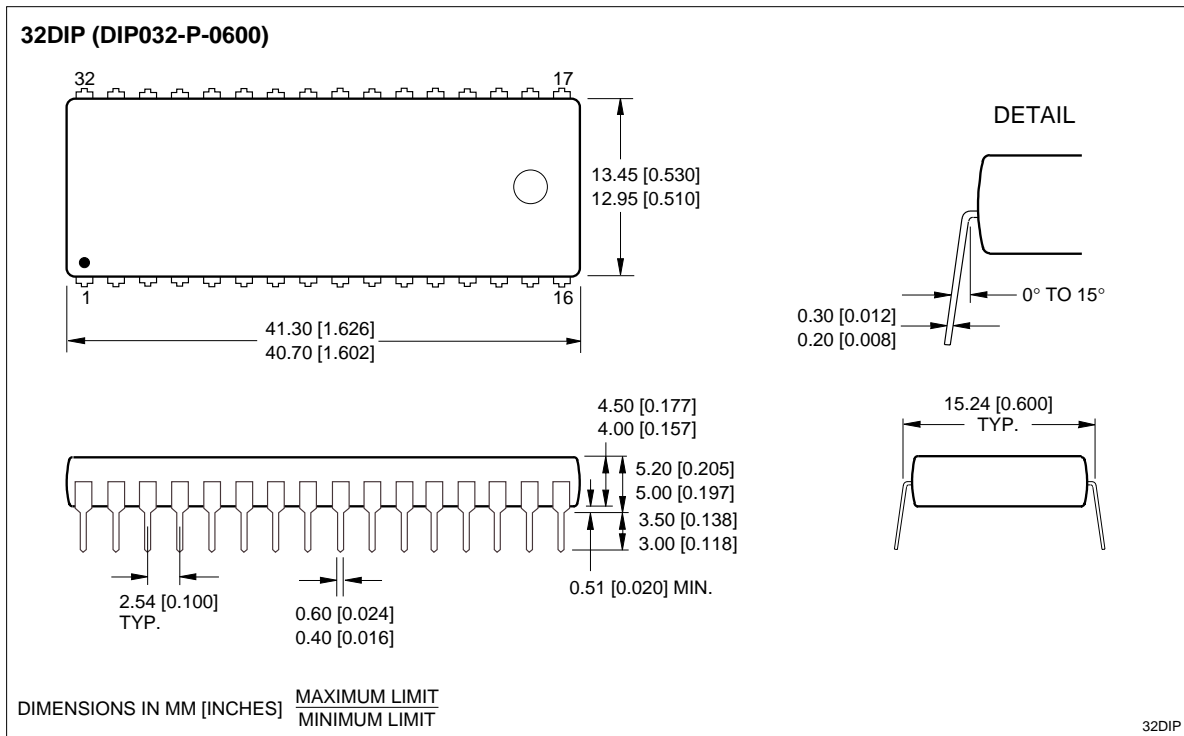
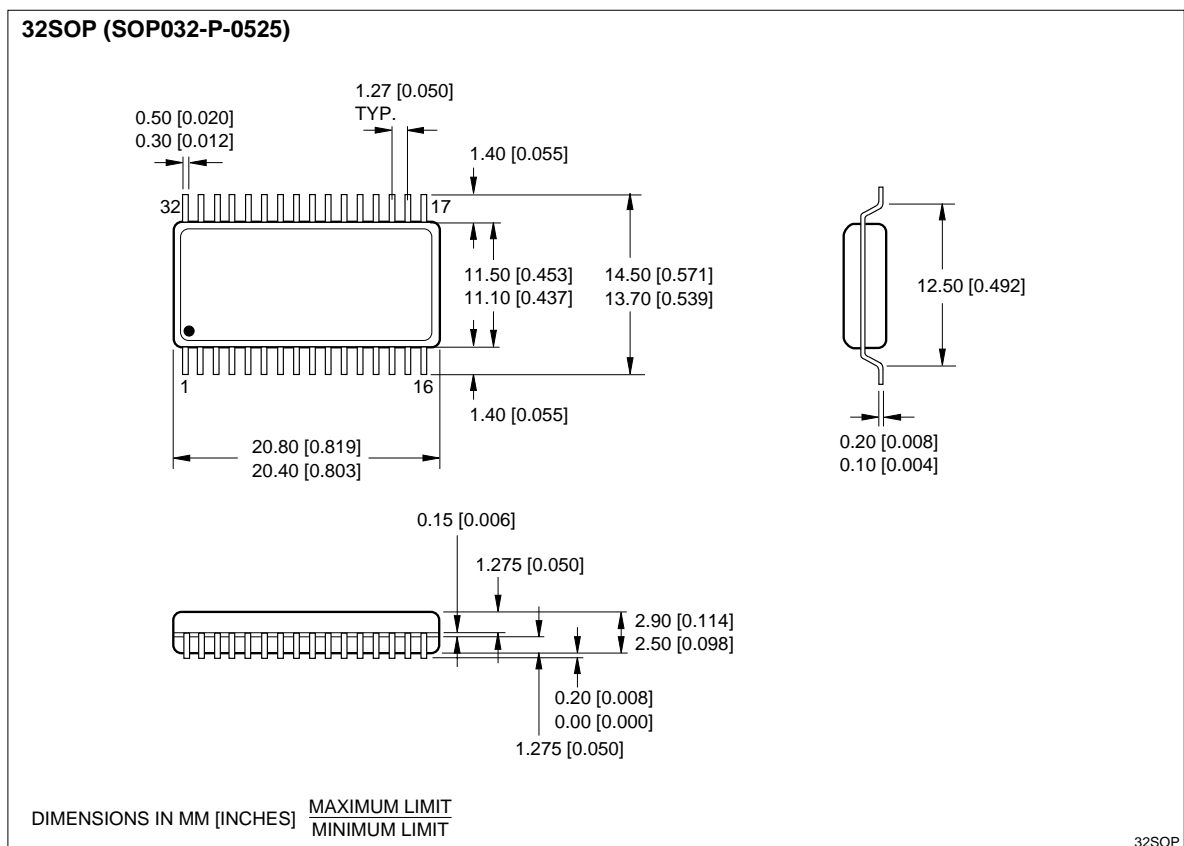


Figure 4. Timing Diagram

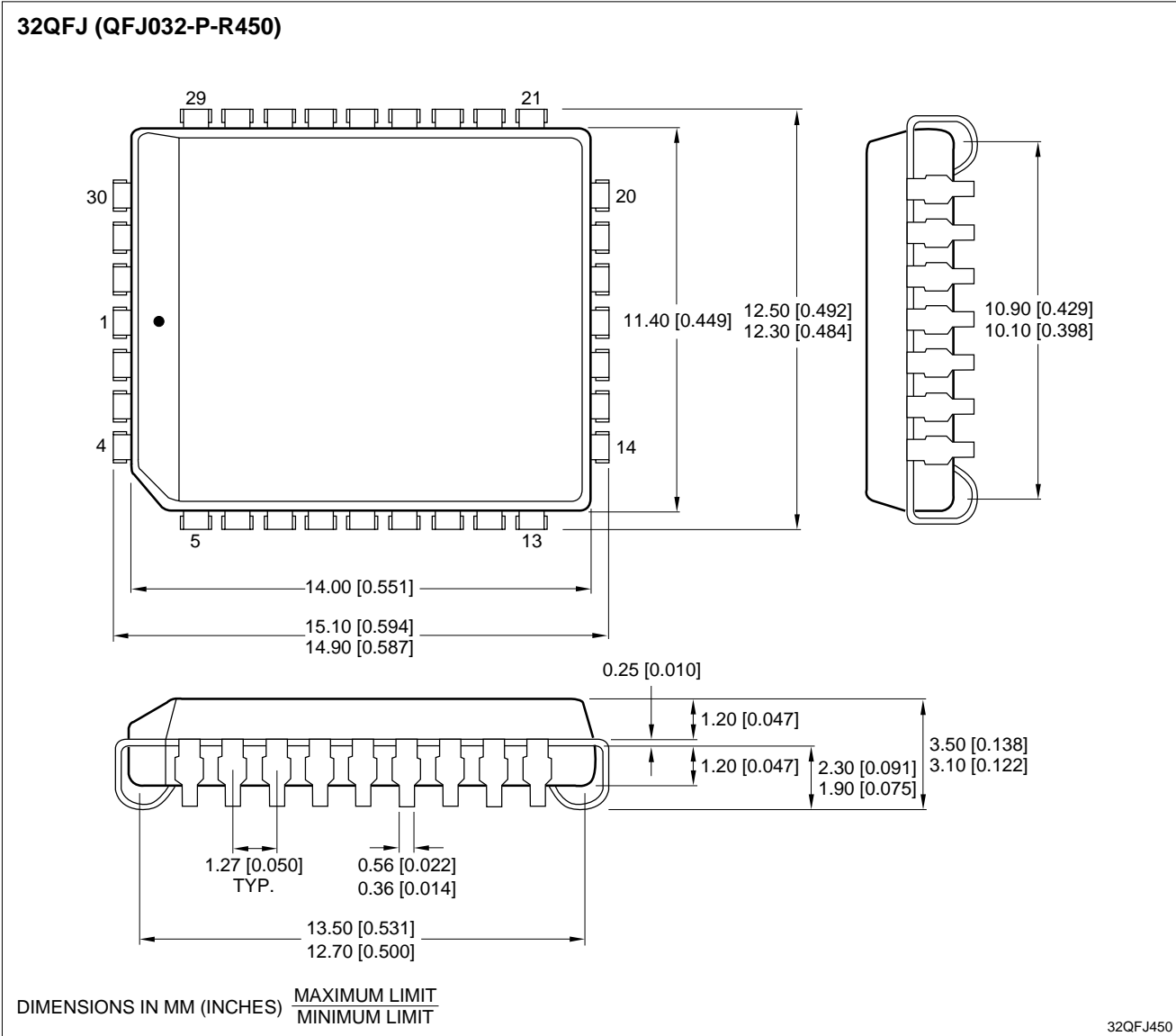
PACKAGE DIAGRAMS



32-pin, 600-mil DIP



32-pin, 525-mil SOP



32-pin, 450-mil QFJ (PLCC)

ORDERING INFORMATION

