

# LH5324C00

CMOS 24M (1.5M × 16) MROM

## FEATURES

- 1,572,864 × 16 bit organization
- Access time: 120 ns (MAX.)
- Supply current:
  - Operating: 80 mA (MAX.)
  - Standby: 100 μA (MAX.)
- TTL compatible I/O
- Three-state output
- Single +5 V Power supply
- Static operation
- When the address input at both A<sub>19</sub> and A<sub>20</sub> is high level, outputs become high impedance irrespective of CE or OE.
- Package:
  - 42-pin, 600-mil DIP
- Others:
  - Non programmable
  - Not designed or rated as radiation hardened
  - CMOS process (P type silicon substrate)

## PIN CONNECTIONS

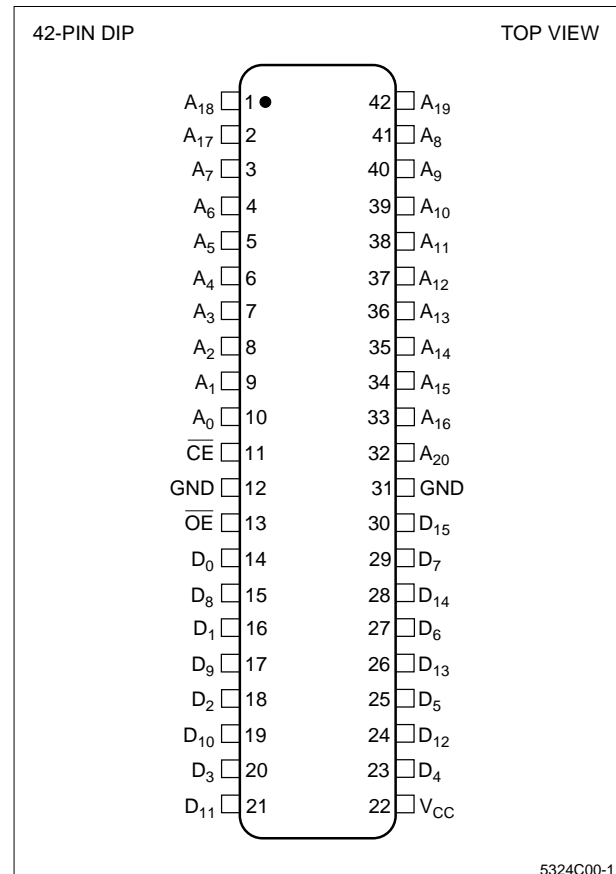
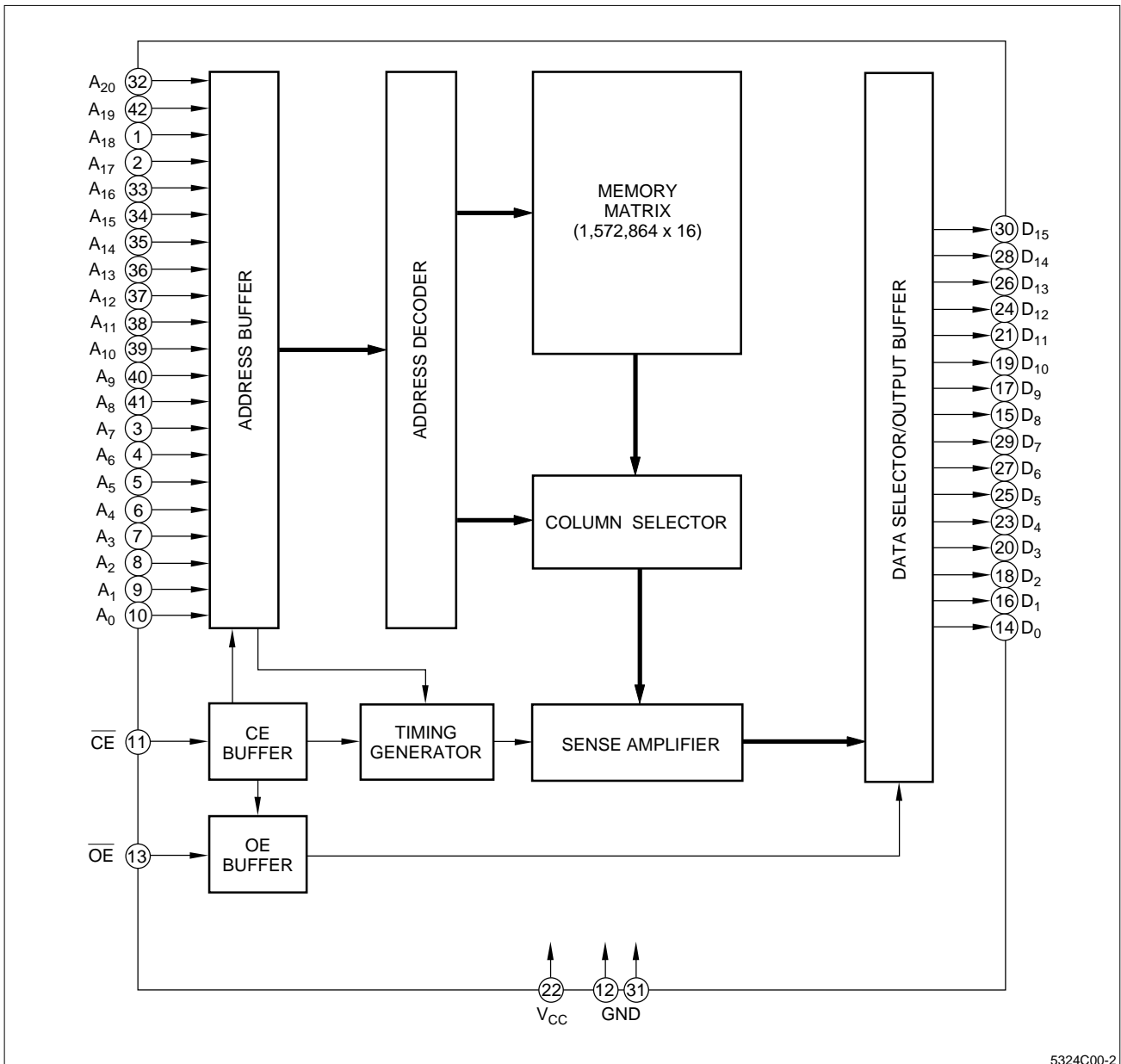


Figure 1. Pin Connections

## DESCRIPTION

The LH5324C00 is a 24M-bit mask-programmable ROM organized as 1,572,864 × 16 bits. It is fabricated using silicon-gate CMOS process technology.



5324C00-2

Figure 2. LH5324C00 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>20</sub>	Address input
D <sub>0</sub> - D <sub>15</sub>	Data output
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
OE	Output enable input
V <sub>CC</sub>	Power supply (+5 V)
GND	Ground

## TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	A <sub>0</sub> - A <sub>18</sub>	A <sub>19</sub>	A <sub>20</sub>	DATA OUTPUT	SUPPLY CURRENT
					D <sub>0</sub> - D <sub>15</sub>	
H	X	X	X	X	High-Z	Standby (I <sub>SB</sub> )
L	H	X	X	X	High-Z	Operating (I <sub>CC</sub> )
L	L	X	L	L	Output	Operating (I <sub>CC</sub> )
L	L	X	L	H	Output	Operating (I <sub>CC</sub> )
L	L	X	H	L	Output	Operating (I <sub>CC</sub> )
L	L	X	H	H	High-Z	Operating (I <sub>CC</sub> )

## NOTES:

- X = Don't care; High-Z = High-impedance
- When the address inputs become HIGH to both A<sub>19</sub> and A<sub>20</sub>, the data does not exist in this address area, the data outputs become "High Impedance".

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>OPR</sub>	0 to +70	°C
Storage temperature	T <sub>STG</sub>	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V <sub>IH</sub>	—	2.2	V <sub>CC</sub> + 0.3	V	—
Input 'Low' voltage	V <sub>IL</sub>	—	-0.3	0.8	V	—
Output 'High' voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4	—	V	—
Output 'Low' voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA	—	0.4	V	—
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	—	10	μA	—
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	—	10	μA	1
Operating current	I <sub>CC1</sub>	t <sub>RC</sub> = 120 ns	—	80	mA	2
	I <sub>CC2</sub>	t <sub>RC</sub> = 1 μs	—	70		
Standby current	I <sub>SB1</sub>	CE = V <sub>IH</sub>	—	2	mA	—
	I <sub>SB2</sub>	CE = V <sub>CC</sub> - 0.2 V	—	100		
Input capacitance	C <sub>IN</sub>	f = 1 MHz, t <sub>A</sub> = 25°C	—	10	pF	—
Output capacitance	C <sub>OUT</sub>		—	10	pF	—

## NOTES:

- CE = V<sub>IH</sub>, OE = V<sub>IH</sub>
- V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>, CE = V<sub>IL</sub>, output is open

**AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +5\text{ V} \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	120	—	ns	—
Address access time	$t_{AA}$	—	120	ns	—
Chip enable access time	$t_{ACE}$	—	120	ns	—
Output enable delay time	$t_{OE}$	—	60	ns	—
Output hold time	$t_{OH}$	0	—	ns	—
Output floating time	$t_{CHZ}$	—	50	ns	1
	$t_{OHZ}$	—	50	ns	
	$t_{AHZ}$	—	60	ns	

**NOTE:**

1. Determined by the time for the output to be opened. (Irrespective of output voltage)

**AC TEST CONDITIONS**

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

**NOTE:**

It is recommended that a decoupling capacitor be connected between  $V_{CC}$  and GND-Pin.

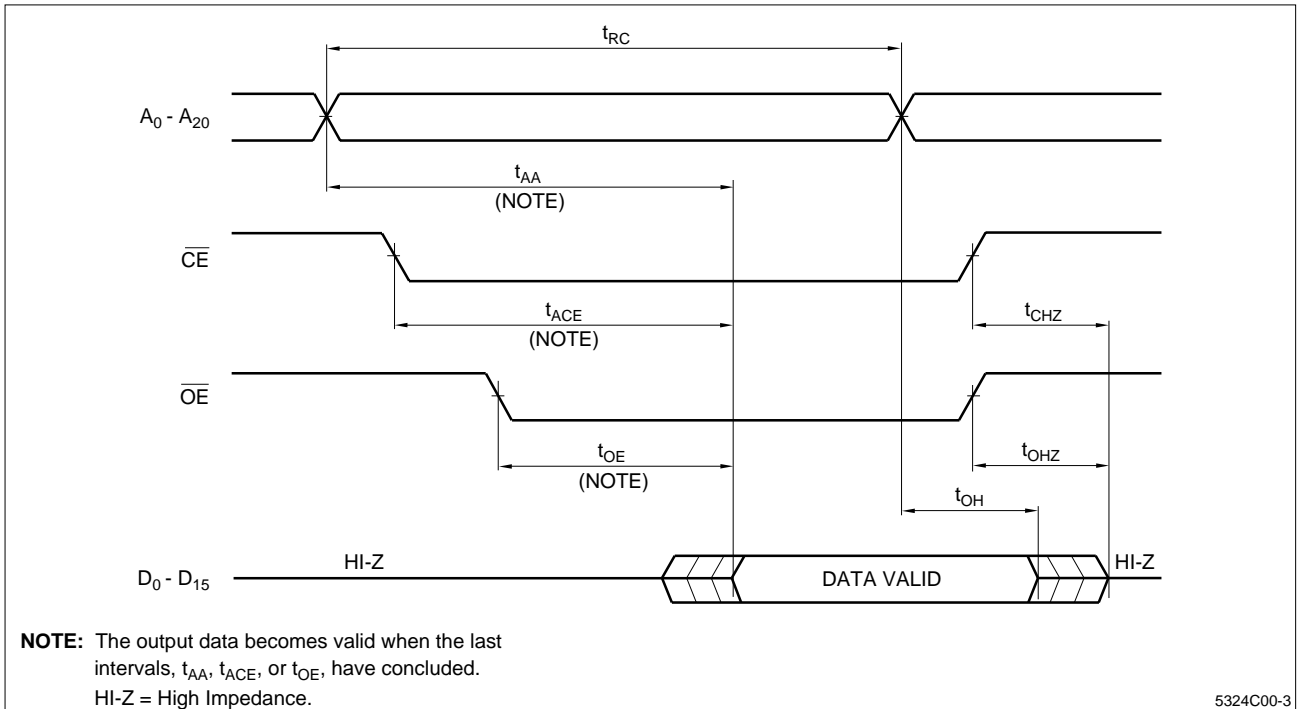


Figure 3. Byte Mode

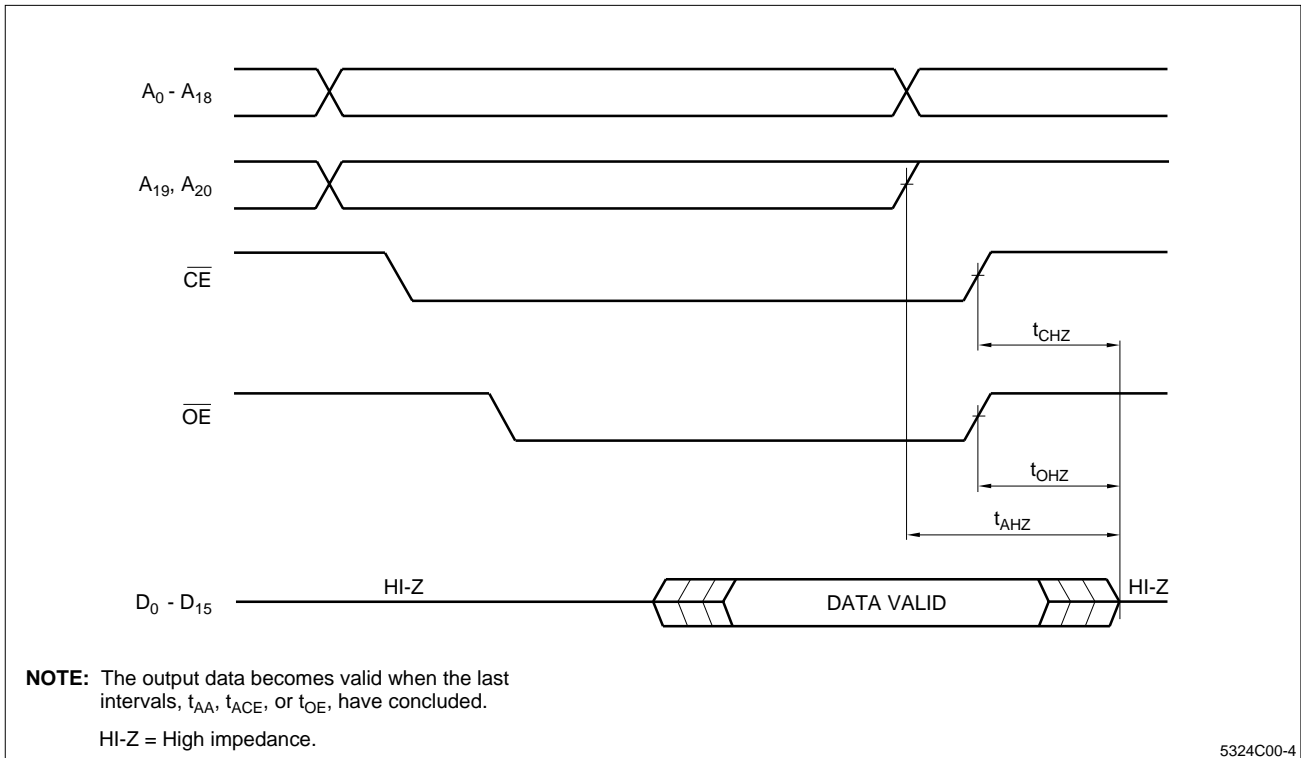


Figure 4. Word Mode

