LH5496/96H

CMOS 512 × 9 FIFO

FEATURES

- Fast Access Times:
  15 */20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable-in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil PDIP
  28-Pin, 600-mil PDIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7201

FUNCTIONAL DESCRIPTION

The LH5496/96H are dual port memories with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, they provide fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic provides for unlimited expansion in both word size and depth.

Read and write operations automatically access sequential locations in memory in that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

* LH5496 only.

PIN CONNECTIONS

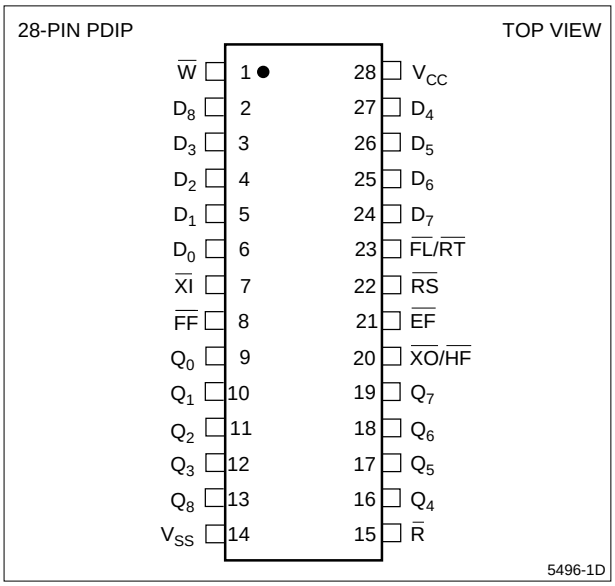


Figure 1. Pin Connections for PDIP Packages

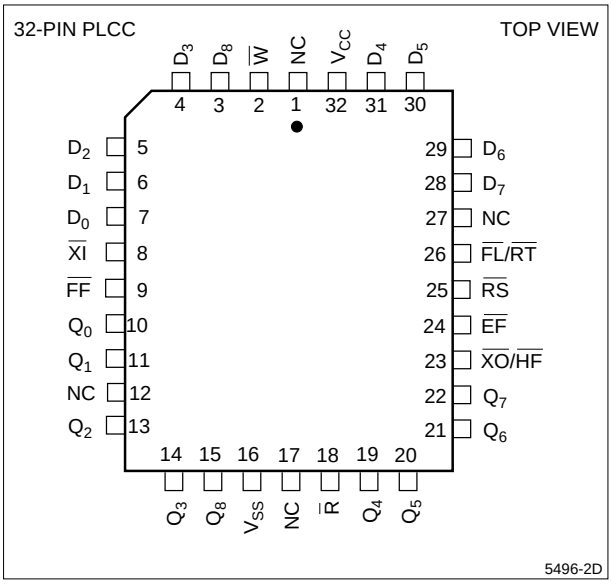


Figure 2. Pin Connections for PLCC Package

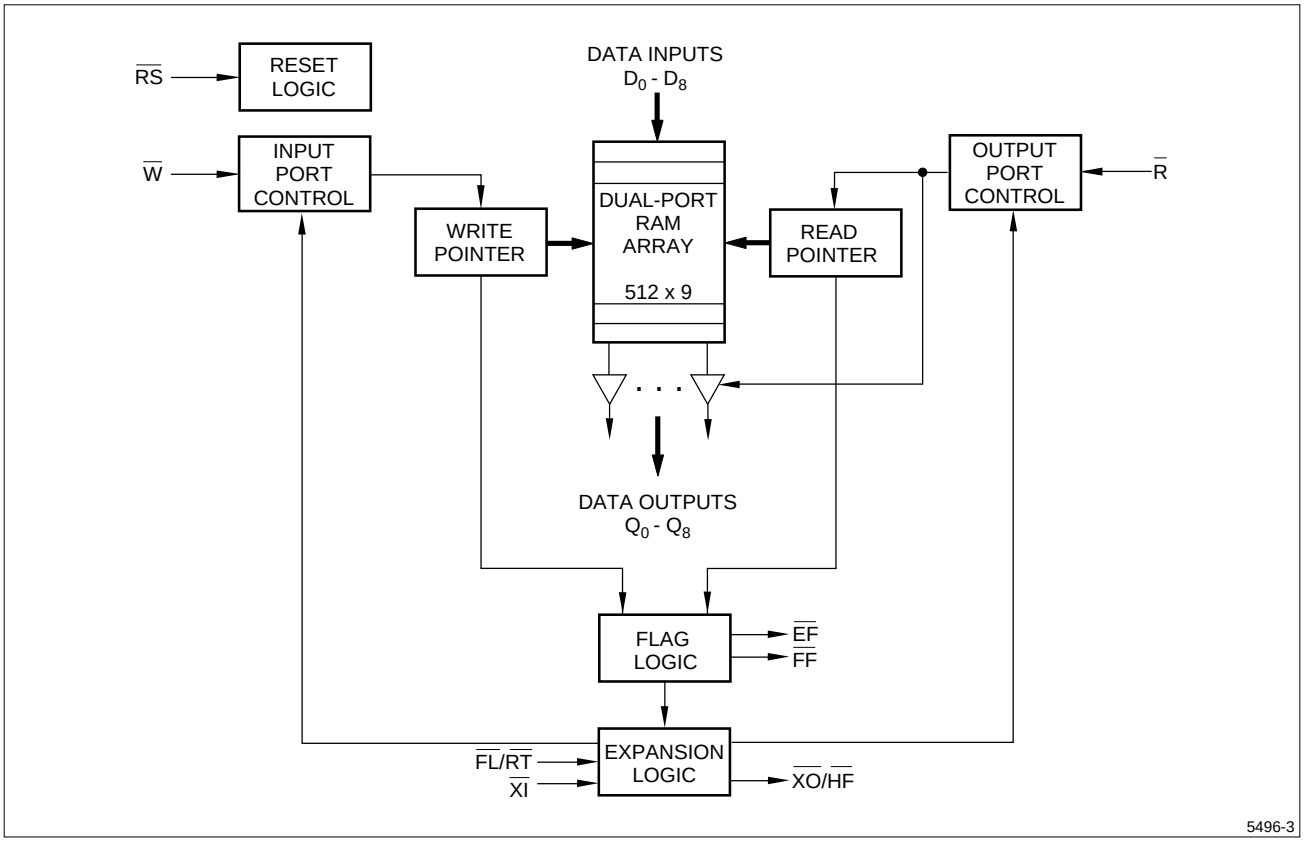


Figure 3. LH5496/96H Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 – D_8$	I	Input Data Bus
$Q_0 – Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	–0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	–0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	±50 mA
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied To Outputs In High-Z State	–0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a device stress rating for transient conditions only. Functional operation at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient, LH5496	0	70	°C
T_A	Temperature, Ambient, LH5496H	–40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	–0.5	0.8	V
V_{IH}	Logic '1' Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	–10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	–10	10	µA
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} – 0.2 V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

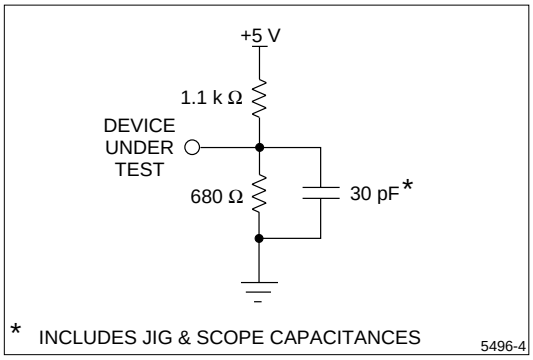


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns [2]		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [3]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [4]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [4,5]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [4]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [3]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [3]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [3]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. LH5496 only.
2. All timing measurements performed at 'AC Test Condition' levels.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$. The reset operation forces the Empty Flag $\overline{EF}$ to be asserted ($\overline{EF}$ = LOW), and the Half-Full Flag $\overline{HF}$ and the Full FLag $\overline{FF}$ to be deasserted ($\overline{HF}$ = $\overline{FF}$ = HIGH); the Data Out pins ($D_0 - D_8$) are forced into a high-impedance state.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read opertations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

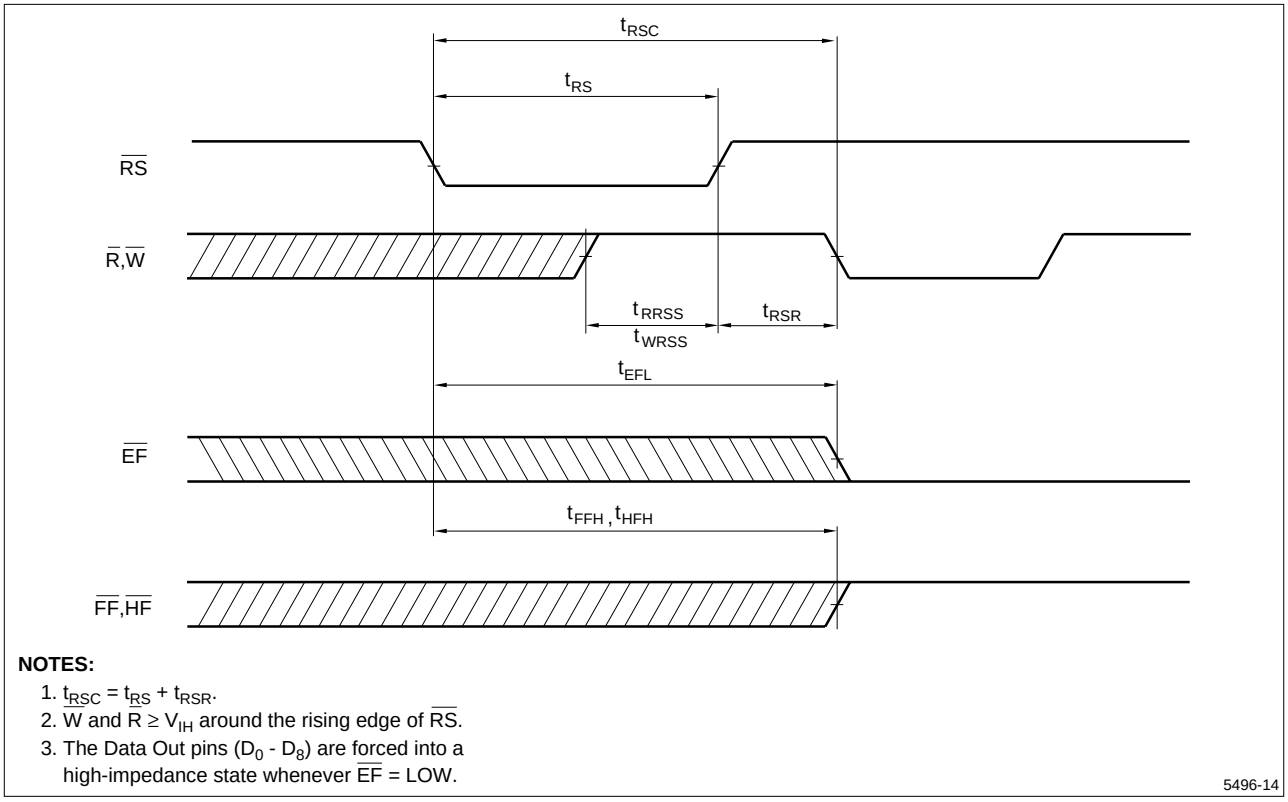
Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 512 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

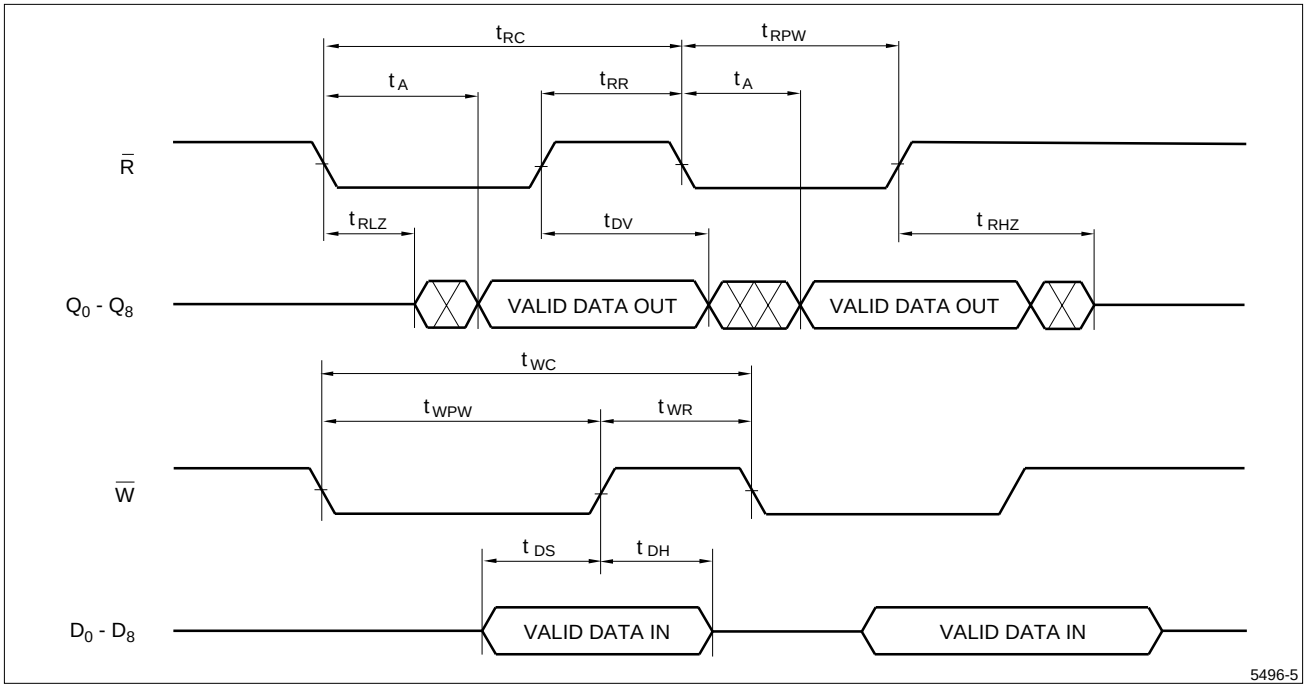


NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{RS}$.
3. The Data Out pins (D_0 - D_8) are forced into a high-impedance state whenever $\overline{EF}$ = LOW.

5496-14

Figure 5. Reset Timing



5496-5

Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

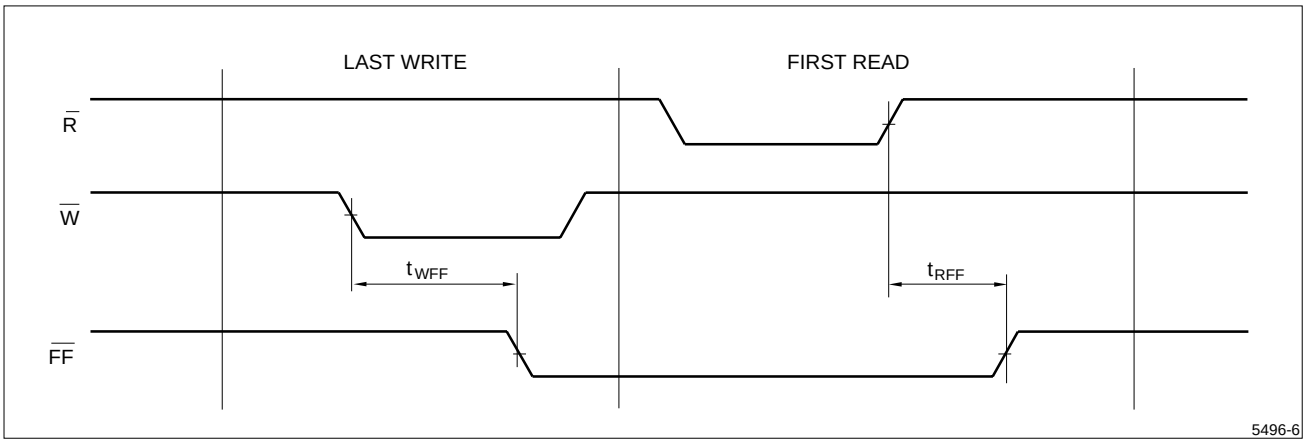
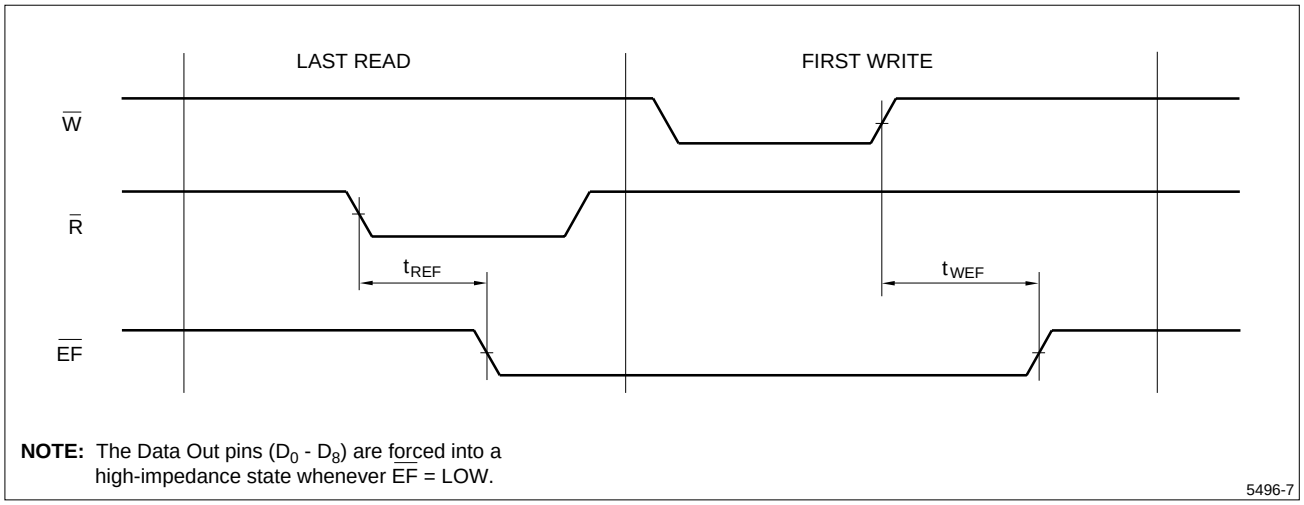


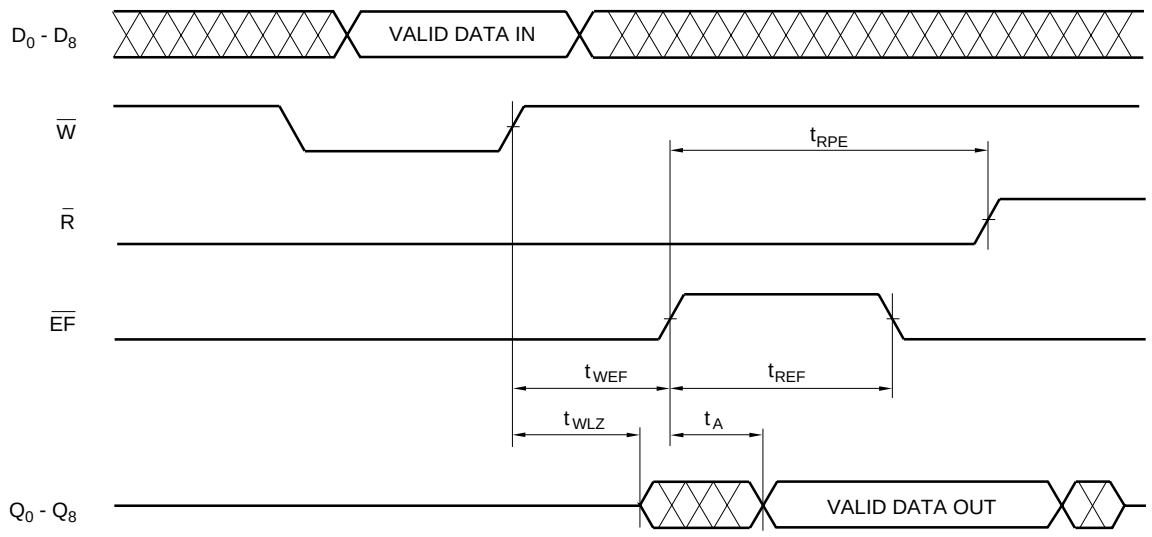
Figure 7. Full Flag from Last Write to First Read



NOTE: The Data Out pins (D_0 - D_8) are forced into a high-impedance state whenever $\overline{EF}$ = LOW.

Figure 8. Empty Flag from Last Read to First Write

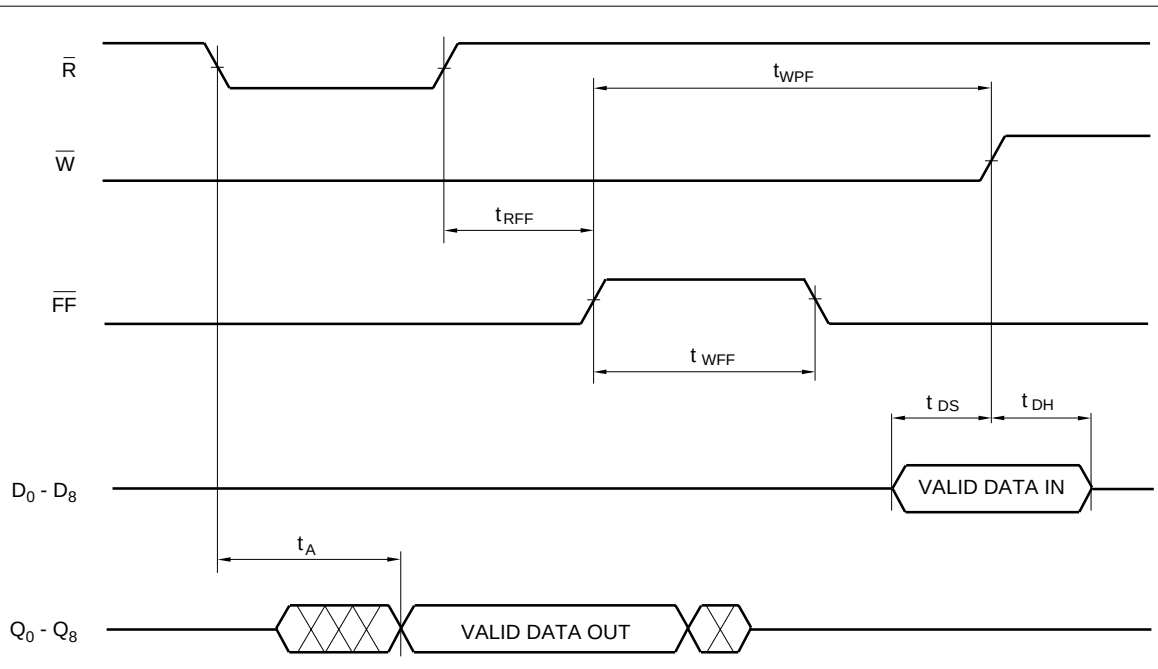
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.
3. The Data Out pins (D_0 - D_8) are forced into a high-impedance state whenever $\overline{EF}$ = LOW.

5496-8

Figure 9. Read Data Flow-Through

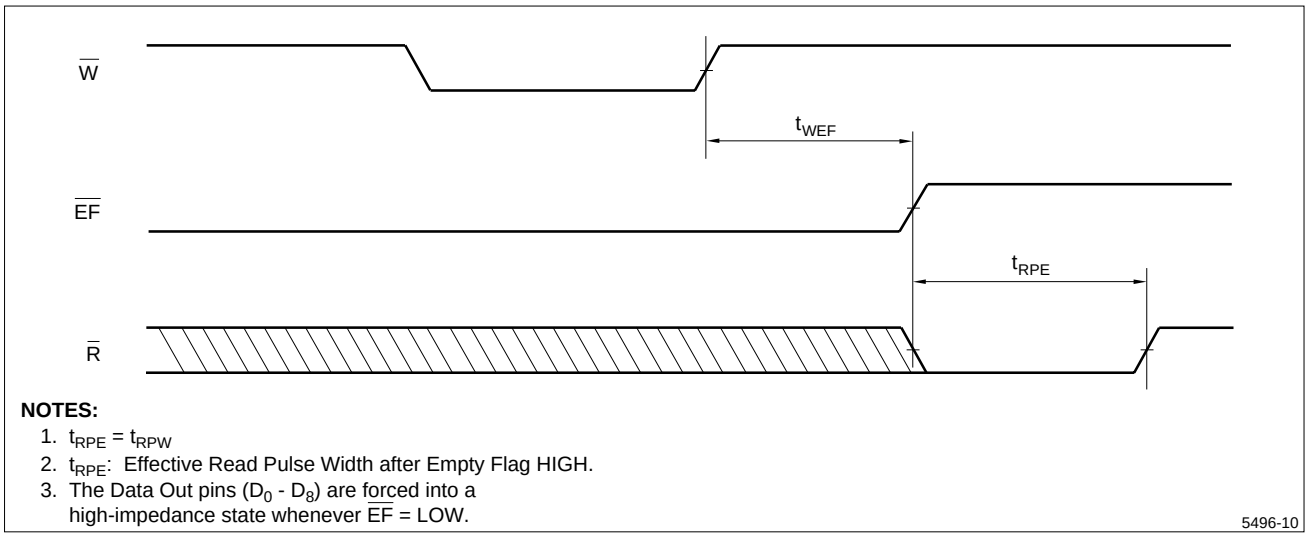


NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

5496-9

Figure 10. Write Data Flow-Through

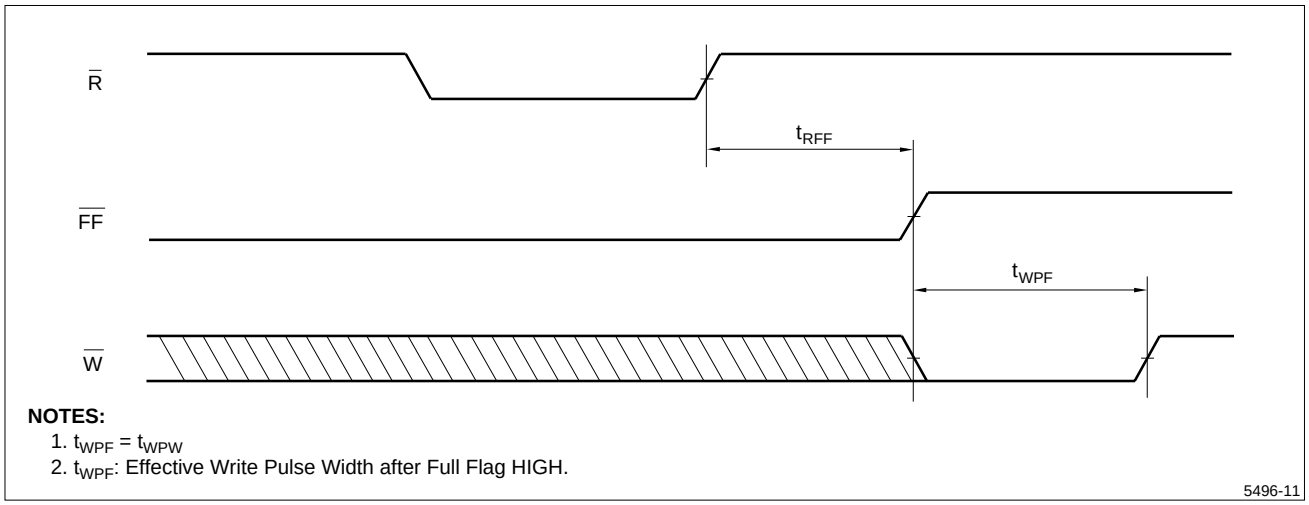
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.
3. The Data Out pins (D_0 - D_8) are forced into a high-impedance state whenever $\overline{EF}$ = LOW.

5496-10

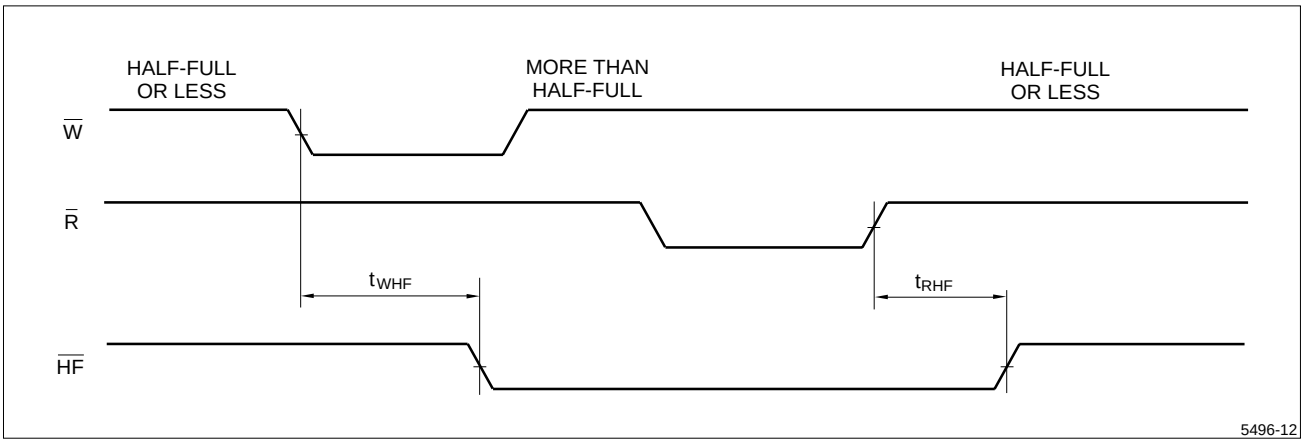
Figure 11. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

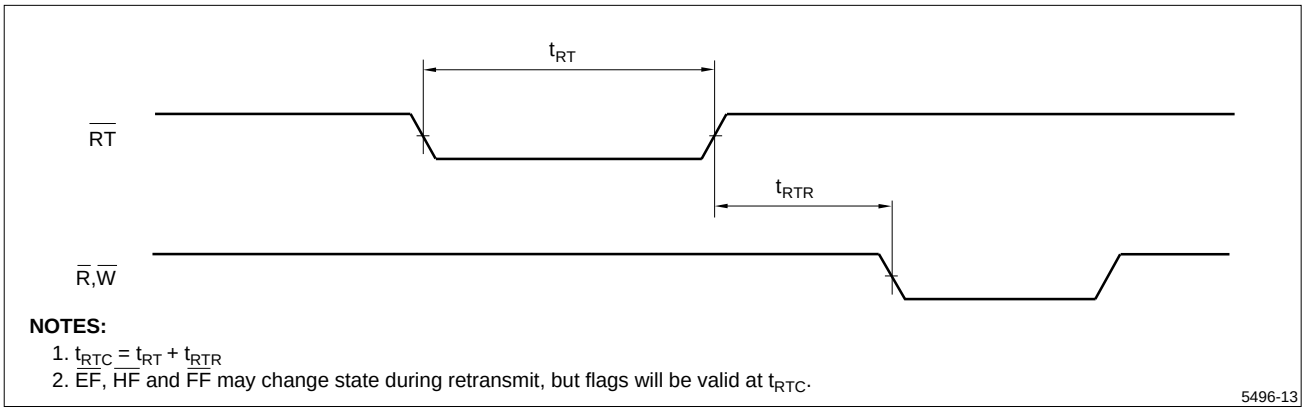
5496-11

Figure 12. Full Flag Timing



5496-12

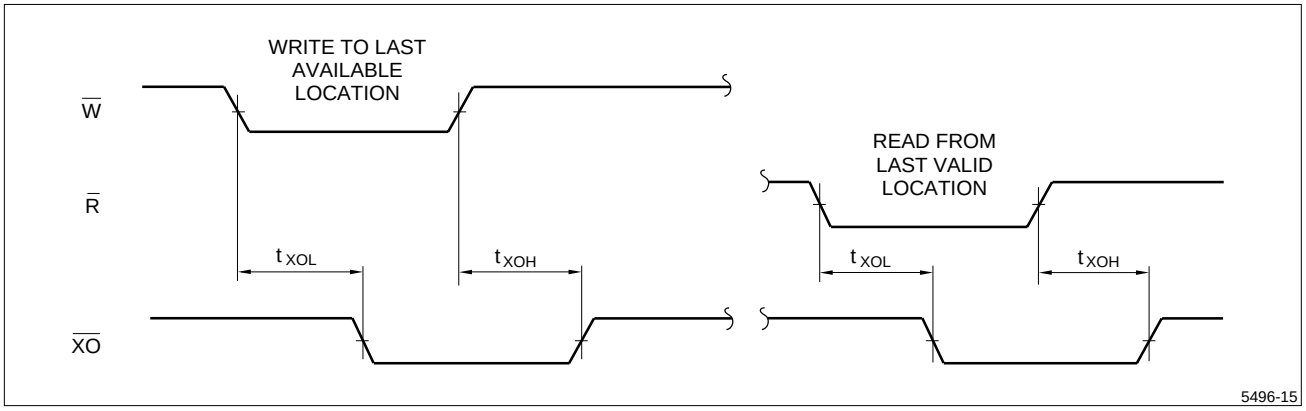
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit, but flags will be valid at t_{RTC}.

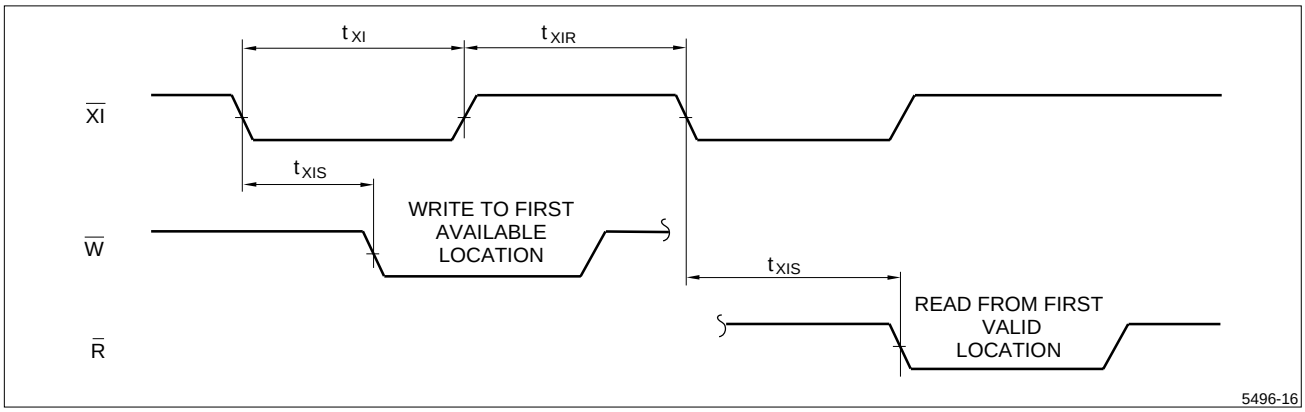
5496-13

Figure 14. Retransmit Timing



5496-15

Figure 15. Expansion Out Timing



5496-16

Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5496/96H devices in parallel. Each LH5496/96H should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

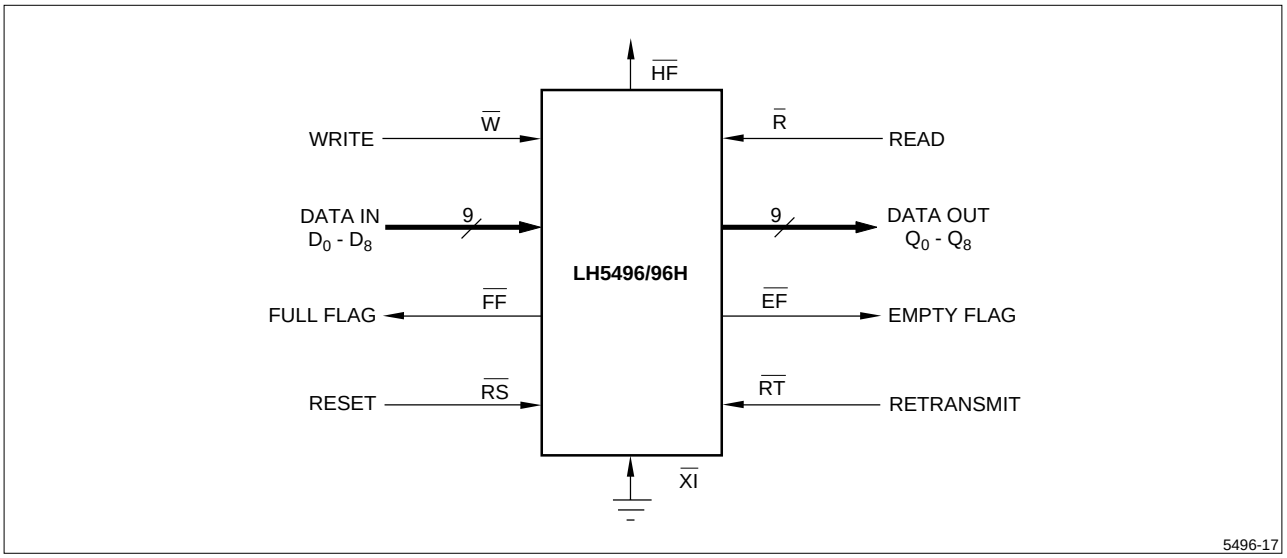


Figure 17. Single FIFO (512 × 9)

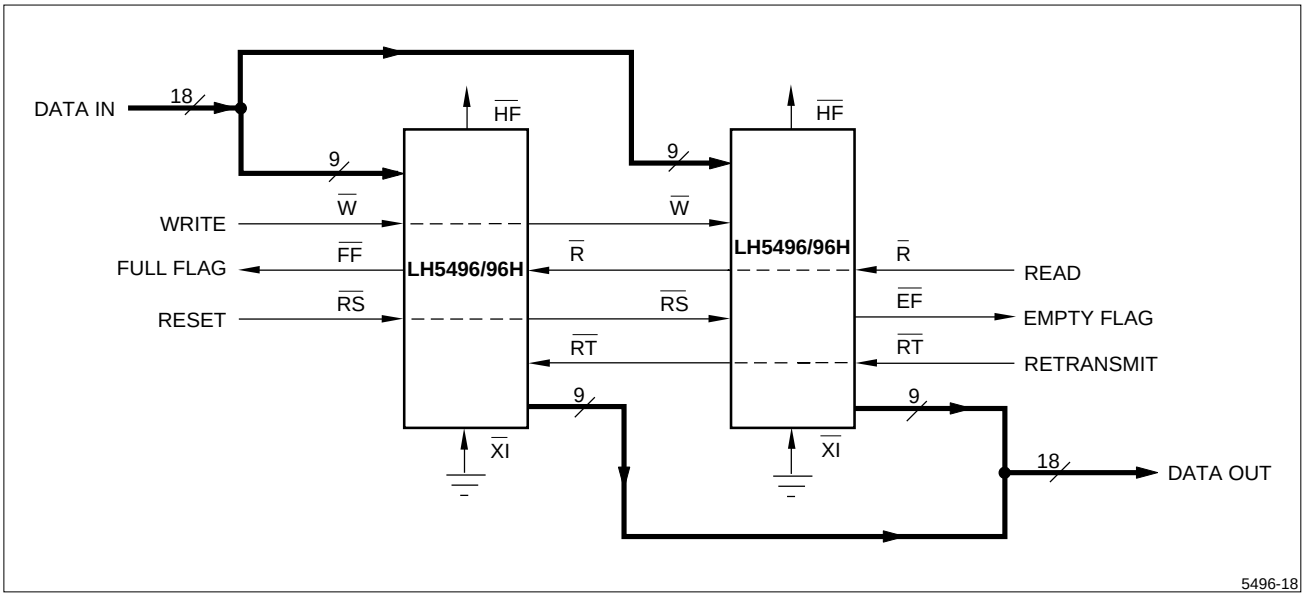


Figure 18. FIFO Width Expansion (512 × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

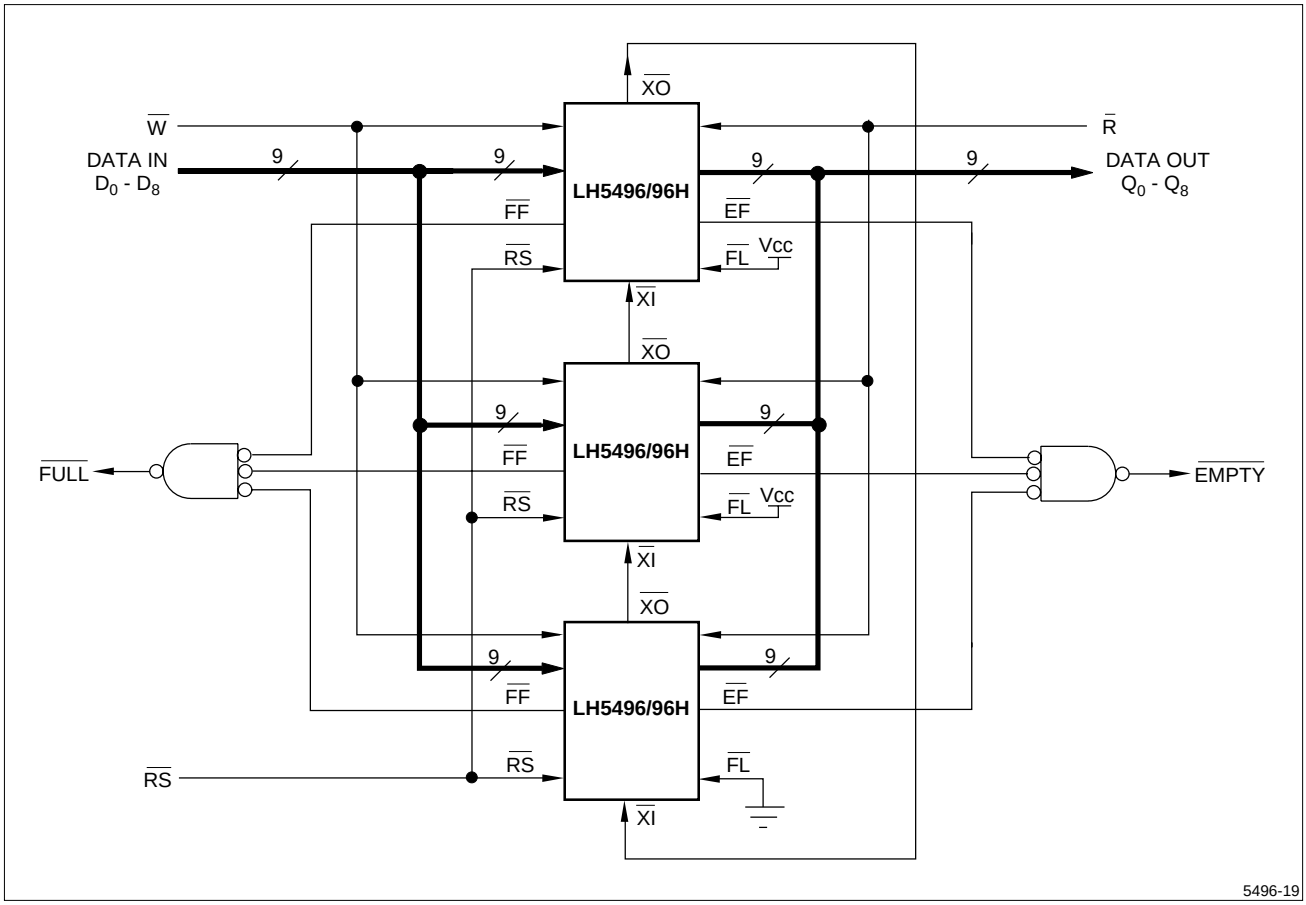


Figure 19. FIFO Depth Expansion (1536 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5496/96H devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

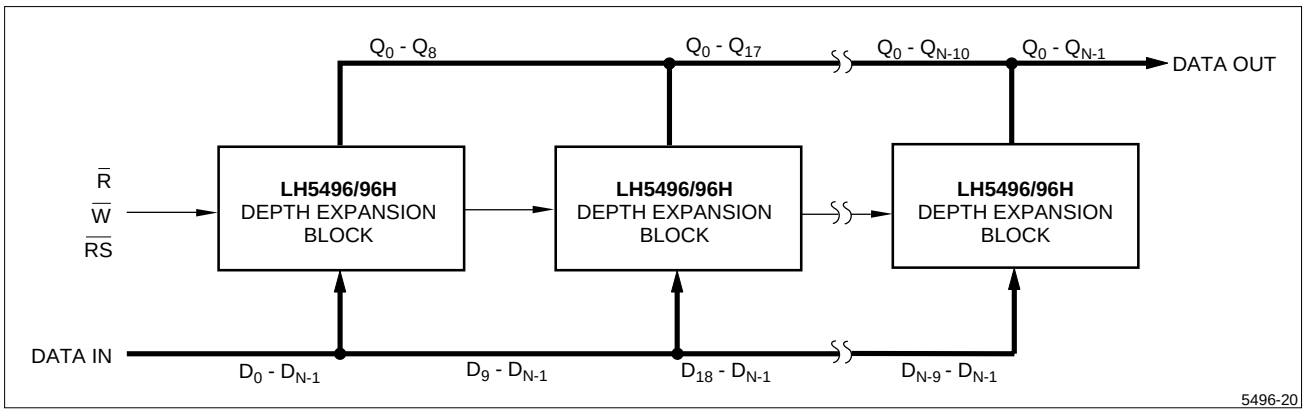


Figure 20. Compound FIFO Expansion

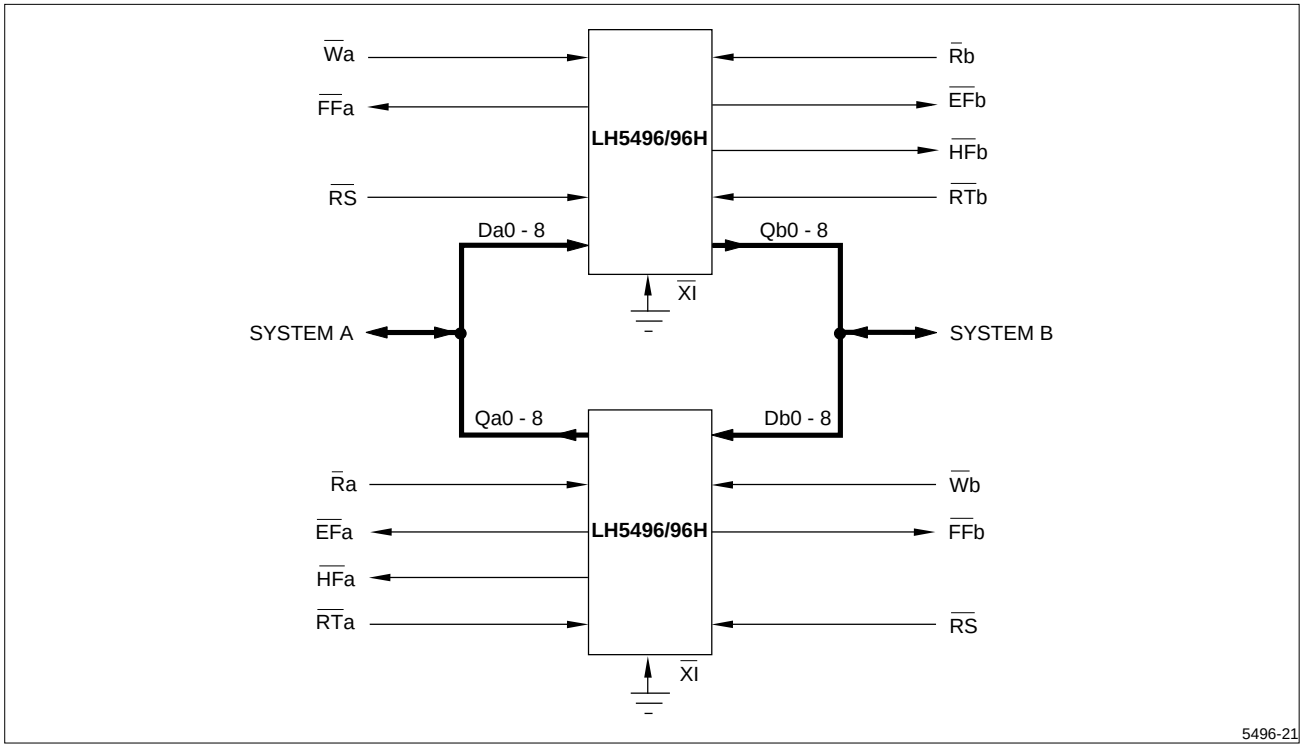
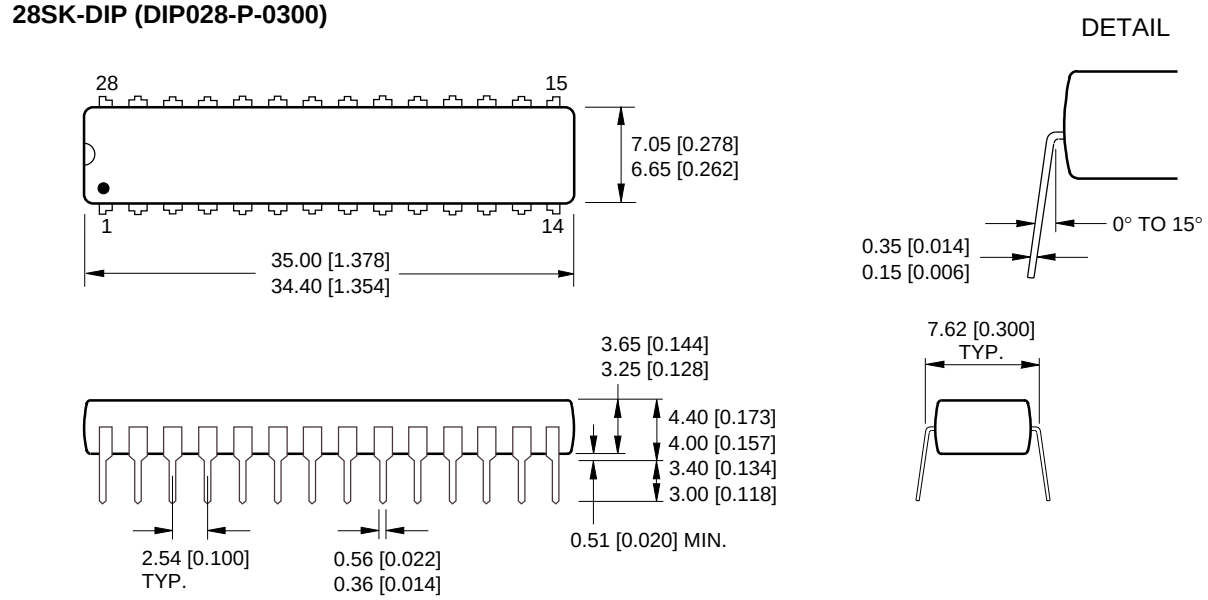


Figure 21. Bidirectional FIFO Buffer

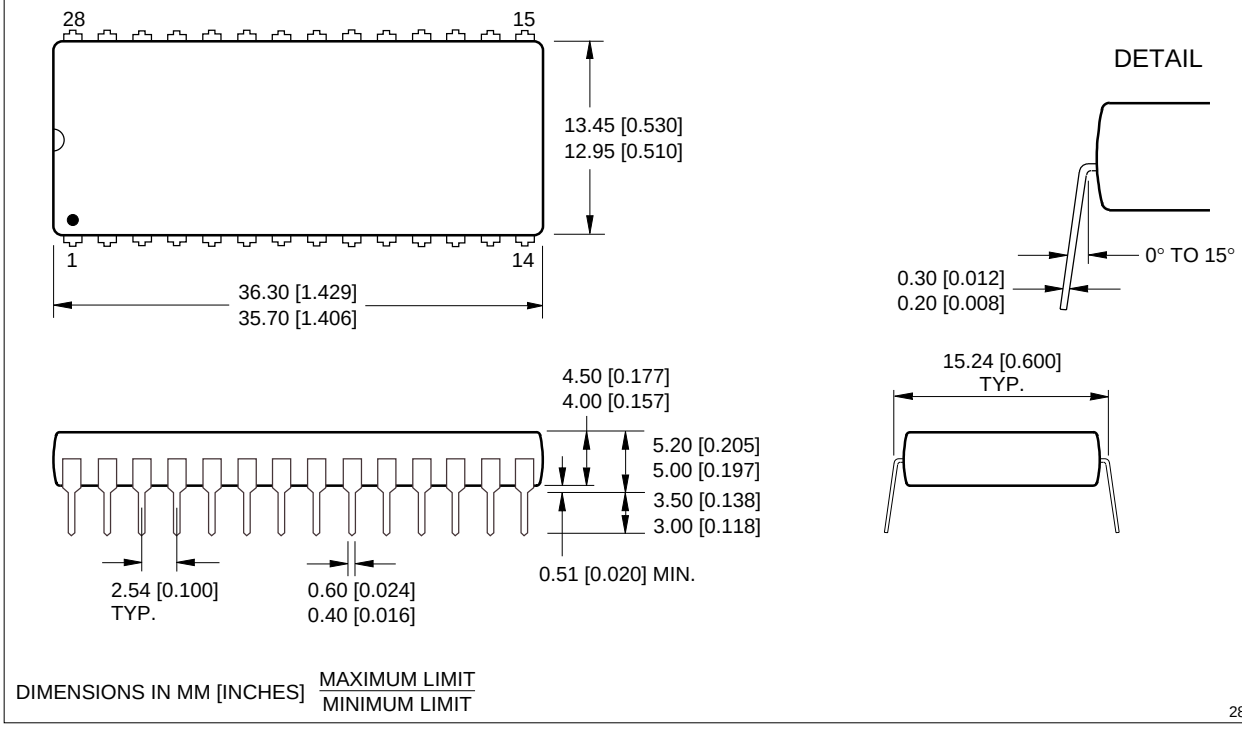
PACKAGE DIAGRAMS

28SK-DIP (DIP028-P-0300)



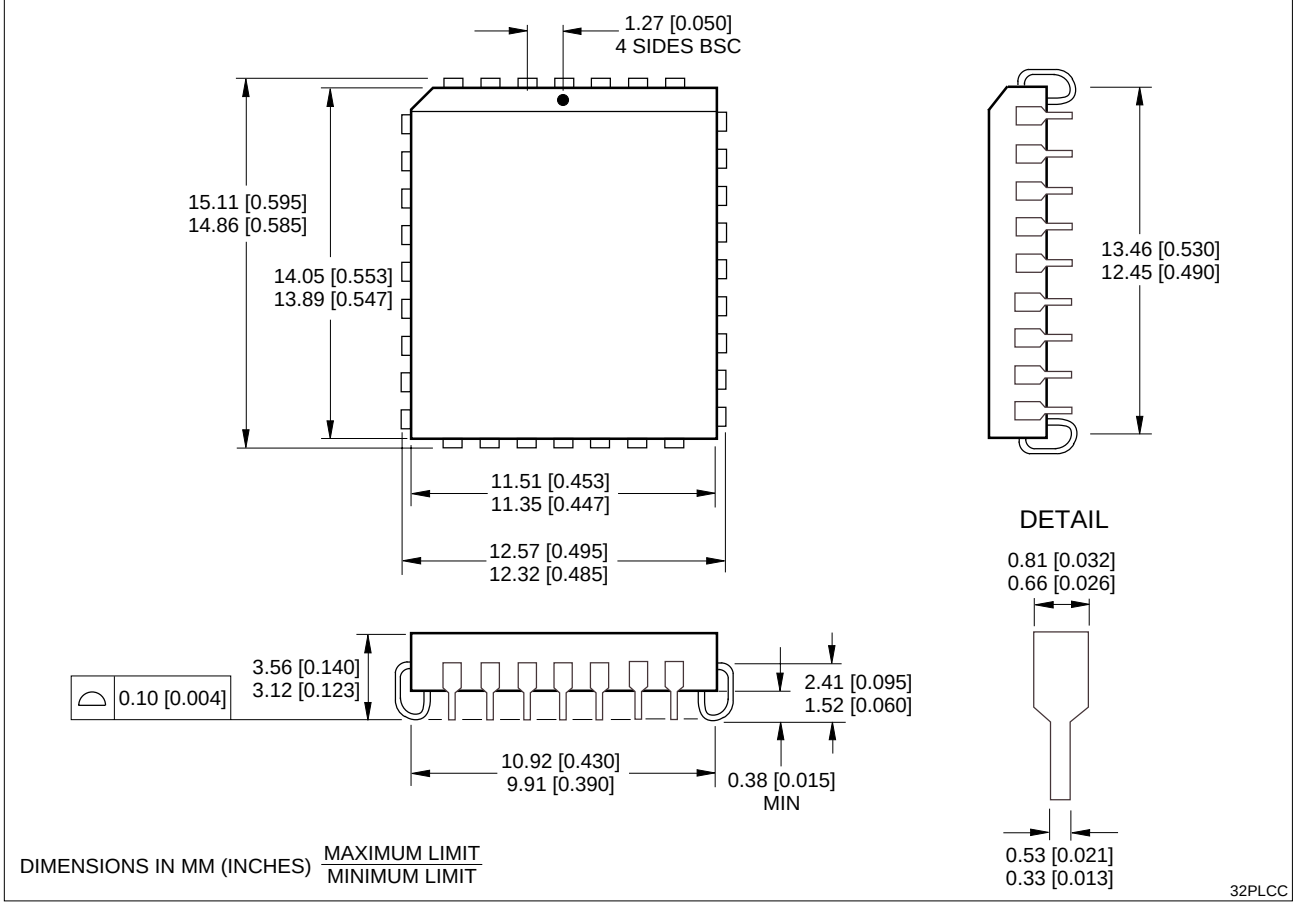
28-pin, 300-mil PDIP

28DIP (DIP028-P-0600)



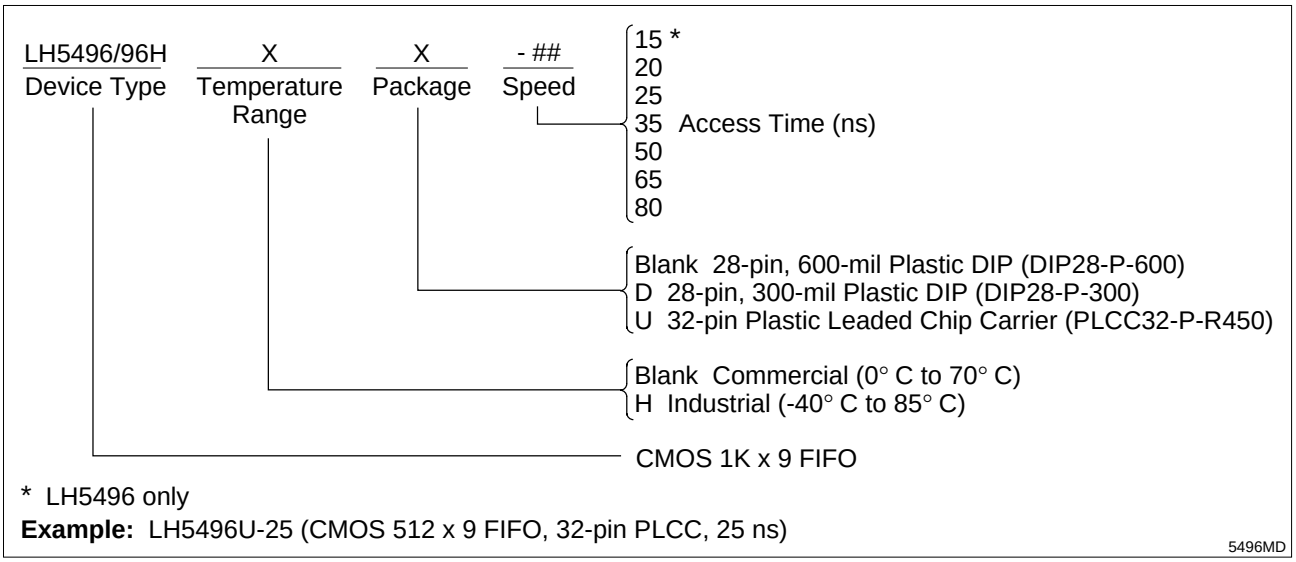
28-pin, 600-mil PDIP

32PLCC (PLCC32-P-R450)



32-pin, 450-mil PLCC

ORDERING INFORMATION



* LH5496 only

Example: LH5496U-25 (CMOS 512 x 9 FIFO, 32-pin PLCC, 25 ns)

5496MD