LH28F160BG-TL/BGH-TL

16 M-bit (1 MB x 16) Smart 3 Flash Memories

DESCRIPTION

The LH28F160BG-TL/BGH-TL flash memories with Smart 3 technology are high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. The LH28F160BG-TL/ BGH-TL can operate at V_{CC} and V_{PP} = 2.7 V. Their low voltage operation capability realizes longer battery life and suits for cellular phone application. Their boot, parameter and main-blocked architecture, flexible voltage and enhanced cycling capability provide for highly flexible component suitable for portable terminals and personal computers. Their enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F160BG-TL/BGH-TL offer two levels of protection : absolute protection with V_{PP} at GND, selective hardware boot block locking. These alternatives give designers ultimate control of their code security needs.

FEATURES

- Smart 3 technology
  - 2.7 to 3.6 V V_{CC}
  - 2.7 to 3.6 V or 12 V V_{PP}
- High performance read access time
  LH28F160BG-TL10/BGH-TL10
  - 100 ns (2.7 to 3.6 V)
  LH28F160BG-TL12/BGH-TL12
  - 120 ns (2.7 to 3.6 V)
- Enhanced automated suspend options
  - Word write suspend to read
  - Block erase suspend to word write
  - Block erase suspend to read
- SRAM-compatible write interface
- Optimized array blocking architecture
  - Two 4 k-word boot blocks
  - Six 4 k-word parameter blocks
  - Thirty-one 32 k-word main blocks
  - Top or bottom boot location
- Enhanced cycling capability
  - 100 000 block erase cycles
- Low power management
  - Deep power-down mode
  - Automatic power saving mode decreases I_{CC} in static mode
- Automated word write and block erase
  - Command user interface
  - Status register
- ETOX™* V nonvolatile flash technology
- Packages
  - 48-pin TSOP Type I (TSOP048-P-1220) Normal bend/Reverse bend
  - 60-ball CSP (FBGA060/048-P-0811)

* ETOX is a trademark of Intel Corporation.

COMPARISON TABLE

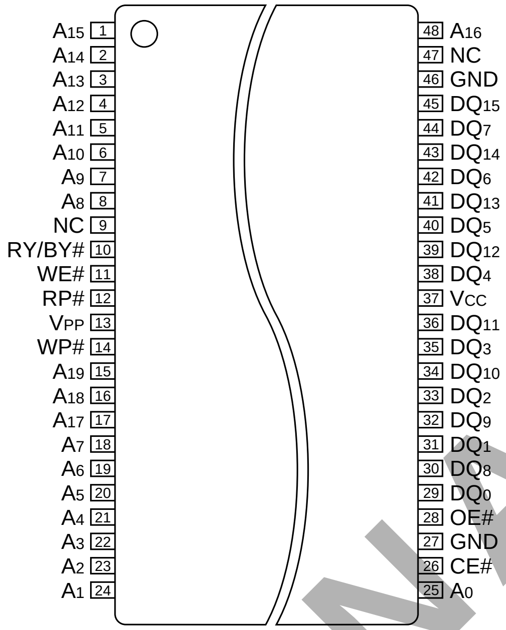
VERSIONS	BIT CONFIGURATION	OPERATING TEMPERATURE
LH28F160BG-TL	1 MB x 16	0 to +70°C
LH28F160BGH-TL	1 MB x 16	–25 to +85°C
LH28F160BV-TL*	2 MB x 8/1 MB x 16	0 to +70°C
LH28F160BVH-TL*	2 MB x 8/1 MB x 16	–40 to +85°C

* Refer to the datasheet of LH28F160BV-TL/BVH-TL.

PIN CONNECTIONS

48-PIN TSOP (Type I)

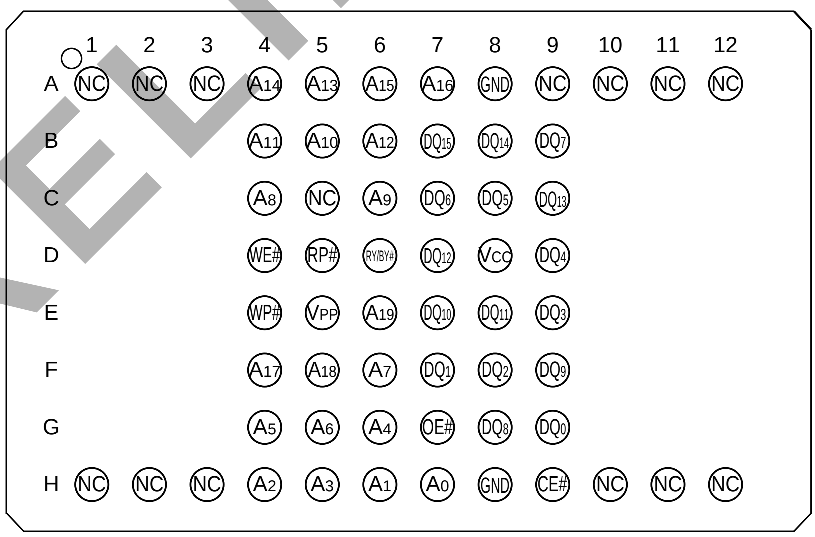
TOP VIEW



(TSOP048-P-1220)

NOTE :
Reverse bend available on request.

60-BALL CSP



(FBGA060/048-P-0811)

BLOCK ORGANIZATION

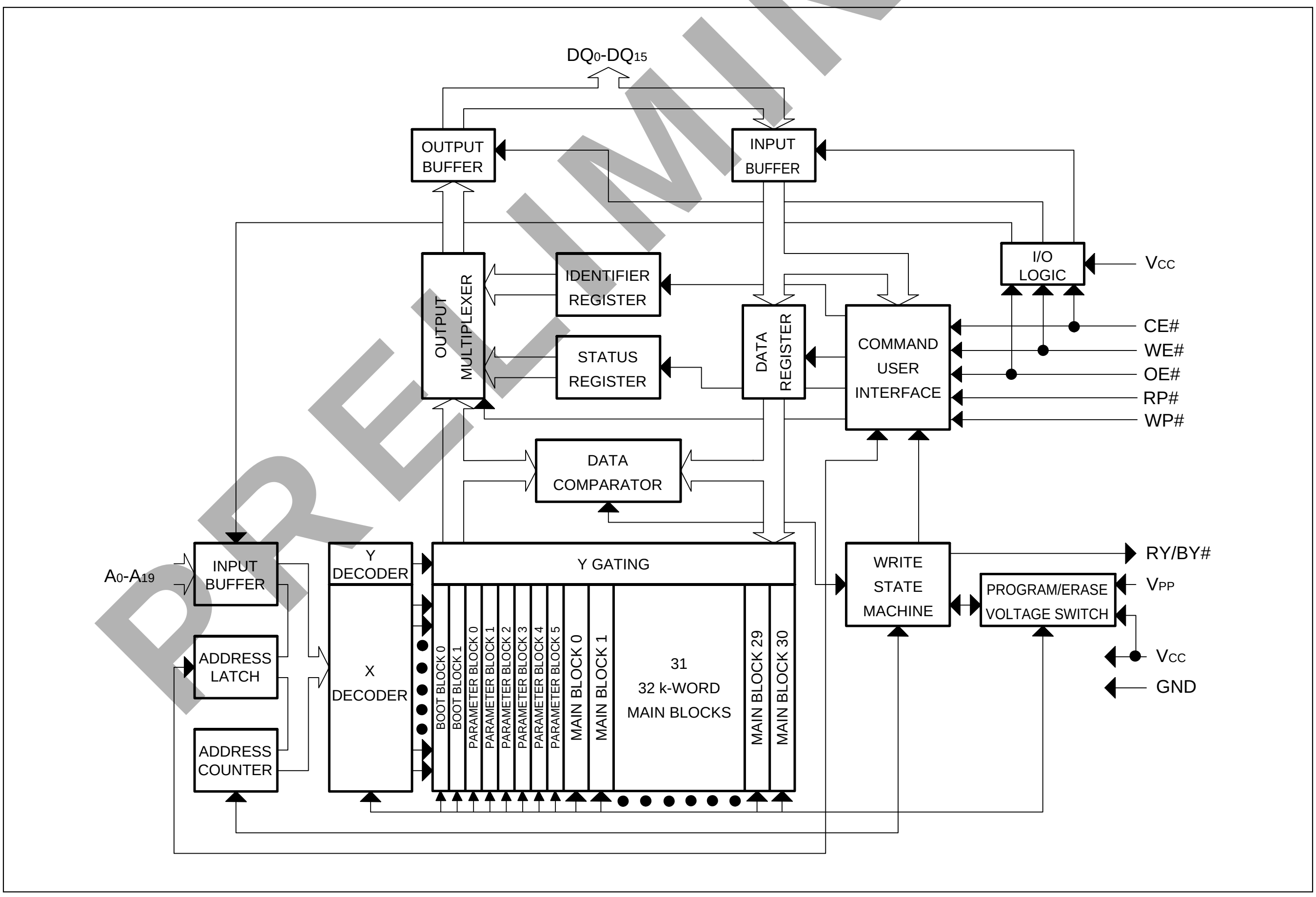
This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100 000 times. For the address locations of the blocks, see the memory map in **Fig. 1**.

Boot Blocks : The two boot blocks are intended to replace a dedicated boot PROM in a micro-processor or microcontroller-based system. The boot blocks of 4 k words (4 096 words) feature hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot blocks is controlled using a combination of the V_{PP}, RP# and WP# pins.

Parameter Blocks : The boot block architecture includes parameter blocks to facilitate storage of frequently update small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. Each boot block component contains six parameter blocks of 4 k words (4 096 words) each. The parameter blocks are not write-protectable.

Main Blocks : The reminder is divided into main blocks for data or code storage. Each 16 M-bit device contains thirty-one 32 k words (32 768 words) blocks.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A_0-A_{19}	INPUT	**ADDRESS INPUTS :** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
DQ_0-DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS :** Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE :** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	**RESET/DEEP POWER-DOWN :** Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provide data protection during power transitions. Exit from deep power-down sets the device to read array mode. Block erase or word write with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.
OE#	INPUT	**OUTPUT ENABLE :** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE :** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	**WRITE PROTECT :** Master control for boot blocks locking. When V_{IL}, locked boot blocks cannot be erased and programmed.
RY/BY#	OUTPUT	**READY/BUSY :** Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase or word write). RY/BY#-high-impedance indicates that the WSM is ready for new commands, block erase is suspended, and word write is inactive, word write is suspended, or the device is in deep power-down mode.
V_{PP}	SUPPLY	**BLOCK ERASE AND WORD WRITE POWER SUPPLY :** For erasing array blocks or writing words. With $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. Block erase and word write with an invalid V_{PP} (see **Section 6.2.3 "DC CHARACTERISTICS"**) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY :** 2.7 to 3.6 V. Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see **Section 6.2.3 "DC CHARACTERISTICS"**) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND :** Do not float any ground pins.
NC		**NO CONNECT :** Lead is not internal connected; recommend to be floated.

1 INTRODUCTION

This datasheet contains LH28F160BG-TL/BGH-TL specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications. LH28F160BG-TL/BGH-TL flash memories documentation also includes ordering information which is referenced in Section 7.

1.1 New Features

Key enhancements of LH28F160BG-TL/BGH-TL Smart 3 flash memories are :

- 2.7 V V_{CC} and V_{PP} Write/Erase Operation
- Enhanced Suspend Capabilities
- Boot Block Architecture

Note following important differences :

- V_{PPLK} has been lowered to 1.5 V to support 2.7 V block erase and word write operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- To take advantage of Smart 3 technology, allow V_{PP} connection to 2.7 V or 12 V.

1.2 Product Overview

The LH28F160BG-TL/BGH-TL are high-performance 16 M-bit Smart 3 flash memories organized as 1 024 k-word of 16 bits. The 1 024 k-word of data is arranged in two 4 k-word boot blocks, six 4 k-word parameter blocks and thirty-one 32 k-word main blocks which are individually erasable in-system. The memory map is shown in **Fig. 1**.

V_{PP} at 2.7 V eliminates the need for a separate 12 V converter, while V_{PP} = 12 V maximizes block erase and word write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word write operations.

A block erase operation erases one of the device's 32 k-word blocks typically within 1.2 second (3.0 V V_{CC} and V_{PP}), independent of other blocks. Each block can be independently erased 100 000 times. Block erase suspend mode allows system software to suspend block erase to read data from, or write data to any other block.

Writing memory data is performed in word increments of the device's 32 k-word blocks typically within 55 µs, 4 k-word blocks typically within 60 µs (3.0 V V_{CC} and V_{PP}). Word write suspend mode enables the system to read data from, or write data to any other flash memory array location.

The boot block is located at either the top or the bottom of the address map in order to accommodate different micro-processor protect for boot code location. The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by WP# and/or RP# (see **Section 4.9** for details). Block erase or word write for boot block must not be carried out by WP# to low and RP# to V_{IH}.

The status register indicates when the WSM's block erase or word write operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase or word write. RY/BY#-High-impedance indicates that the WSM is ready for a new command, block erase is suspended (and word write is inactive), word write is suspended, or the device is in deep power-down mode.

The access time is 100 ns or 120 ns (t_{AVQV}) at the V_{CC} supply voltage range of 2.7 to 3.6 V over the temperature range, 0 to +70°C (LH28F160BG-TL)/ –25 to +85°C (LH28F160BGH-TL).

The Automatic Power Saving (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 3 mA at 2.7 V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

Top Boot

FFFFF FF000	4 k-Word Boot Block	0
FEFFF FE000	4 k-Word Boot Block	1
FDFFF FD000	4 k-Word Parameter Block	0
FCFFF FC000	4 k-Word Parameter Block	1
FBFFF FB000	4 k-Word Parameter Block	2
FAFFF FA000	4 k-Word Parameter Block	3
F9FFF F9000	4 k-Word Parameter Block	4
F8FFF F8000	4 k-Word Parameter Block	5
F7FFF F0000	32 k-Word Main Block	0
EFFFF E8000	32 k-Word Main Block	1
E7FFF E0000	32 k-Word Main Block	2
DFFFF D8000	32 k-Word Main Block	3
D7FFF D0000	32 k-Word Main Block	4
CFFFF C8000	32 k-Word Main Block	5
C7FFF C0000	32 k-Word Main Block	6
BFFFF B8000	32 k-Word Main Block	7
B7FFF B0000	32 k-Word Main Block	8
AFFFF A8000	32 k-Word Main Block	9
A7FFF A0000	32 k-Word Main Block	10
9FFFF 98000	32 k-Word Main Block	11
97FFF 90000	32 k-Word Main Block	12
8FFFF 88000	32 k-Word Main Block	13
87FFF 80000	32 k-Word Main Block	14
7FFFF 78000	32 k-Word Main Block	15
77FFF 70000	32 k-Word Main Block	16
6FFFF 68000	32 k-Word Main Block	17
67FFF 60000	32 k-Word Main Block	18
5FFFF 58000	32 k-Word Main Block	19
57FFF 50000	32 k-Word Main Block	20
4FFFF 48000	32 k-Word Main Block	21
47FFF 40000	32 k-Word Main Block	22
3FFFF 38000	32 k-Word Main Block	23
37FFF 30000	32 k-Word Main Block	24
2FFFF 28000	32 k-Word Main Block	25
27FFF 20000	32 k-Word Main Block	26
1FFFF 18000	32 k-Word Main Block	27
17FFF 10000	32 k-Word Main Block	28
0FFFF 08000	32 k-Word Main Block	29
07FFF 00000	32 k-Word Main Block	30

Bottom Boot

FFFFF F8000	32 k-Word Main Block	30
F7FFF F0000	32 k-Word Main Block	29
EFFFF E8000	32 k-Word Main Block	28
D7FFF D0000	32 k-Word Main Block	27
DFFFF D8000	32 k-Word Main Block	26
D7FFF D0000	32 k-Word Main Block	25
CFFFF C8000	32 k-Word Main Block	24
C7FFF C0000	32 k-Word Main Block	23
BFFFF B8000	32 k-Word Main Block	22
B7FFF B0000	32 k-Word Main Block	21
AFFFF A8000	32 k-Word Main Block	20
A7FFF A0000	32 k-Word Main Block	19
9FFFF 98000	32 k-Word Main Block	18
97FFF 90000	32 k-Word Main Block	17
8FFFF 88000	32 k-Word Main Block	16
87FFF 80000	32 k-Word Main Block	15
7FFFF 78000	32 k-Word Main Block	14
77FFF 70000	32 k-Word Main Block	13
6FFFF 68000	32 k-Word Main Block	12
67FFF 60000	32 k-Word Main Block	11
5FFFF 58000	32 k-Word Main Block	10
57FFF 50000	32 k-Word Main Block	9
4FFFF 48000	32 k-Word Main Block	8
47FFF 40000	32 k-Word Main Block	7
3FFFF 38000	32 k-Word Main Block	6
37FFF 30000	32 k-Word Main Block	5
2FFFF 28000	32 k-Word Main Block	4
27FFF 20000	32 k-Word Main Block	3
1FFFF 18000	32 k-Word Main Block	2
17FFF 10000	32 k-Word Main Block	1
0FFFF 08000	32 k-Word Main Block	0
07FFF 07000	4 k-Word Parameter Block	5
06FFF 06000	4 k-Word Parameter Block	4
05FFF 05000	4 k-Word Parameter Block	3
04FFF 04000	4 k-Word Parameter Block	2
03FFF 03000	4 k-Word Parameter Block	1
02FFF 02000	4 k-Word Parameter Block	0
01FFF 01000	4 k-Word Boot Block	1
00FFF 00000	4 k-Word Boot Block	0

NOTES :

BLOCK CONFIGURATION	VERSIONS
Top Boot	LH28F160BG-TTL
	LH28F160BGH-TTL
Bottom Boot	LH28F160BG-BTL
	LH28F160BGH-BTL

Fig. 1 Memory Map

2 PRINCIPLES OF OPERATION

The LH28F160BG-TL/BGH-TL Smart 3 flash memories include an on-chip WSM to manage block erase and word write functions. It allows for : fixed power supplies during block erasure and word write, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see **Table 1 "Bus Operations"**), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure and word writing. All functions associated with altering memory contents—block erase, word write, status and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word write. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase and word write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspended. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases or word writes are required) or hardwired to $V_{PPH1/2}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase or word write command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's blocks locking capability provides additional protection from inadvertent code or data alteration by gating erase and word write operations.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes or status register independent of the V_{PP} voltage. RP# can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component : CE#, OE#, WE#, RP# and WP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH} or V_{HH}. **Fig. 9** illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_{15}) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase or word write, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or word write modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase or word write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes

The read identifier codes operation outputs the manufacture code and device code (see **Fig. 2**). Using the manufacture and device codes, the system CPU can automatically match the device with its proper algorithms.

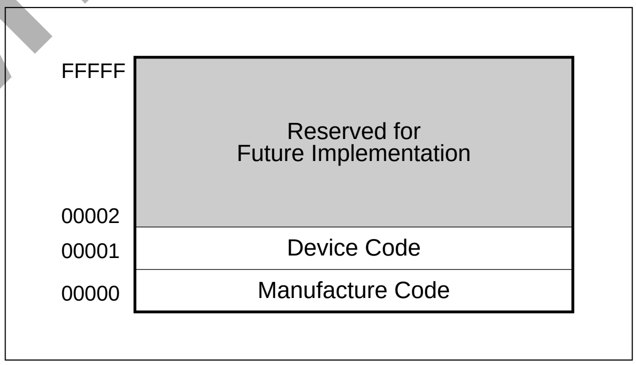


Fig. 2 Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. **Fig. 10** and **Fig. 11** illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

When the $V_{PP} \leq V_{PPLK}$, read operations from the status register, identifier codes, or blocks are enabled.

Device operations are selected by writing specific commands into the CUI. **Table 2** defines these commands.

Table 1 Bus Operations

MODE	NOTE	RP#	CE#	OE#	WE#	ADDRESS	V_{PP}	DQ_{0-15}	RY/BY#
Read	1, 2, 3, 8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes	8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See **Fig. 2**	X	(NOTE 5)	High Z
Write	3, 6, 7, 8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES :

1. Refer to **Section 6.2.3 "DC CHARACTERISTICS"**. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See **Section 6.2.3 "DC CHARACTERISTICS"** for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase or word write algorithm. It is high-impedance when the WSM is not busy, in block erase suspend mode (with word write inactive), word write suspend mode or deep power-down mode.
4. RP# at GND±0.2 V ensures the lowest deep power-down current.
5. See **Section 4.2** for read identifier code data.
6. V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.
7. Refer to **Table 2** for valid D_{IN} during a write operation.
8. Don't use the timing both OE# and WE# are V_{IL}.

Table 2 Command Definitions (NOTE 7)

COMMAND	BUS CYCLES REQ'D.	NOTE	FIRST BUS CYCLE			SECOND BUS CYCLE		
			Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)	Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥ 2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Word Write	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	5	Write	X	B0H			
Block Erase and Word Write Resume	1	5	Write	X	D0H			

NOTES :

1. Bus operations are defined in **Table 1**.
2. X = Any valid address within the device.
   IA = Identifier code address : see **Fig. 2**.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See **Table 5** for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacture and device codes. See **Section 4.2** for read identifier code data.
5. If the block is boot block, WP# must be at V_{IH} or RP# must be at V_{HH} to enable block erase or word write operations. Attempts to issue a block erase or word write to a boot block while WP# is V_{IH} or RP# is V_{IH}.
6. Either 40H or 10H is recognized by the WSM as the word write setup.
7. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or word write, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in **Fig. 2** retrieve the manufacture and device codes (see **Table 3** for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read :

Table 3 Identifier Codes

CODE	ADDRESS	DATA
Manufacture Code	00B0H	00000H
Device Code (Top Boot)	0068H	00001H
Device Code (Bottom Boot)	0069H	00001H

4.3 Read Status Register Command

The status register may be read to determine when a block erase or word write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see **Table 5**). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. RP# can be V_{IH} or V_{HH}. This command is not functional during block erase or word write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see **Fig. 3**). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions.

The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when V_{CC} = V_{CC1} and V_{PP} = $V_{PPH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that the corresponding if set, that WP# = V_{IH} or RP# = V_{HH}. If block erase is attempted to boot block when the corresponding WP# = V_{IL} or RP# = V_{IH}, SR.1 and SR.5 will be set to "1". Block erase operations with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

4.6 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see **Fig. 4**). The CPU can detect the completion of the word write event by analyzing the RY/BY# pin or status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when V_{CC} = V_{CC1} and V_{PP} = $V_{PPH1/2}$. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word write for boot blocks requires that the corresponding if set, that WP# = V_{IH} or RP# = V_{HH}. If word write is attempted to boot block when the corresponding WP# = V_{IL} or RP# = V_{IH}, SR.1 and SR.4 will be set to "1". Word write operations with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block erase interruption to read or word write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word Write Suspend command (see **Section 4.8**), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see **Fig. 5**). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for block erase). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word write operations initiated during block erase suspend have completed.

4.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). RY/BY# will also transition to high-impedance. Specification t_{WHRH1} defines the word write suspend latency.

At this point, a Read Array command can be written to read data from location other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continues the word write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Word Write Resume command is written, the device automatically outputs status register data when read (see **Fig. 6**). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for word write) while in word write suspend mode. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for word write). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word write).

4.9 Block Locking

This Boot Block flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

4.9.1 V_{PP} = V_{IL} FOR COMPLETE PROTECTION

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device.

4.9.2 WP# = V_{IL} FOR BLOCK LOCKING

The lockable blocks are locked when WP# = V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. Unlocked blocks can be programmed or erased normally (Unless V_{PP} is below V_{PPLK}).

4.9.3 BLOCK UNLOCKING

WP# = V_{IH} or RP# =V_{HH} unlocks all lockable blocks.

These blocks can now be programmed or erased.

WP# or RP# controls all block locking and V_{PP} provides protection against spurious writes. **Table 4** defines the write protection methods.

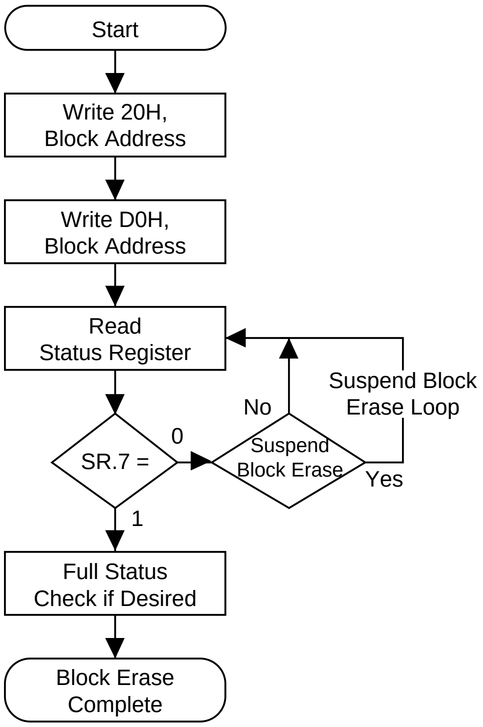
Table 4 Write Protection Alternatives

OPERATION	V_{PP}	RP#	WP#	EFFECT
Block Erase or Word Write	V_{IL}	X	X	All Blocks Locked.
	> V_{PPLK}	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{IH}	V_{IL}	2 Boot Blocks Locked.
			V_{IH}	All Blocks Unlocked.

Table 5 Status Register Definition

WSMS	ESS	ES	WWS	VPPS	WWSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES :
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/BY# or SR.7 to determine block erase or word write completion. SR.6-0 are invalid while SR.7 = "0".
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erase 0 = Successful Block Erase	If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.
SR.4 = WORD WRITE STATUS (WWS) 1 = Error in Word Write 0 = Successful Word Write	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase or Word Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2}$.
SR.2 = WORD WRITE SUSPEND STATUS (WWSS) 1 = Word Write Suspended 0 = Word Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = WP# or RP# Lock Detected, Operation Abort 0 = Unlock	The WSM interrogates the WP# and RP# only after Block Erase or Word Write command sequences. It informs the system, depending on the attempted operation, if the WP# is not V_{IH}, RP# is not V_{HH}.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.



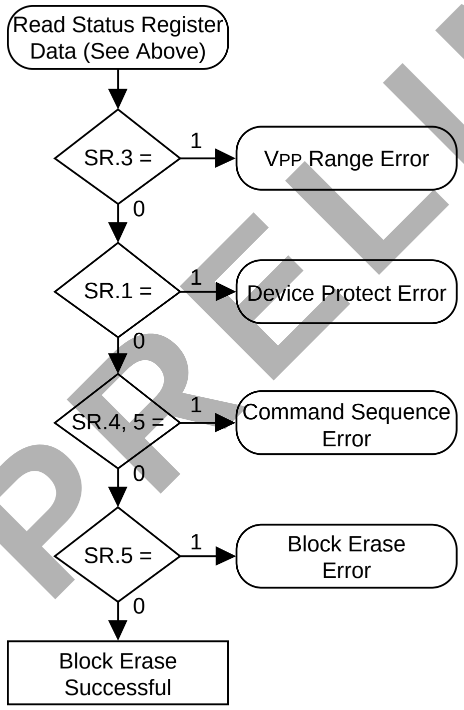
BUS OPERATION	COMMAND	COMMENTS
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last block erase operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

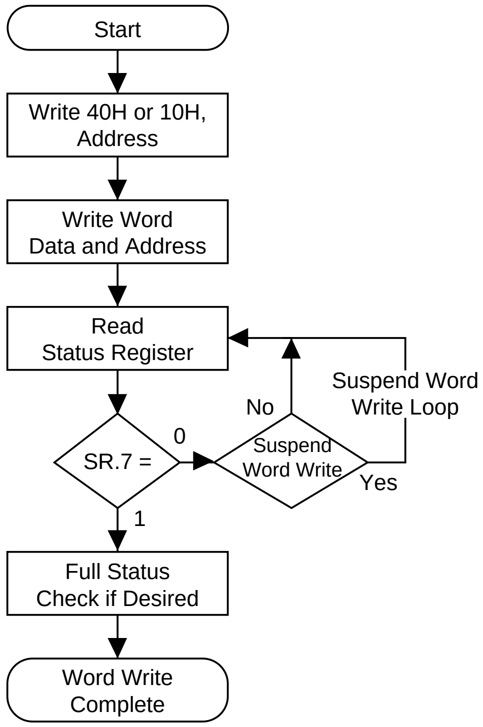


BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

Fig. 3 Automated Block Erase Flowchart



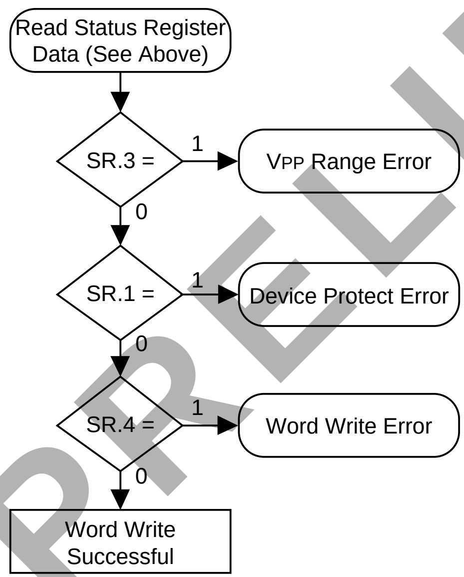
BUS OPERATION	COMMAND	COMMENTS
Write	Setup Word Write	Data = 40H or 10H Addr = Location to be Written
Write	Word Write	Data = Data to be Written Addr = Location to be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent word writes.

SR full status check can be done after each word write or after a sequence of word writes.

Write FFH after the last word write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

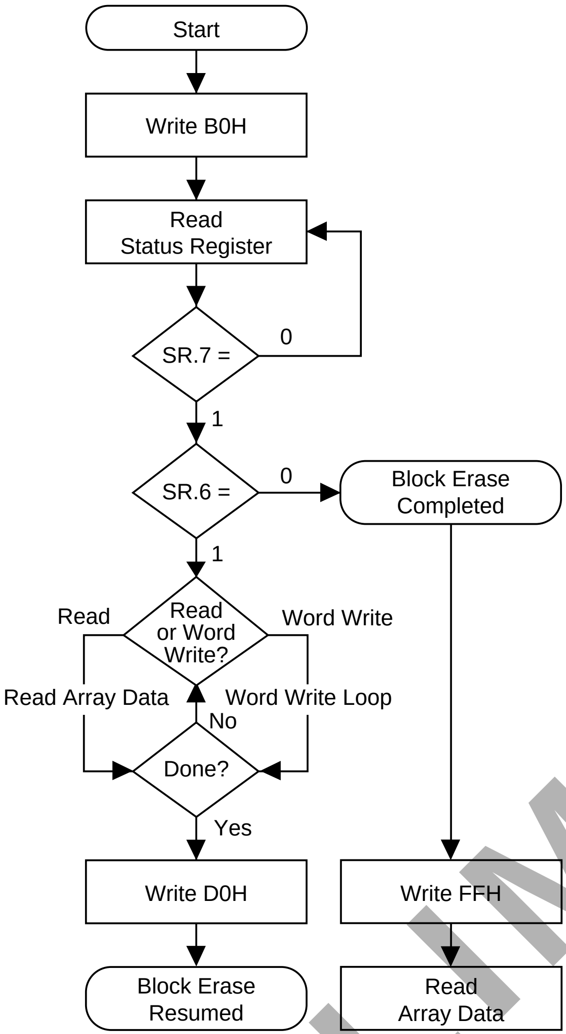


BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4 1 = Data Write Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.

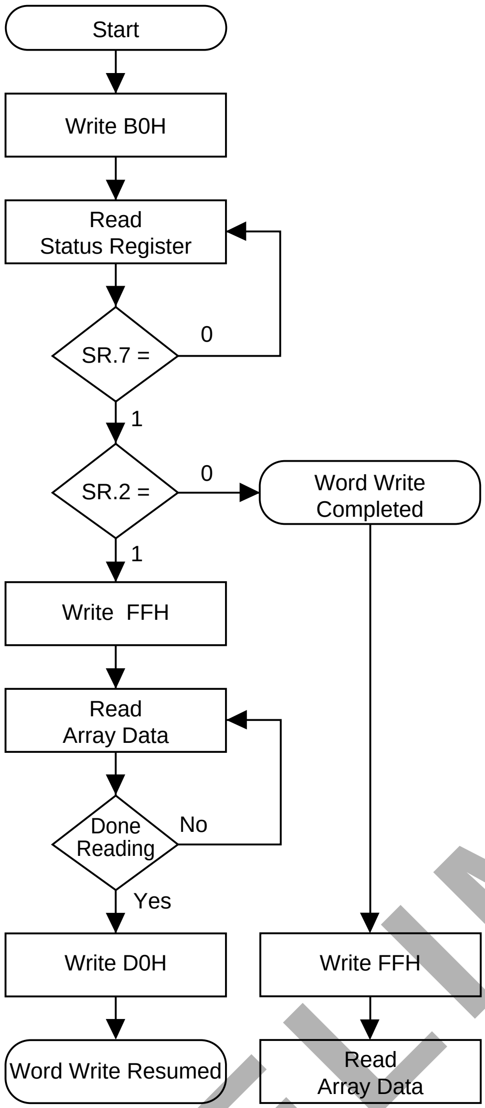
If error is detected, clear the status register before attempting retry or other error recovery.

Fig. 4 Automated Word Write Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

Fig. 5 Block Erase Suspend/Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Word Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Word Write Suspended 0 = Word Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations other than that being written.
Write	Word Write Resume	Data = D0H Addr = X

Fig. 6 Word Write Suspend/Resume Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for :

a. Lowest possible memory power consumption.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY#, Block Erase and Word Write Polling

RY/BY# is a output that provides a hardware method of detecting block erase and word write completion. It transitions low after block erase or word write commands and returns to high-impedance when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also high-impedance when the device is in block erase suspend (with word write inactive), word write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designers pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for word writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase and word write are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2}$ range, V_{CC} falls outside of a valid V_{CC1} range, or RP# $\neq$ V_{IH} or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase or word write, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP#

transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase or word write, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure or word writing during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

WP# provides additional protection from inadvertent code or data alteration. The device is disabled while RP# = V_{IL} regardless of its control inputs state.

5.7 Power Consumption

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See **Section 6.2.4 through 6.2.6 "AC CHARACTERISTICS - READ-ONLY and WRITE OPERATIONS"** and **Fig. 9**, **Fig. 10** and **Fig. 11** for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Operating Temperature

- LH28F160BG-TL
  - During Read, Block Erase and Word Write ········ 0 to +70°C (NOTE 1)
  - Temperature under Bias ········ –10 to +80°C
- LH28F160BGH-TL
  - During Read, Block Erase and Word Write ········ –25 to +85°C (NOTE 2)
  - Temperature under Bias ········ –25 to +85°C

Storage Temperature ········ –65 to +125°C

Voltage On Any Pin (except V_{CC}, V_{PP}, and RP#) ·· –0.5 V to V_{CC}+0.5 V (NOTE 3)

V_{CC} Supply Voltage ········ –0.2 to +3.9 V (NOTE 3)

V_{PP} Update Voltage during Block Erase and Word Write ········ –0.2 to +14.0 V (NOTE 3, 4)

RP# Voltage ········ –0.5 to +14.0 V (NOTE 3, 4)

Output Short Circuit Current ········ 100 mA (NOTE 5)

NOTICE : The specifications are subject to change without notice. Verify with your local SHARP sales office that you have the latest datasheet before finalizing a design.

**WARNING* : *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES :

1. Operating temperature is for commercial product defined by this specification.
2. Operating temperature is for extended temperature product defined by this specification.
3. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5 V which, during transitions, may overshoot to V_{CC}+2.0 V for periods < 20 ns.
4. Maximum DC voltage on V_{PP} and RP# may overshoot to +14.0 V for periods < 20 ns.
5. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

SYMBOL	PARAMETER	NOTE	MIN.	MAX.	UNIT	VERSIONS
T_A	Operating Temperature	1	0	+70	˚C	LH28F160BG-TL
			–25	+85	˚C	LH28F160BGH-TL
V_{CC1}	V_{CC} Supply Voltage		2.7	3.6	V	

NOTE :

1. Test condition : Ambient temperature

6.2.1 CAPACITANCE (NOTE 1)

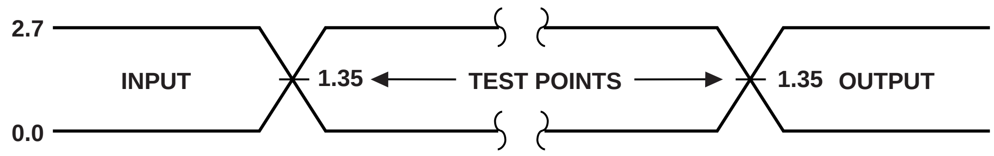
T_A = +25˚C, f = 1 MHz

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITION
C_{IN}	Input Capacitance	7	10	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT} = 0.0 V

NOTE :

1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS



AC test inputs are driven at 2.7 V for a logic "1" and 0.0 V for a Logic "0". Input timing begins, and output timing ends, at 1.35 V. Input rise and fall times (10% to 90%) < 10 ns.

Fig. 7 Transient Input/Output Reference Waveform for V_{CC} = 2.7 to 3.6 V

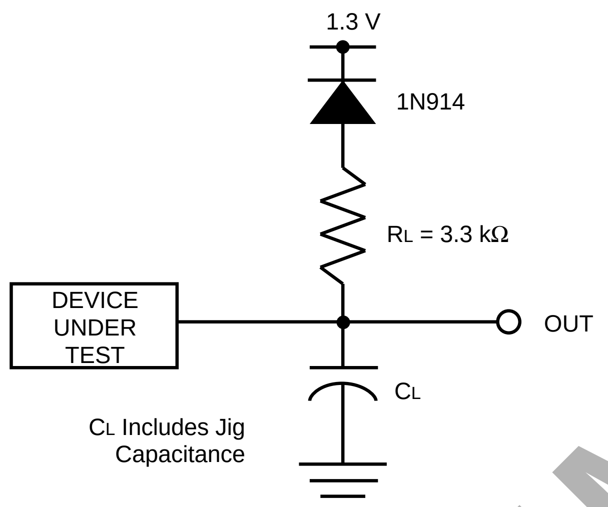


Fig. 8 Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	C_L (pF)
V_{CC} = 2.7 to 3.6 V	50

6.2.3 DC CHARACTERISTICS

SYMBOL	PARAMETER	NOTE	V_{CC} = 2.7 to 3.6 V		UNIT	TEST CONDITIONS
			TYP.	MAX.		
I_{LI}	Input Load Current	1		±1	µA	V_{CC} = V_{CC} Max. V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1		±10	µA	V_{CC} = V_{CC} Max. V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1, 3, 6	25	50	µA	CMOS Inputs V_{CC} = V_{CC} Max. CE# = RP# = V_{CC}±0.2 V
			0.2	2	mA	TTL Inputs V_{CC} = V_{CC} Max. CE# = RP# = V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1	5	10	µA	RP# = GND±0.2 V I_{OUT} (RY/BY#) = 0 mA
I_{CCR}	V_{CC} Read Current	1, 5, 6		25	mA	CMOS Inputs V_{CC} = V_{CC} Max. CE# = GND f = 5 MHz I_{OUT} = 0 mA
				30	mA	TTL Inputs V_{CC} = V_{CC} Max. CE# = GND f = 5 MHz I_{OUT} = 0 mA
I_{CCW}	V_{CC} Word Write Current	1, 7		17	mA	V_{PP} = 2.7 to 3.6 V
				12	mA	V_{PP} = 12.0±0.6 V
I_{CCE}	V_{CC} Block Erase Current	1, 7		17	mA	V_{PP} = 2.7 to 3.6 V
				12	mA	V_{PP} = 12.0±0.6 V
I_{CCWS} I_{CCES}	V_{CC} Word Write or Block Erase Suspend Current	1, 2		6	mA	CE# = V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	1	±2	±15	µA	$V_{PP} \leq V_{CC}$
			10	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	µA	RP# = GND±0.2 V, $V_{PP} \leq V_{CC}$
			14	150	µA	RP# = GND±0.2 V, $V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Word Write Current	1, 7	12	40	mA	V_{PP} = 2.7 to 3.6 V
				30	mA	V_{PP} = 12.0±0.6 V
I_{PPE}	V_{PP} Block Erase Current	1, 7	11	35	mA	V_{PP} = 2.7 to 3.6 V
				20	mA	V_{PP} = 12.0±0.6 V
I_{PPWS} I_{PPES}	V_{PP} Word Write or Block Erase Suspend Current	1	10	200	µA	V_{PP} = $V_{PPH1/2}$

6.2.3 DC CHARACTERISTICS (contd.)

SYMBOL	PARAMETER	NOTE	V_{CC} = 2.7 to 3.6 V		UNIT	TEST CONDITIONS
			MIN.	MAX.		
V_{IL}	Input Low Voltage	7	–0.5	0.8	V	
V_{IH}	Input High Voltage	7	$0.7V_{CC}$	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage	3, 7		0.4	V	V_{CC} = V_{CC} Min. I_{OL} = 2.0 mA
V_{OH1}	Output High Voltage (TTL)	3, 7	$0.85V_{CC}$		V	V_{CC} = V_{CC} Min. I_{OH} = –2.0 mA
V_{OH2}	Output High Voltage (CMOS)	3, 7	0.5		V	V_{CC} = V_{CC} Min. I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lockout Voltage during Normal Operations	4, 7		1.5	V	
V_{PPH1}	V_{PP} Voltage during Word Write or Block Erase Operations		2.7	3.6	V	
V_{PPH2}	V_{PP} Voltage during Word Write or Block Erase Operations		11.4	12.6	V	
V_{LKO}	V_{CC} Lockout Voltage		1.3		V	
V_{HH}	RP# Unlock Voltage	8, 9	11.4	12.6	V	Block Erase and Word Write for Boot Blocks

NOTES :

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.0 V, V_{PP} = 3.0 V and T_A = +25˚C. These currents are valid for all product versions (packages and speeds).
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If reading or word writing in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/BY#.
4. Block erases and word writes are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (max.) and V_{PPH1} (min.), between V_{PPH1} (max.) and V_{PPH2} (min.), and above V_{PPH2} (max.).
5. Automatic Power Saving (APS) reduces typical I_{CCR} to 3 mA at 2.7 V V_{CC} in static operation.
6. CMOS inputs are either V_{CC}±0.2 V or GND±0.2 V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Boot block erases and word writes are inhibited when the corresponding RP# = V_{IH} or WP# = V_{IL}. Block erase and word write operations are not guaranteed with V_{IH} < RP# < V_{HH} and should not be attempted.
9. RP# connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS (NOTE 1)

• V_{CC} = 2.7 to 3.6 V, T_A = 0 to +70˚C or −25 to +85˚C

VERSIONS			LH28F160BG-TL10 LH28F160BGH-TL10		LH28F160BG-TL12 LH28F160BGH-TL12		UNIT
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
t_{AVAV}	Read Cycle Time		100		120		ns
t_{AVQV}	Address to Output Delay			100		120	ns
t_{ELQV}	CE# to Output Delay	2		100		120	ns
t_{PHQV}	RP# High to Output Delay		10		10		µs
t_{GLQV}	OE# to Output Delay	2		45		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		45		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20		25	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns

NOTES :

1. See AC Input/Output Reference Waveform (**Fig. 7**) for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

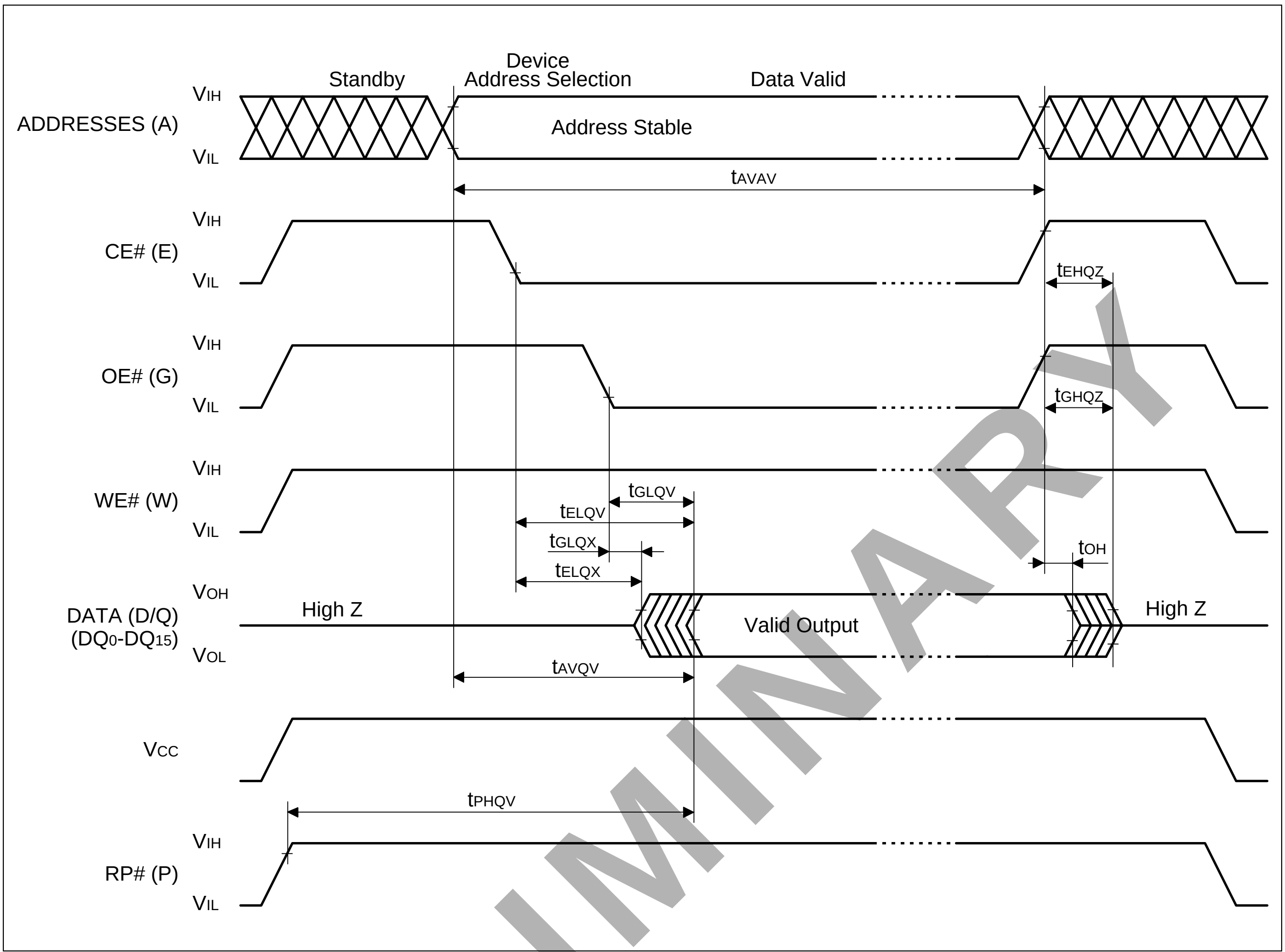


Fig. 9 AC Waveform for Read Operations

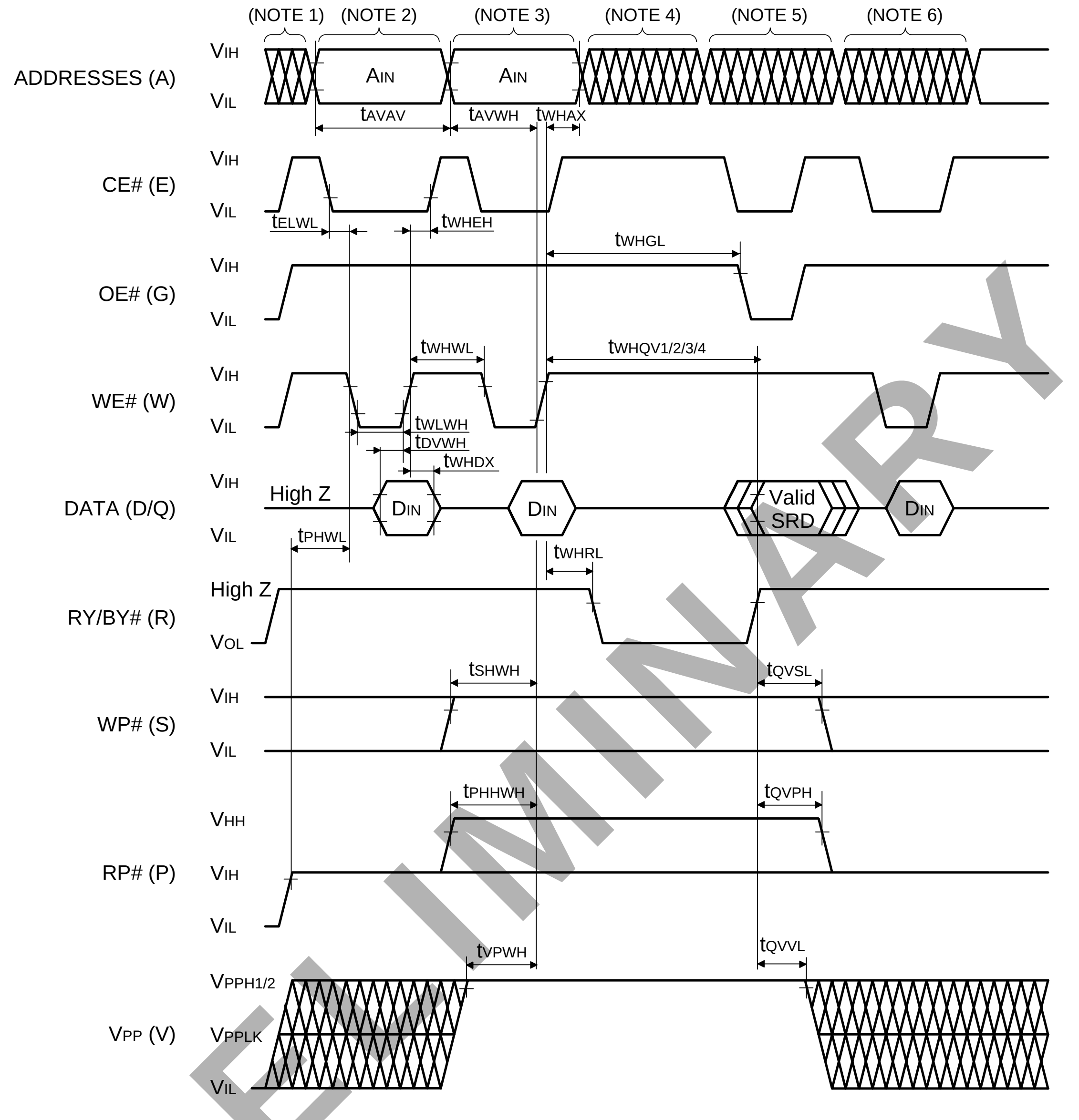
6.2.5 AC CHARACTERISTICS FOR WE#-CONTROLLED WRITE OPERATIONS (NOTE 1)

• V_{CC} = 2.7 to 3.6 V, T_A = 0 to +70˚C or −25 to +85˚C

VERSIONS			LH28F160BG-TL10 LH28F160BGH-TL10		LH28F160BG-TL12 LH28F160BGH-TL12		UNIT
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
t_{AVAV}	Write Cycle Time		100		120		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	10		10		µs
t_{ELWL}	CE# Setup to WE# Going Low		0		0		ns
t_{WLWH}	WE# Pulse Width		50		50		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		100		ns
t_{SHWH}	WP# V_{IH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		50		ns
t_{WHDX}	Data Hold from WE# High		0		0		ns
t_{WHAX}	Address Hold from WE# High		0		0		ns
t_{WHEH}	CE# Hold from WE# High		0		0		ns
t_{WHWL}	WE# Pulse Width High		30		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			100		100	ns
t_{WHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns

NOTES :

1. Read timing characteristics during block erase and word write operations are the same as during read-only operations. Refer to **Section 6.2.4 "AC CHARACTERISTICS"** for read-only operations.
2. Sampled, not 100% tested.
3. Refer to **Table 2** for valid A_{IN} and D_{IN} for block erase or word write.
4. V_{PP} should be held at $V_{PPH1/2}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase or word write success (SR.1/3/4/5 = 0 : on Boot Blocks, SR.3/4/5 = 0 : on Parameter Blocks and Main Blocks).



NOTES :

1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Fig. 10 AC Waveform for WE#-Controlled Write Operations

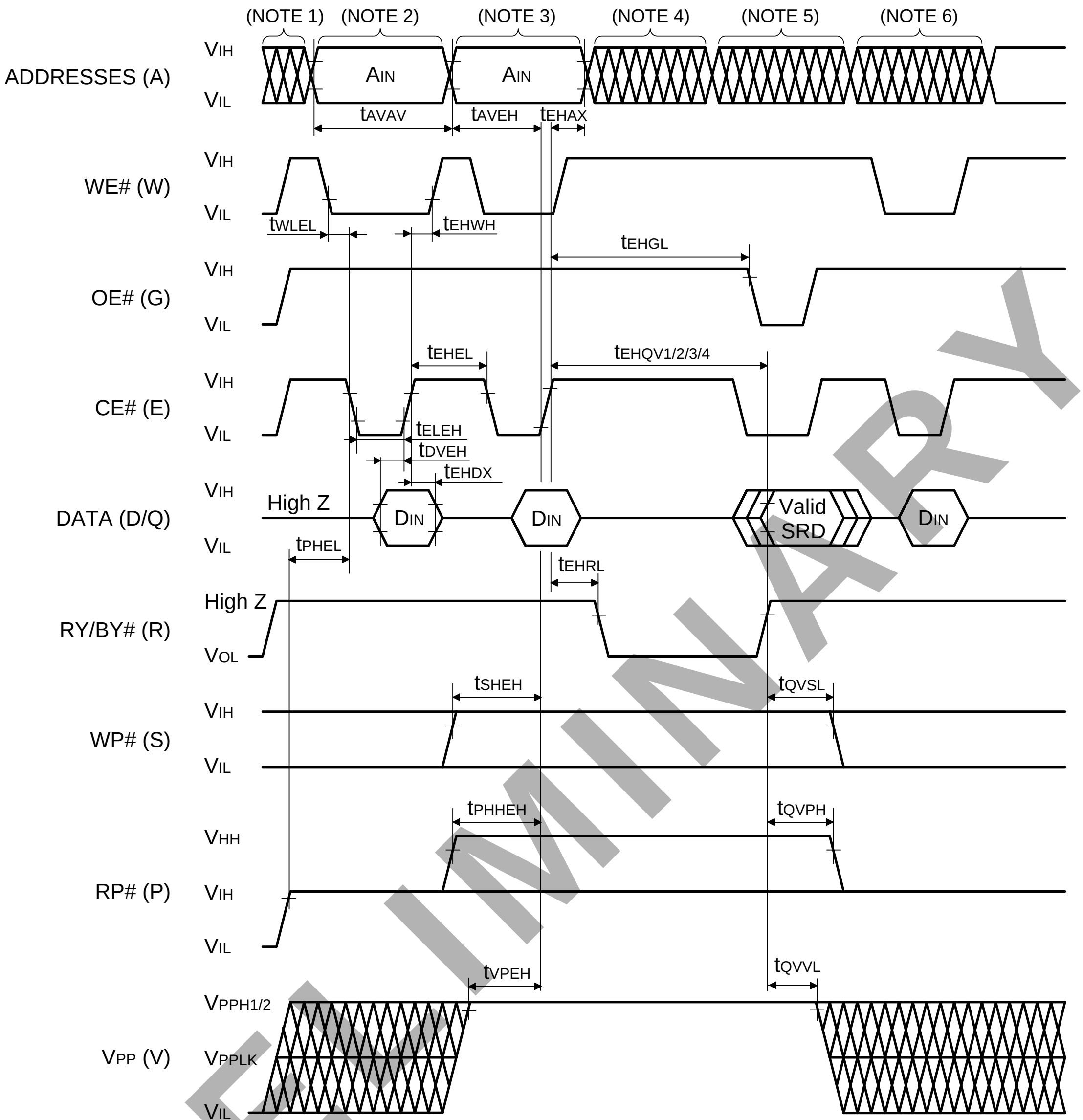
6.2.6 AC CHARACTERISTICS FOR CE#-CONTROLLED WRITE OPERATIONS (NOTE 1)

• V_{CC} = 2.7 to 3.6 V, T_A = 0 to +70˚C or −25 to +85˚C

VERSIONS			LH28F160BG-TL10 LH28F160BGH-TL10		LH28F160BG-TL12 LH28F160BGH-TL12		UNIT
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
t_{AVAV}	Write Cycle Time		100		120		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	10		10		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{ELEH}	CE# Pulse Width		70		70		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		100		ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		50		ns
t_{EHDX}	Data Hold from CE# High		0		0		ns
t_{EHAX}	Address Hold from CE# High		0		0		ns
t_{EHWH}	WE# Hold from CE# High		0		0		ns
t_{EHEL}	CE# Pulse Width High		25		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			100		100	ns
t_{EHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns

NOTES :

1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to **Table 2** for valid A_{IN} and D_{IN} for block erase or word write.
4. V_{PP} should be held at $V_{PPH1/2}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase or word write success (SR.1/3/4/5 = 0 : on Boot Blocks, SR.3/4/5 = 0 : on Parameter Blocks and Main Blocks).



NOTES :

1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Fig. 11 AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS

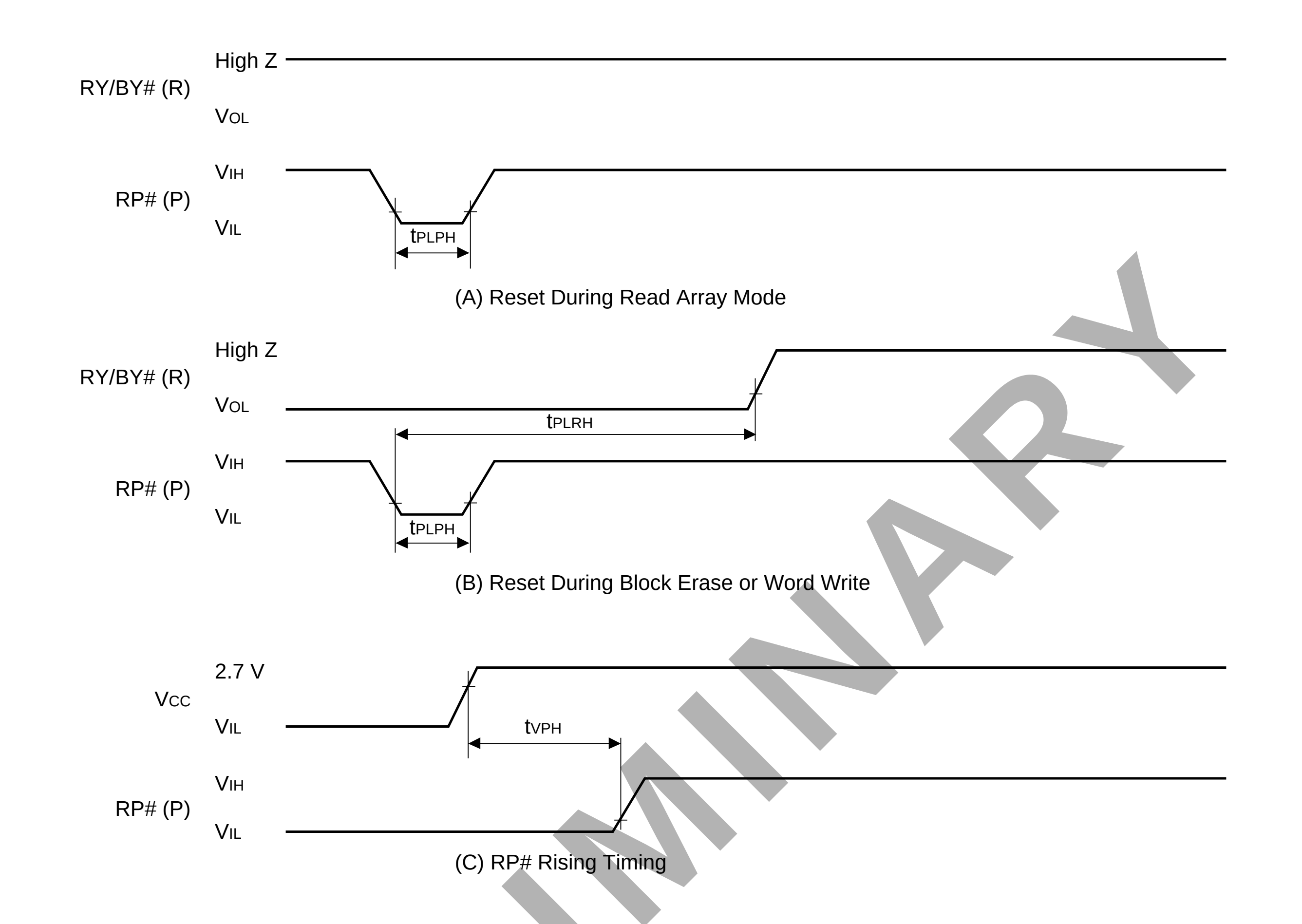


Fig. 12 AC Waveform for Reset Operation

Reset AC Specifications (NOTE 1)

SYMBOL	PARAMETER	NOTE	V_{CC} = 2.7 to 3.6 V		UNIT
			MIN.	MAX.	
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		ns
t_{PLRH}	RP# Low to Reset during Block Erase or Word Write	2, 3		22	µs
t_{VPH}	V_{CC} 2.7 V to RP# High	4	100		ns

NOTES :

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase or word write operation is not executing, the reset will complete within 100 ns.
3. A reset time, t_{PHQV}, is required from the latter of RY/BY# or RP# going high until outputs are valid.
4. When the device power-up, holding RP#-low minimum 100 ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE AND WORD WRITE PERFORMANCE (NOTE 3, 4)

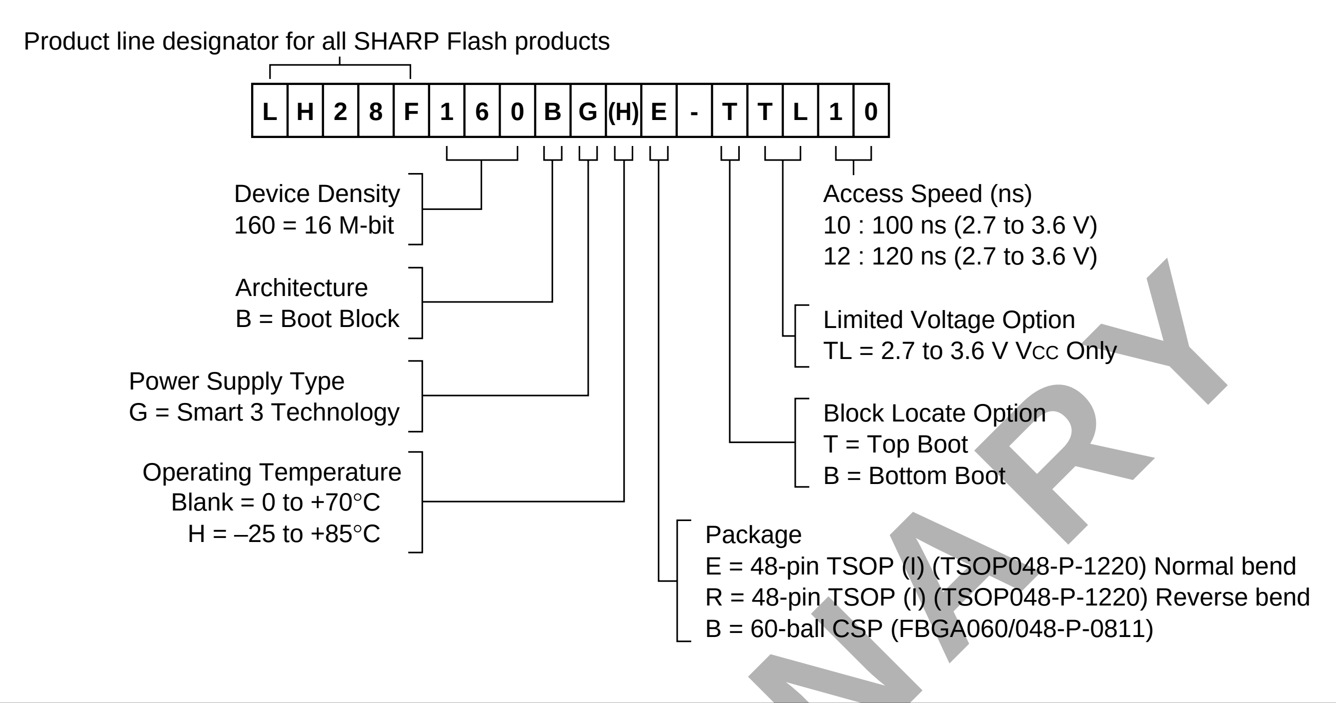
• V_{CC} = 2.7 to 3.6 V, T_A = 0 to +70°C or −25 to +85°C

SYMBOL	PARAMETER		NOTE	V_{PP} = 2.7 to 3.6 V			V_{PP} = 12.0±0.6 V			UNIT
				MIN.	TYP.(NOTE 1)	MAX.	MIN.	TYP.(NOTE 1)	MAX.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32 k-Word Block	2		55			15		µs
		4 k-Word Block	2		60			30		µs
	Block Write Time	32 k-Word Block	2		1.8			0.6		s
		4 k-Word Block	2		0.3			0.2		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32 k-Word Block	2		1.2			0.7		s
		4 k-Word Block	2		0.5			0.5		s
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read				7.5	8.6		6.5	7.5	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read				19.3	23.6		11.8	15	µs

NOTES :

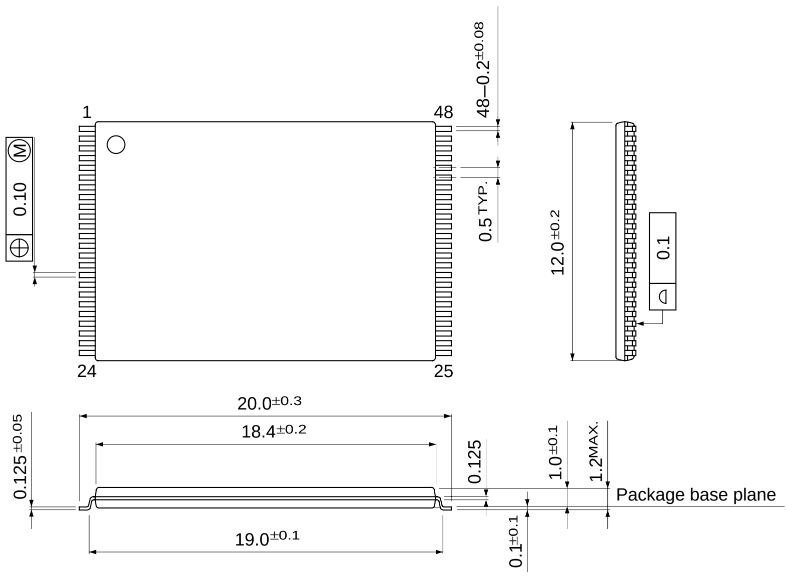
1. Typical values measured at T_A = +25°C and V_{CC} = 3.0 V, V_{PP} = 3.0 V/V_{CC} = 3.0 V, V_{PP} = 12.0 V. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, not 100% tested.

7 ORDERING INFORMATION



OPTION	ORDER CODE	VALID OPERATIONAL COMBINATIONS V_{CC} = 2.7 to 3.6 V 50 pF load, 1.35 V I/O Levels
1	LH28F160BGXX-XTL10	100 ns
2	LH28F160BGXX-XTL12	120 ns

48 TSOP (TSOP048-P-1220)



60 CSP (FBGA060/048-P-0811)