## SM5K4

#### **DESCRIPTION**

The SM5K4 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, ROM, RAM, 10-bit A/D converter and timer/counters.

It provides three kinds of interrupts and 4 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package: best suitable for Low power controlling, compact equipment like a precision charger.

#### **FEATURES**

ROM capacity: 2 048 x 4 bits
RAM capacity: 128 x 4 bits

• Instruction sets: 50

• Subroutine nesting : 4 levels

• I/O port :

Input

8 (30SDIP/32SOP/36QFP)

5 (24SSOP)

Output

4

Input/output

out 12 (36QFP/32SOP)

11 (30SDIP) 8 (24SSOP)

Interrupts:

Internal interrupt

x 1 (timer)

External interrupt

x 2 (2 external interrupt

inputs)

• A/D converter :

Resolution

10 bits

Channels

4

Conversion cycle

 $122 \mu s (fosc = 500kHz)$ 

Comparator mode cycle 50 µs (fosc = 500kHz)

Timer/counter: 8 bits x 1

Built-in main clock oscillator (CR oscillator :

Capacitor is built-in) for system clock

Oscillator frequency: 2.0 MHz (MAX.)

· Built-in 15 stages divider

• Instruction cycle time :

1.2  $\mu$ s (TYP.) (V<sub>DD</sub> = 5 V, Rf = 33 k $\Omega$ )

# 4-Bit Single-Chip Microcomputer (Controller with 10-Bit A/D Converter)

- Large current output pins (LED direct drive): 4
- Supply voltage: 2.7 to 5.5 V
- · Packages :

30-pin SDIP (SDIP030-P-0400)

32-pin SOP (SOP032-P-0525)

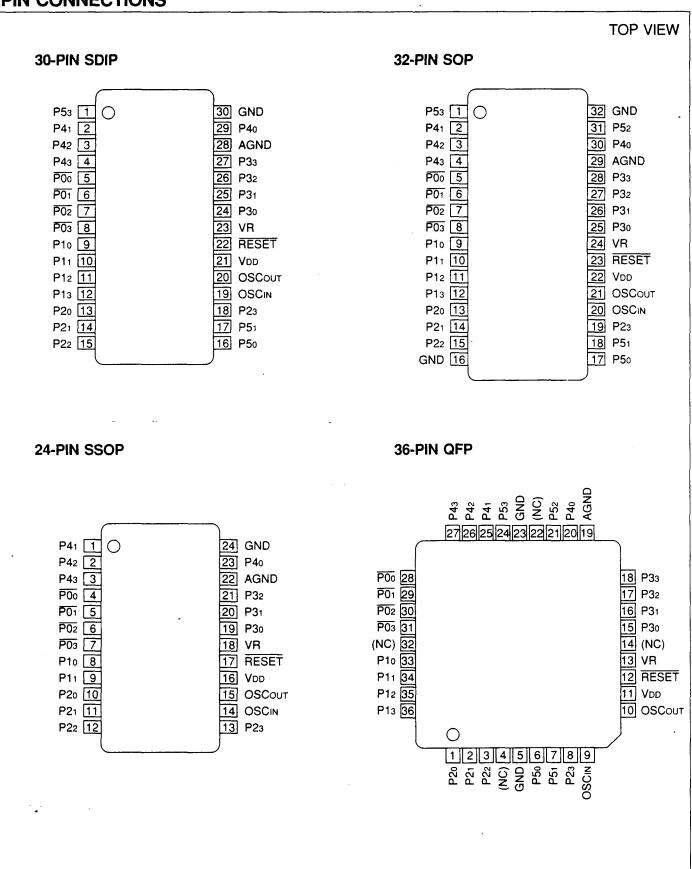
24-pin SSOP (SSOP024-P-0275)

36-pin QFP (QFP036-P-1010)

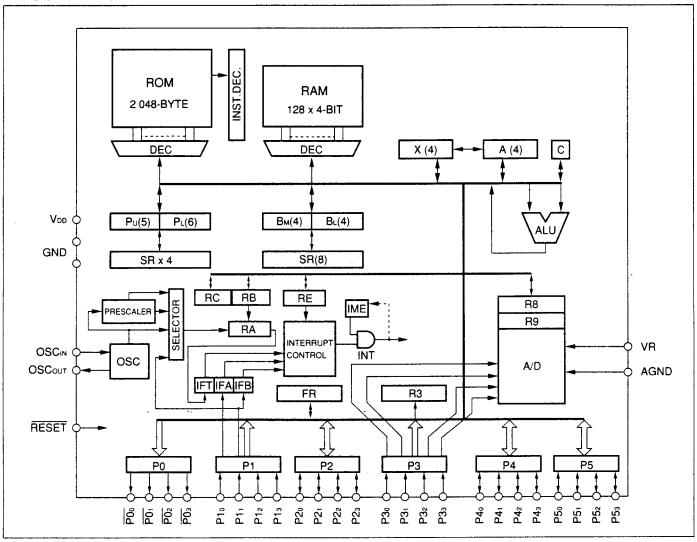
#### NOTE:

Refer to the SM5K5 concerning about system/functional information of SM5K4.

#### PIN CONNECTIONS



## **BLOCK DIAGRAM**



#### Nomenclature

	4.0		
Α	: A register	INT	: Interrupt control unit
A/D	: A/D converter unit	P0-P5	: Port register
ALU	: Arithmetic logic unit	Pu, Pi	: Program counter
Вм, Вь	: RAM address register	R8, R9, RC, RE, RF	: Mode register
С	: Carry flag	RA	: Count register
IFA, IFB, IFT	: Interrupt request flag	RB	: Modulo register
IME	: Interrupt Master enable flag	SB	: SB register
INST. DEC.	: Instruction decoder	SR	: Stack register

## PIN DESCRIPTION

SYMBOL	1/0	FUNCTION
P0 <sub>0</sub> -P0 <sub>3</sub>	0	High current output (sink current 15 mA)
P1 <sub>0</sub> -P1 <sub>1</sub>		Input (standby release) (counter input : P1 <sub>1</sub> ) with pull-up resistor
P1 <sub>2</sub> -P1 <sub>3</sub>	I	Input (standby release) with pull-up resistor
P2 <sub>0</sub> -P2 <sub>3</sub>	1/0	Input or output (independent) with pull-up resistor
P3 <sub>0</sub> -P3 <sub>3</sub>	1	Input (also used as analog input) with pull-up resistor
P4 <sub>0</sub> -P4 <sub>3</sub> , P5 <sub>0</sub> -P5 <sub>3</sub>	I/O	Input and output with pull-up resistor
OSCIN, OSCOUT	I/O	Crystal pins
RESET	l	Reset signal input with pull-up resistor
VR, AGND	I	A/D converter reference supply input port
V <sub>DD</sub> , GND	1	Power supply, Ground

#### NOTE:

Pin numbers apply to the 36-pin QFP and 32-pin SOP. (In case of 30-pin SDIP, P5<sub>2</sub> pin does not exist. In case of 24-pin SSOP, P1<sub>2</sub>, P1<sub>3</sub> P3<sub>3</sub>, P5<sub>0</sub>-P5<sub>3</sub> pins do not exist.)

### **ABSOLUTE MAXIMUM RATINGS**

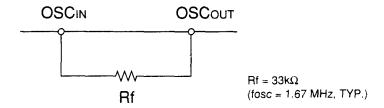
PARAMETER SYMBOL CONDITIONS		RATING	UNIT	
Supply voltage	V <sub>DD</sub>		-0.3 to +7.0	V
Input voltage	Vı		-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	Vo	_	-0.3 to V <sub>DD</sub> +0.3	V
	Юн	High-level output current (all outputs)	4	mA
Maximum output current	The state of the	mA		
	lo <sub>L1</sub>	Low-level output current (all but P00-P03)	4	mA
Tetal autout aurrant	Σюн	High-level output current (all outputs)	20	mA
Total output current	∑iol	Low-level output current (all outputs)	80	mA
Operating temperature	TOPR		-20 to +85	°C
Storage temperature	Тѕтс		-55 to +150	°C

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	Voo		2.7 to 5.5	V
In the estion avala	<b>T</b>	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	2 to 5	μs
Instruction cycle	Tsys	$V_{DD} = 5.0 \text{ V} \pm 10\%$	1 to 5	
Main clock frequency *		$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	1 M to 400 k	1.1-
(OSCIN - OSCOUT)	fosc	$V_{DD} = 5.0 \text{ V} \pm 10\%$	2 M to 400 k	Hz

<sup>\*</sup> Degree of fluctuation frequency: ± 20%

#### **OSCILLATION CIRCUIT**



#### NOTES:

- The typical oscillation frequency shall be determined in consideration of operating condition and fluctuation frequency.
- Mount Rf as close as possible to the oscillator pins of the LSI, in order to reduce an influence from floating capacitance.
- Since the value of resistor Rf varies depending on circuit pattern and others, the final Rf value shall be determined on the actual unit.
- Don't connect any line to OSC<sub>IN</sub> and OSC<sub>OUT</sub> except oscillator circuit.
- Don't put any signal line across the oscillator circuit line.
- -• On the multilayer circuit, do not let the oscillator circuit wiring cross other circuit.
- Minimize the wiring capacitance of GND and VDD wiring.

## DC CHARACTERISTICS

 $(V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{ Ta} = -20 \text{ to } +85^{\circ}\text{C})$ 

PARAMETER	SYMBOL	COND	ITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
	VIH1			0.8 x Vod		Voo	٧	1
Input voltage  Input current  Output current  Supply current  A/D conversion	VIL1			0		0.2 x VDD		'
	V <sub>IH2</sub>			0.9 x V <sub>DD</sub>		V <sub>DD</sub> 0.1 x V <sub>DD</sub>	V	2
	VIL2			0			·	
		V 0.V	$V_{DD} = 2.7 \text{ to } 3.3 \text{ V}$	1.0	25	90	μA	3
	lıLı	Vin = 0 V	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	15	70	250		
Input current	I <sub>IH1</sub>	VIN = VDD				3.0		
	IIL2	VIN = 0 V	O.8 x Vob   O.2 x Vob   O.2 x Vob   O.9 x Vob   O.9 x Vob   O.1	^	4			
	I <sub>IH2</sub>	Vin = VDD			1.0	.10	μA	4
	<b>I</b>	V- 10 V	$V_{DD} = 2.7 \text{ to } 3.3 \text{ V}$	3	15			
Input voltage  Input current  Output current  A/D conversion  Reference clock	lo <sub>L1</sub>	Vo = 1.0 V	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	12	25		mA	5
	1	$V_0 = V_{DD} - 0.5 \text{ V}$	$V_{DD} = 2.7 \text{ to } 3.3 \text{ V}$	0.2	1.5	'''	111/4	
Output ourront	Юн1	VO = VDD - U.5 V	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	0.8	2.2			
Output current	lo <sub>L2</sub>	Vo = 1.5 V	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	4.0	9.0			
	lava	Vo = V <sub>DD</sub> - 0.5 V	$V_{DD} = 2.7 \text{ to } 3.3 \text{ V}$	0.2	2.0		mA	6
	Юн2	VO = VDD - 0.5 V	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	0.8	2.4			
	Іонз	$V_{OH} = V_{DD} - 1.0 V$	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	0.5			mA	7
		fosc = 2.0 MHz	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$		1 200	2 800		
	IDD 	fosc = 1.0 MHz	$V_{DD} = 2.7 \text{ to } 3.3 \text{ V}$		300	900		
		105C = 1.0 W11Z	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	5 V 600	1 400	μA	8	
	Інст	fosc = 2.0 MHz	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$		760	1 700	μA	J
Supply current		fosc = 1.0 MHz	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$		400	1 000		
	Іѕтор	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$				5		
	lva	A/D conversion	$V_{DD} = 2.7 \text{ to } 3.3 \text{ V}$		130	350	μА	9
		in operation	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$		220	500		
		A/D conversion in stop	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$			3	μA	10
	Resolution				10		bit	
	Differential	fosc = 1.0 MHz	V <sub>DD</sub> = VR = 5.0 V		+ 25	± 4.0		
	error	TOPR = 25°C			± 2.5			
A/D conversion	Sequential	fosc = 1 MHz	Von - VR - 50 V		+32 -	+50	LSB	
	error	TOPR = 25°C	VDD = VT( = 5.0 V		2 0.2	2 0.0		
	Total error	fosc = 1 MHz Topr = 25°C	V <sub>DD</sub> = VR = 5.0 V		± 4.0	± 6.0		
Reference clock oscillator frequency	fosc	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V},$	1.34	1.67	2.0	MHz	-	

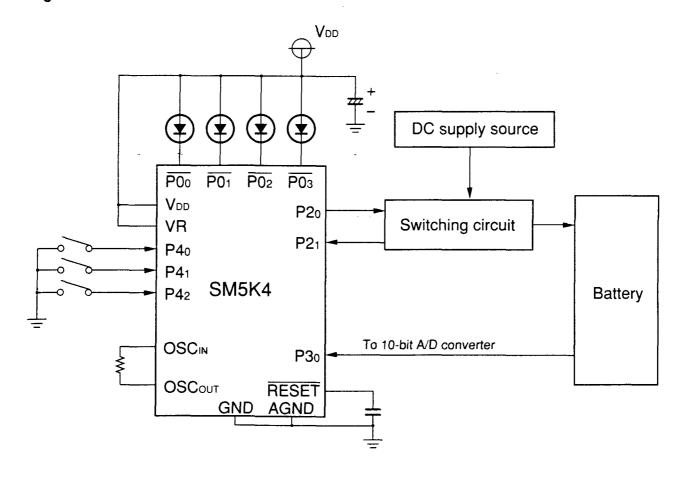
#### NOTES:

- 1. Applicable pins : P1<sub>2</sub>, P1<sub>3</sub>, P2<sub>0</sub>-P2<sub>3</sub>, P3<sub>0</sub>-P3<sub>3</sub> (digital input mode), P4<sub>0</sub>-P4<sub>3</sub>, P5<sub>0</sub>-P5<sub>3</sub>\*<sup>1</sup>
- 2. Applicable pins : OSCIN, RESET, P10, P11
- 3. Applicable pins: RESET, P1o-P13, P2o-P23, P4o-P43, P5o-P53, P3o-P33 (digital input mode)\*1
- 4. Applicable pins : P3₀-P3₃ (analog input mode)
   5. Applicable pins : P0₀-P0₃ (large current output)
- 6. Applicable pins : P2o-P23, P4o-P43, P5o-P53 (output mode)\*1
- 7. Applicable pins: P3<sub>0</sub>-P3<sub>3</sub>\*2

- 8. No-load condition (A/D conversion in stop)
- 9. A/D conversion in operation (A/D conversion enable)
- 10. A/D conversion in stop (A/D conversion disable)
- \*1 In case of 36-pin QFP and 32-pin SOP. (In case of 30-pin SDIP, P52 pin dose not exist. In case of 24-pin SSOP, P12, P13, P33, P50-P53 pins do not exist.)
- \*2 P3 ports are normally used for input port with pull-up resistor. These ports can be also used as a suspected case of output port.

#### SYSTEM CONFIGURATION EXAMPLE

#### Charger controller



Singlechip LH7xxxx '790 '789 '791 SMxxxx 'K series MCU Microcontroller MPU Microprocessor ARM Advanced RISC Machines Databank LCD Controller LCD Driver Controllers Processors Portable Low Power Low Voltage High Performance Power curve MIPS MIPS/Watt Execution Cycle Multiplier High Speed Compact Handheld System on Chip System Integration Chip Integration Integration Superchip Standard Cell Core Core based IC VHDL Verilog Synthesis Chip on Board COB Chip on Flex COF Device on Board DOB Power Supply Controller Handy Products Development Tools Board Support Software Tools Tools 2.10 Software Support Emulators Evaluation Boards ICE In-Circuit Emulators ROM ICE SME Series Programmable User Configurable RTOS Real Time Operating Systems Third Party Support Software Hardware Yokogawa Digital Cosmic Compiler C Language C Like Assembler Linker Debugger Debug A/D D/A DAC Analog Digital 10-bit 4-bit 8-bit 16-bit 32-bit Address bus Data Bus