SM5K6

4-Bit Single-Chip Microcomputer (Controller With 10-Bit A/D Converter)

DESCRIPTION

The SM5K6 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, serial interface function, ROM, RAM, 10-bit A/D converter and timer/counters. It provides five kinds of interrupts and 8 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package : best suitable for low power controlling, compact equipment like a precision charger.

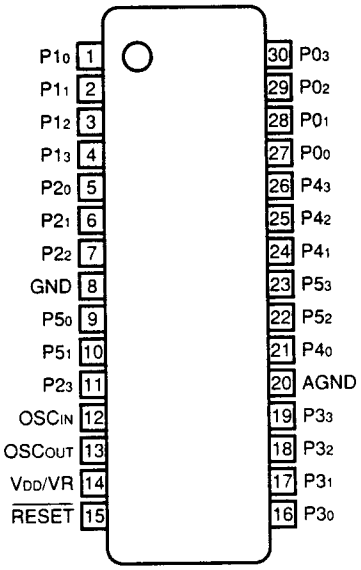
FEATURES

- ROM capacity : 4 096 x 8 bits
- RAM capacity : 256 x 4 bits
- Instruction sets : 52
- Subroutine nesting : 8 levels
- I/O port :
  - input 4
  - input/output 20
- Interrupts :
  - Internal interrupt x 3 (2 timers, 1 serial interface)
  - External interrupt x 2 (2 external interrupt inputs)
- A/D converter :
  - Resolution 10 bits
  - Inputs channels 8
- Timer/counter : 8 bits x 2
- Serial interface : 8 bits synchrounous x 1
- Watch dog timer : 8 bits x 1 (also used as timer 2)
- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider for real time clock
- Instruction cycle time :
  - 1 µs (4 MHz, at 5 V ± 10%)
  - 4 µs (4 MHz, at 2.0 to 5.5 V)
- Large current output pins (LED direct drive) : 8
- Buzzer output
- Supply voltage : 2.0 to 5.5 V
- Packages :
  - 30-pin SDIP (SDIP030-P-0400)
  - 32-pin SOP (SOP032-P-0525)
  - 36-pin QFP (QFP036-P-1010)

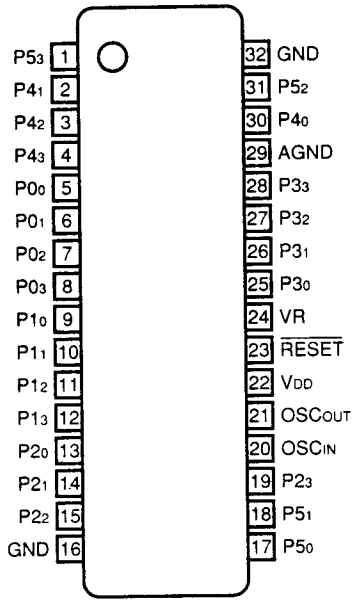
PIN CONNECTIONS

TOP VIEW

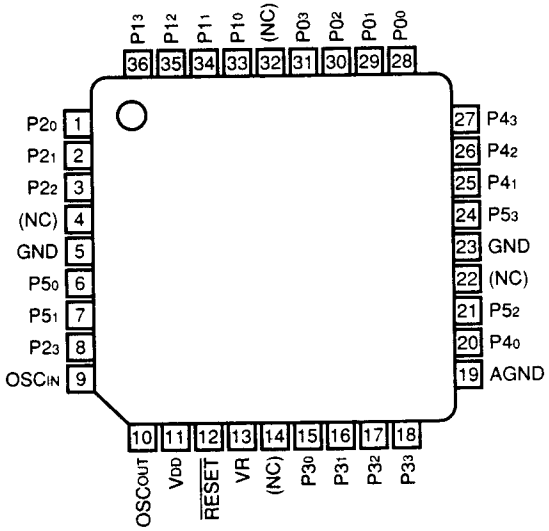
30-PIN SDIP



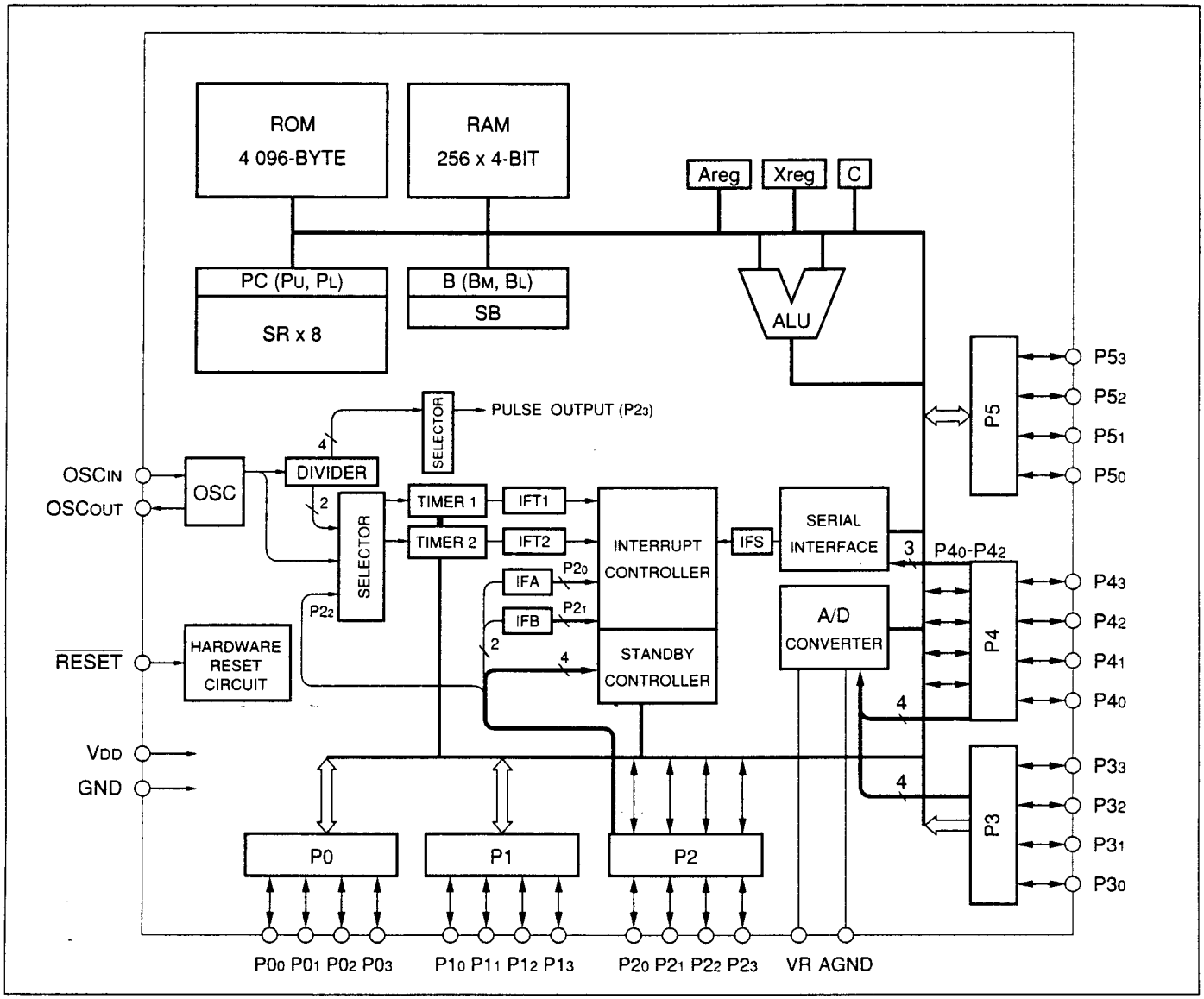
32-PIN SOP



36-PIN QFP



BLOCK DIAGRAM



Nomenclature

Areg	: A register (Accumulator)
ALU	: Arithmetic logic unit
B	: RAM address register
C	: Carry latch flag
IFA, IFB, IFS	: Interrupt request flag
IFT1, IFT2	
OSC	: System clock oscillator
P0, P1, P2	: I/O access
P3, P4, P5	
PC	: Program counter
RAM	: Data memory
ROM	: Program memory
SB	: SB register (Stack B-reg)
SR	: Stack register (Stack PC)
Xreg	: X register (Sub accumulator)

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$P0_0$-$P0_3$	I/O	Parallel input/output : Direction of pins can be set in units of 4 bits. When set at output, each pin serves as a drive with a 15 mA (Typ.) current sinking capability.
$P1_0$-$P1_3$	I/O	Parallel input/output : Direction of pins can be set in units of 4 bits. When set at output, each pin serves as a drive with a 15mA (Typ.) current sinking capability
$P2_0$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes external interrupt input or standby release.
$P2_1$	I/O	Input or output (independent) : Direction of this pin can set independently. Assumes count clock input or standby release.
$P2_2$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes external interrupt input or standby release.
$P2_3$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes standby release or buzzer output (divider clock).
$P3_0$-$P3_3$	I	Parallel input : Accepts input in units of 4 bits. Also assumes A/D pins.
$P4_0$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes A/D pin or SIO data input.
$P4_1$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes A/D pin or SIO data output.
$P4_2$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes A/D pin or SIO clock I/O.
$P4_3$	I/O	Input or output (independent) : Direction of this pin can be set independently. Also assumes A/D pin.
$P5_0$-$P5_3$	I/O	Parallel input/output : Direction of pins can be set in units of 4 bits.
$\overline{RESET}$	I	Hardware reset input : Input to this pin resets the microcomputer. For normal run, connect 0.1 µF (Typ.) across $\overline{RESET}$ and GND pins.
OSC_{IN}, OSC_{OUT}	I, O	Main clock circuit pins. Connecting a crystal across these pins completes main clock oscillator. The divided-by-4 main clock is used as the system clock.
V_{DD}, GND	-	Power supply input to the microcomputer
VR, AGND	-	A/D converter reference voltage : Connect to VR to V_{DD} pin and AGND to GND pin.

NOTES :

1. Hardware reset sets all I/O pins to input.
2. Input ports and I/O ports programmed as input port are provided with pull-up resistors.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}		−0.3 to V_{DD}+0.3	V
Max. Output current	I_{OH}	High-level output current (at each output)	4	mA
	I_{OL0}	Low-level output current ($P0_0$-$P0_3$, $P1_0$-$P1_3$)	30	mA
	I_{OL1}	Low-level output current (all but $P0_0$-$P0_3$, $P1_0$-$P1_3$)	4	mA
Total output current	ΣI_{OH}	High-level output current (all outputs)	20	mA
	ΣI_{OL}	Low-level output current (all outputs)	120	mA
Operating temperature	T_{OPR}		−20 to +70	°C
Storage temperature	T_{STG}		−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		2.0 to 5.5	V
Instruction cycle	t_{CYC}	V_{DD} = 2.0 to 5.5 V	4 to 122	µs
		V_{DD} = 5.0 V ± 10%	1 to 122	
System clock frequency	f_{SYS}	V_{DD} = 2.0 to 5.5 V	250 k to 8.192 k	Hz
		V_{DD} = 5 V ± 10%	1 M to 8.192 k	
Main clock frequency (OSC_{IN}-OSC_{OUT})	f_{OSC}	V_{DD} = 2.0 to 5.5 V	1 M to 32.768 k	Hz
		V_{DD} = 5.0 V ± 10%	4 M to 32.768 k	

DC CHARACTERISTICS

(Ta = –20 to 70°C, Typ. value : V_{DD} = 5.0 or 3.0 V, Unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.0 to 3.3 V	2	25	90	µA	3
			V_{DD} = 4.5 to 5.5 V	25	70	250		
	I_{IH1}	V_{IN} = V_{DD}				2		
	I_{IL2}	V_{IN} = 0 V			1	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}			1	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.0 to 3.3 V	3	15		mA	5
			V_{DD} = 4.5 to 5.5 V	15	25			
	I_{OH1}	V_O = V_{DD} - 0.5 V	V_{DD} = 2.0 to 3.3 V	0.2	1.5			
			V_{DD} = 4.5 to 5.5 V	1.0	2.2			
	I_{OL2}	V_O = 0.5 V	V_{DD} = 2.0 to 3.3 V	70	600		µA	6
			V_{DD} = 4.5 to 5.5 V	400	1 000			
	I_{OH2}	V_O = V_{DD} - 0.5 V	V_{DD} = 2.0 to 3.3 V	200	2 000			
			V_{DD} = 4.5 to 5.5 V	1 000	2 400			
Supply current	I_{DD}	fosc = 2 MHz	V_{DD} = 4.5 to 5.5 V		1 600	3 500	µA	7
		fosc = 1 MHz	V_{DD} = 2.0 to 3.3 V		400	1 100		
			V_{DD} = 4.5 to 5.5 V		850	1 700		
		fosc = 32.768 kHz	V_{DD} = 2.0 to 3.3 V		28	170		
			V_{DD} = 4.5 to 5.5 V		55	220		
	I_{HALT}	fosc = 2 MHz	V_{DD} = 4.5 to 5.5 V		900	1 800	µA	
		fosc = 1 MHz	V_{DD} = 4.5 to 5.5 V		500	1 100		
		fosc = 32.768 kHz	V_{DD} = 2.0 to 3.3 V		20	75		
			V_{DD} = 4.5 to 5.5 V		25	120		
	I_{STOP}	Ceramic OSC mode	V_{DD} = 2.0 to 3.3 V			3		
		Crystal OSC mode	V_{DD} = 2.0 to 5.5 V		20	45		
		(32.786kHz)	V_{DD} = 4.5 to 5.5 V		25	65		
	I_{VR}	A/D active	V_{DD} = 2.0 to 3.3 V		180	420	µA	8
			V_{DD} = 4.5 to 5.5 V		300	650		
		A/D inactive	V_{DD} = 2.0 to 5.5 V			3	µA	9
A/D conversion	n	Resolution			10		bit	
	Differential linearity	fosc = 2 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Linearity	fosc = 2 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	fosc = 2 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		

NOTES :

1. Applicable pins : $P0_0$-$P0_3$, $P1_0$-$P1_3$, $P2_2$, $P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_1$, $P4_3$ (digital input mode), $P5_0$-$P5_3$
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, $P2_0$, $P2_1$, $P4_0$, $P4_2$ (digital input mode)
3. Applicable pins : $P4_0$-$P4_3$, $P3_0$-$P3_3$ (digital input mode), $\overline{RESET}$, $P2_0$-$P2_3$, $P5_0$-$P5_3$, $P0_0$-$P0_3$, $P1_0$-$P1_3$
4. Applicable pins : $P3_0$-$P3_3$, $P4_0$-$P4_3$ (A/D mode)
5. Applicable pins : $P0_0$-$P0_3$, $P1_0$-$P1_3$ (High current port)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (output mode)
7. Non-load condition (A/D conversion disabled) MAX. V_{DD} = 5.5 V (or 3.3 V), T_{OPR} = –20°C
8. Current into VR at A/D conversion mode (run enable status)
9. Current into VR at Non-A/D conversion mode (run disable status)

SYSTEM CONFIGURATION

A Register and X Register

The A register (accumulator : Acc) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM, to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register.

When the table reference instruction PAT is used, the X and A registers load ROM data.

A pair of A and X registers can accommodate 8 bit data.

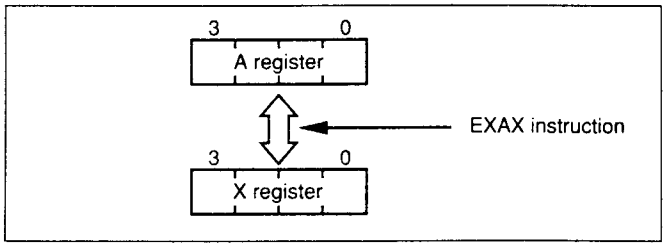


Fig. 1 Data Transfer Example between Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation.

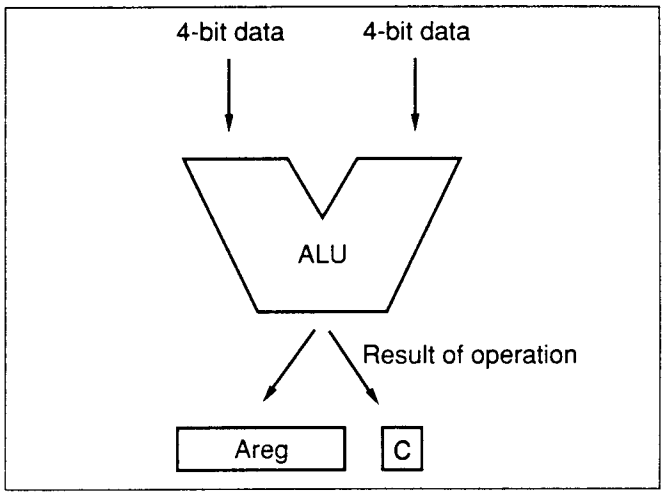


Fig. 2 ALU

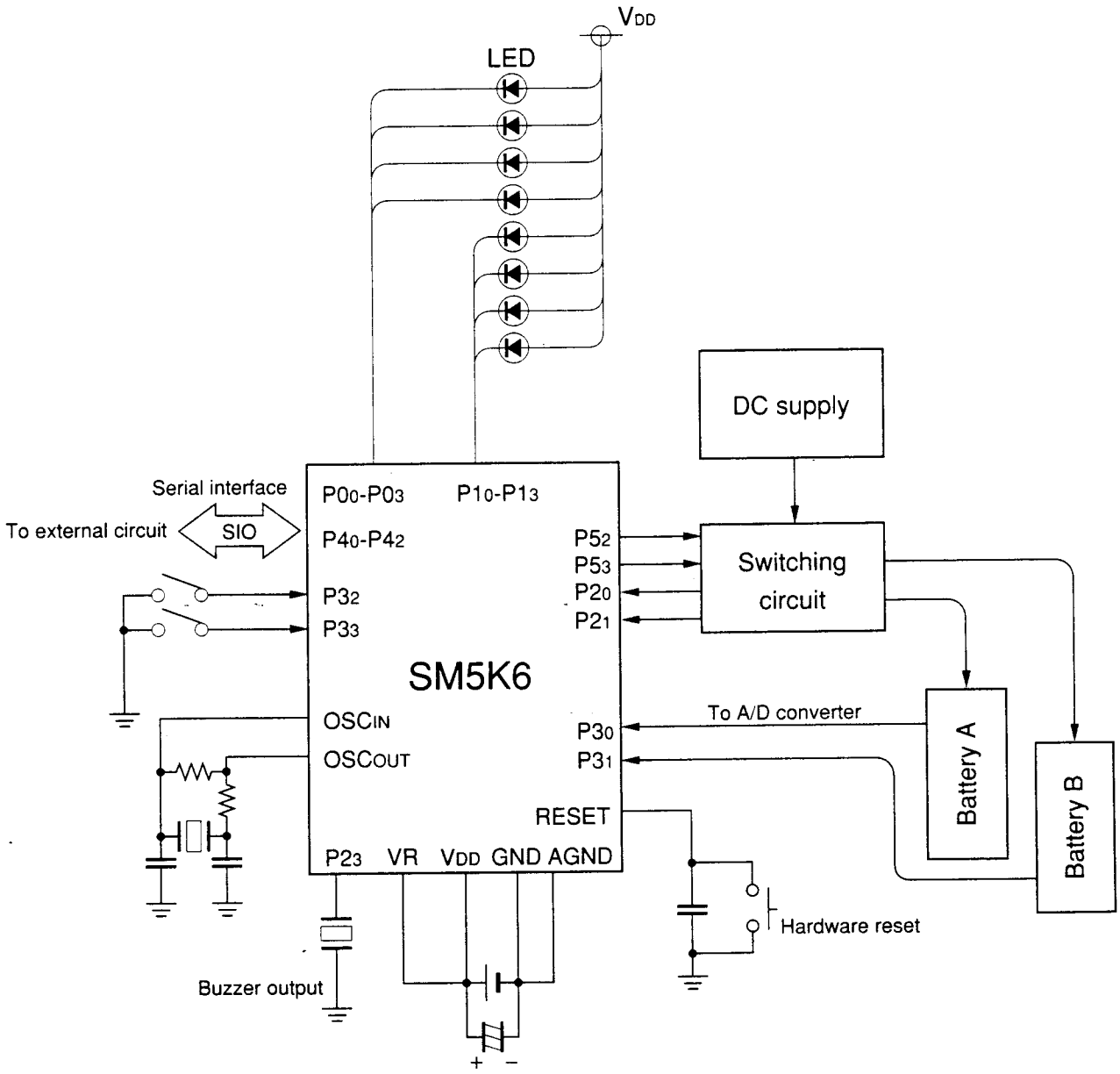
The ALU operates binary addition in conjunction with RAM, C flag and A register. Cy is the symbol for carry signal and not for C flag.

The C flag latches the carry-over as the result of arithmetic instruction. The flag can be set/clear using SC and RC instructions.

The content of C flag can be tested using the TC instruction.

SYSTEM CONFIGURATION EXAMPLE

• **Versatile charger**



Singlechip LH7xxxx ‘790 ‘789 ‘791 SMxxxx ‘K series MCU Microcontroller MPU Microprocessor ARM Advanced RISC Machines Databank LCD Controller LCD Driver Controllers Processors Portable Low Power Low Voltage High Performance Power curve MIPS MIPS/Watt Execution Cycle Multiplier High Speed Compact Handheld System on Chip System Integration Chip Integration Integration Superchip Standard Cell Core Core based IC VHDL Verilog Synthesis Chip on Board COB Chip on Flex COF Device on Board DOB Power Supply Controller Handy Products Development Tools Board Support Software Tools Tools 2.10 Software Support Emulators Evaluation Boards ICE In-Circuit Emulators ROM ICE SME Series Programmable User Configurable RTOS Real Time Operating Systems Third Party Support Software Hardware Yokogawa Digital Cosmic Compiler C Language C Like Assembler Linker Debugger Debug A/D D/A DAC Analog Digital 10-bit 4-bit 8-bit 16-bit 32-bit Address bus Data Bus