

### Applications

- ❑ Bluetooth™ Class 1
- ❑ USB Dongles
- ❑ Laptops
- ❑ Access Points
- ❑ Cordless Piconets

### Features

- ❑ +22.7 dBm at 45% Power Added Efficiency
- ❑ Low current 80mA typical @ Pout=+20 dBm
- ❑ Temperature stability better than 1dB
- ❑ Power-control and Power-down modes
- ❑ Single 3.3 V Supply Operation
- ❑ Temperature Rating: -40C to +85C
- ❑ 8 lead Exposed Pad MSOP Plastic Package

### Ordering Information

Type	Package	Shipping Method
PA2423MB	8 - MSOP	Tape and reel Tubes -samples
PA2423MB-EV	Evaluation kit	

### Product Description

A monolithic, high-efficiency, silicon-germanium power amplifier IC, the PA2423MB is designed for class 1 Bluetooth™ 2.4 GHz radio applications. It delivers +22.7 dBm output power with 45% power-added efficiency – making it capable of overcoming insertion losses of up to 2.7 dB between amplifier output and antenna input in class 1 Bluetooth™ applications.

The amplifier features:

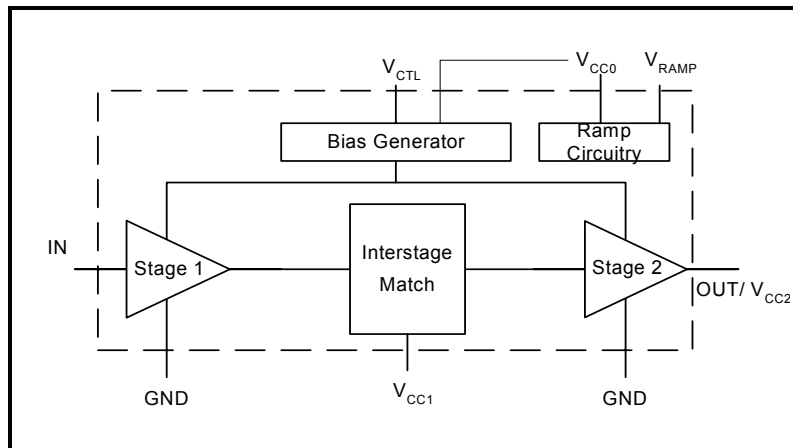
- ❑ an analog control input for improving PAE at reduced output power levels;
- ❑ a digital control input for controlling power up and power down modes of operation.

An on-chip ramping circuit provides the turn-on/off switching of amplifier output with less than 3dB overshoot, meeting the Bluetooth™ specification 1.1.

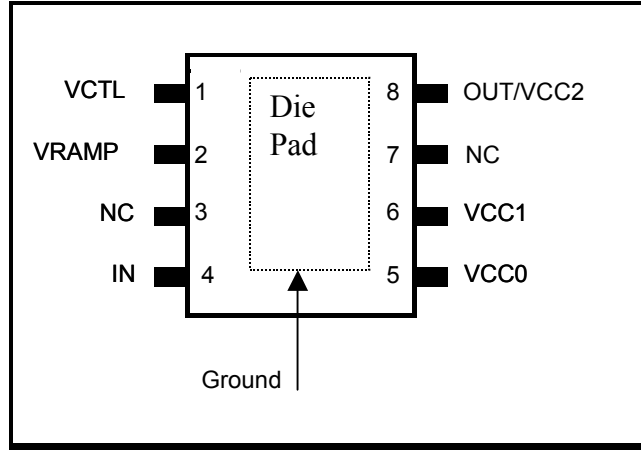
The PA2423MB operates at 3.3V DC. At typical output power level (+22.7 dBm), its current consumption is 125 mA.

The silicon/silicon-germanium structure of the PA2423MB – and its exposed-die-pad package, soldered to the system PCB – provide high thermal conductivity and a subsequently low junction temperature. This device is capable of operating at a duty cycle of 100 percent.

### Functional Block Diagram



**Pin Out Diagram – top view**



**Pin Out Description**

Pin No.	Name	Description
1	V <sub>CTL</sub>	Controls the output level of the power amplifier. An analog control signal between 0V and V <sub>cc</sub> varies the PA output power between minimum and maximum values
2	V <sub>RAMP</sub>	Enable/Disable the power amplifier. A digital control signal with V <sub>cc</sub> logic high (power up) and 0V logic low (power down) is used to turn the device on and off.
3	NC	No connection
4	IN	Power amplifier RF input, external input matching network with DC blocking is required
5	V <sub>CC0</sub>	Bias supply voltage
6	V <sub>CC1</sub>	Stage 1 collector supply voltage, external inter-stage matching network is required
7	NC	No connection
8	OUT/V <sub>CC2</sub>	PA Output and Stage2 collector supply voltage, external output matching network with DC blocking is required
Die Pad	GND	Heatslug Die Pad is ground

### Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	-0.3	+3.6	V
V <sub>CTL</sub>	Control Voltage	-0.3	V <sub>CC</sub>	V
V <sub>RAMP</sub>	Ramping Voltage	-0.3	V <sub>CC</sub>	V
P <sub>IN</sub>	RF Input Power		+8	dBm
T <sub>A</sub>	Operating Temperature Range	-40	+85	°C
T <sub>STG</sub>	Storage Temperature Range	-40	+150	°C
T <sub>j</sub>	Maximum Junction Temperature		+150	°C

Operation in excess of any one of above Absolute Maximum Ratings may result in permanent damage. This device is a high performance RF integrated circuit with ESD rating < 600V and is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

### DC Electrical Characteristics

Conditions: V<sub>CC0</sub> = V<sub>CC1</sub> = V<sub>CC2</sub> = V<sub>RAMP</sub> = 3.3V, V<sub>CTL</sub> = 3.3V, P<sub>IN</sub> = +2dBm, T<sub>A</sub> = 25°C, f = 2.45GHz,  
 Input and Output externally matched to 50Ω, unless otherwise noted.

Symbol	Note	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>		Supply Voltage	3	3.3	3.6	V
I <sub>CC</sub>	1	Supply Current (I <sub>CC</sub> = I <sub>VCC0</sub> + I <sub>VCC1</sub> + I <sub>VCC2</sub> ), V <sub>CTL</sub> = 3.3V		125	150	mA
ΔI <sub>CCtemp</sub>	3	Supply Current variation over temperature from T <sub>A</sub> = 25°C (-40°C < T <sub>A</sub> < +85°C)		25		%
V <sub>CTL</sub>		PA Output Power Control Voltage Range	0		V <sub>CC</sub>	V
I <sub>CTL</sub>	1	Current sourced by V <sub>CTL</sub> Pin		200	250	μA
V <sub>RAMP</sub>	3	Logic High Voltage	2.0			V
	3	Logic Low Voltage			0.8	V
I <sub>stby</sub>	1	Leakage Current when V <sub>ramp</sub> = 0V, V <sub>ctl</sub> = high		0.5	10	μA

### AC Electrical Characteristics

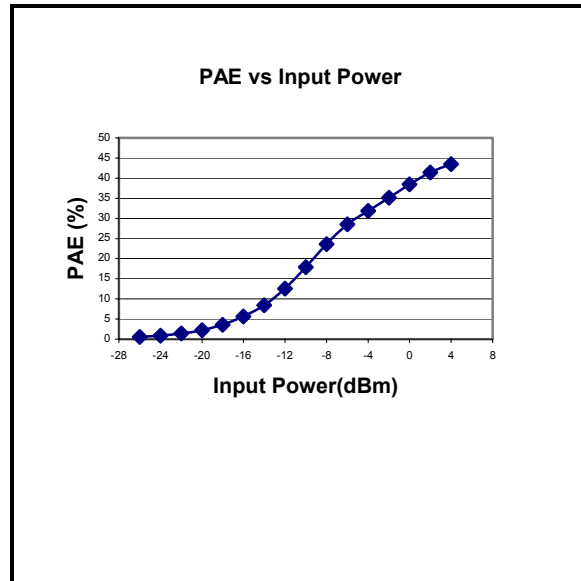
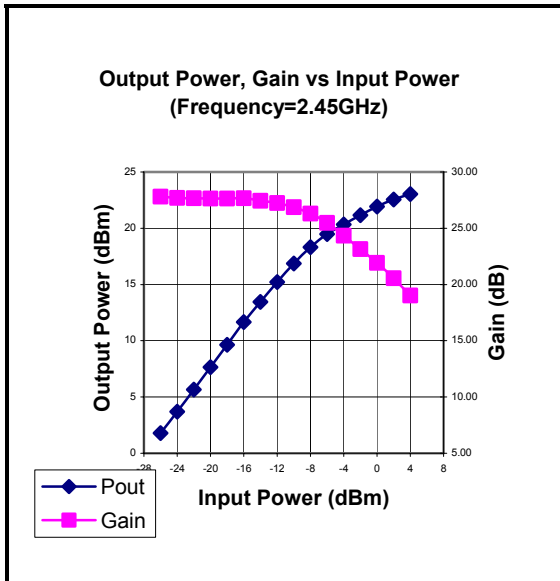
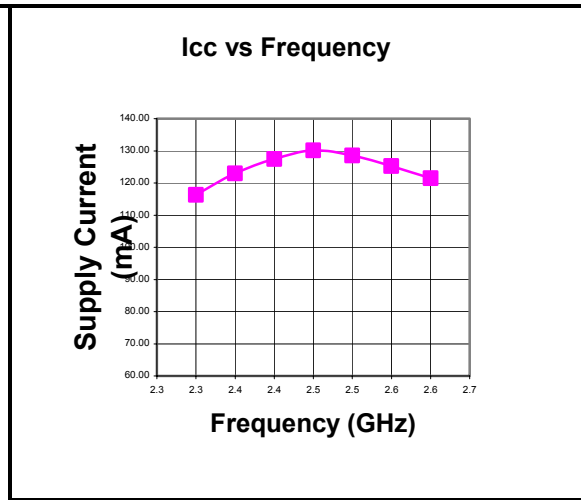
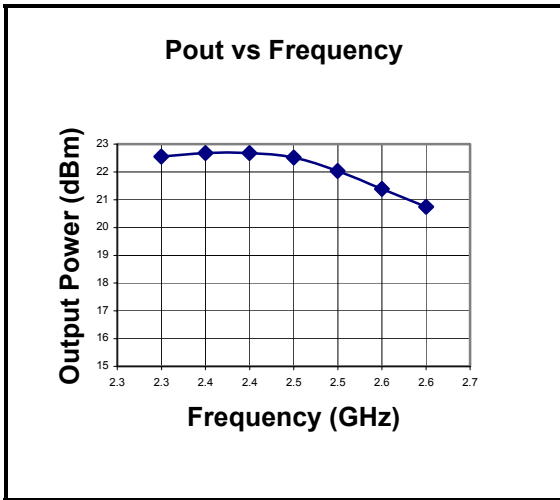
Conditions  $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP} = 3.3V$ ,  $V_{CTL} = 3.3V$ ,  $P_{IN} = +2 \text{ dBm}$ ,  $T_A = 25^\circ\text{C}$ ,  $f = 2.45 \text{ GHz}$ ,  
 Input and Output externally matched to  $50\Omega$ , unless otherwise noted.

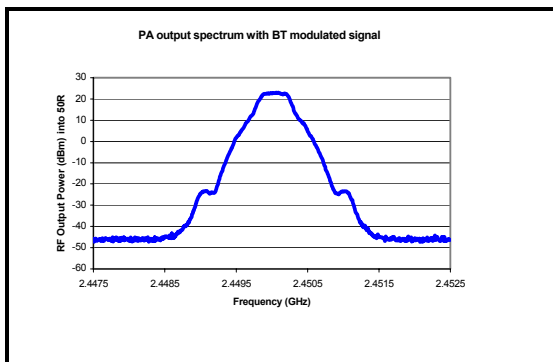
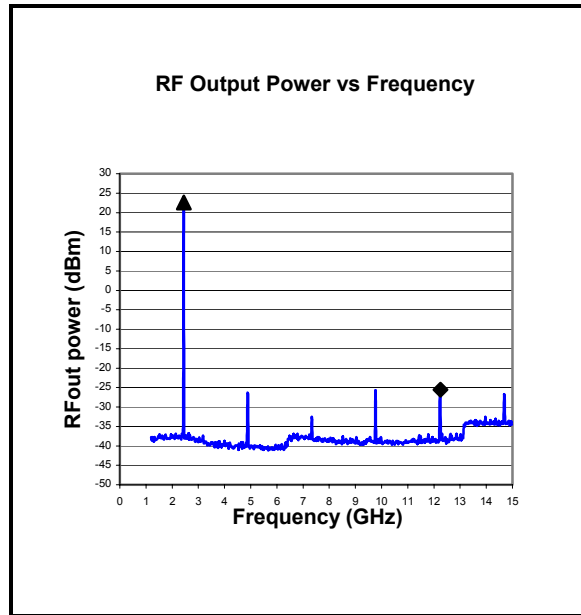
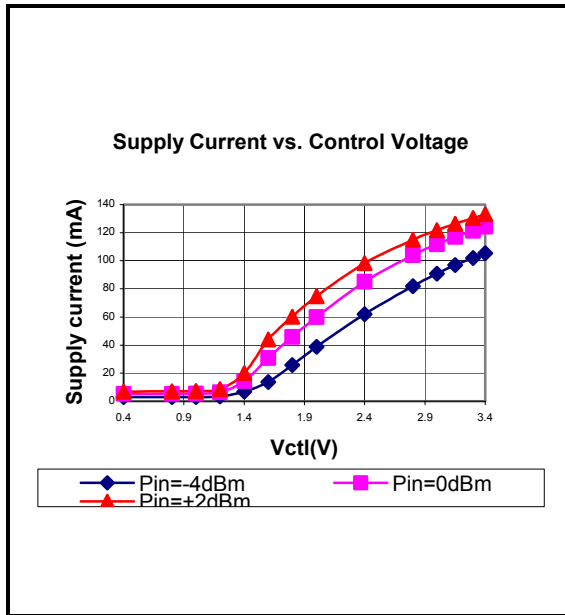
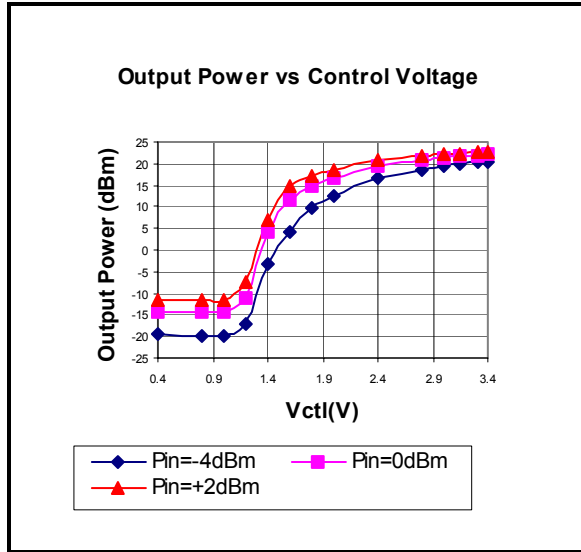
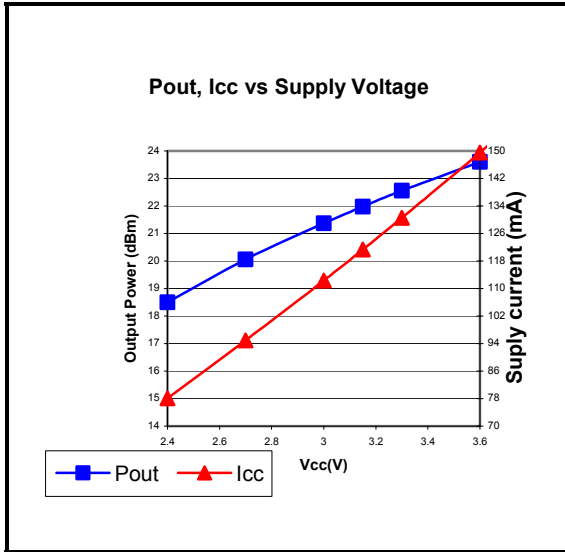
Symbol	Note	Parameter	Min.	Typ.	Max	Unit
$f_{L-U}$	3	Frequency Range	2400		2500	MHz
$P_{out}$	1	Output Power @ $P_{IN} = +2 \text{ dBm}$ , $V_{CTL} = 3.3V$	21	22.7	23.5	dBm
	1	Output Power @ $P_{IN} = +2 \text{ dBm}$ , $V_{CTL} = 0.4V$		-20	0	dBm
$\Delta P_{temp}$	3	Output Power variation over temperature ( $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ )		1	2	dB
$dP_{OUT}/dV_{CTL}$	3	Control Voltage Sensitivity			120	dBm/V
PAE		Power Added Efficiency at +22.5 dBm Output Power		45		%
$G_{VAR}$	3	Gain Variation over band (2400-2500 MHz)		0.7	1.0	dB
2f, 3f, 4f, 5f	3,4	Harmonics		-35	-30	dBc
IS <sub>21</sub> I <sub>OFF</sub>	2	Isolation in "OFF" State, $P_{IN} = +2\text{dBm}$ , $V_{RAMP} = 0V$	20	25		dB
IS <sub>12</sub> I	2	Reverse Isolation	32	42		dB
STAB	2	Stability ( $P_{IN} = +2\text{dBm}$ , Load VSWR = 6:1)	All non-harmonically related outputs less than -50 dBc			

- Notes:**
- (1) Guaranteed by production test at  $T_A = 25^\circ\text{C}$ .
  - (2) Guaranteed by design only
  - (3) Guaranteed by design and characterization
  - (4) Harmonic levels are greatly affected by topology of external matching networks.

**Typical Performance Characteristics**

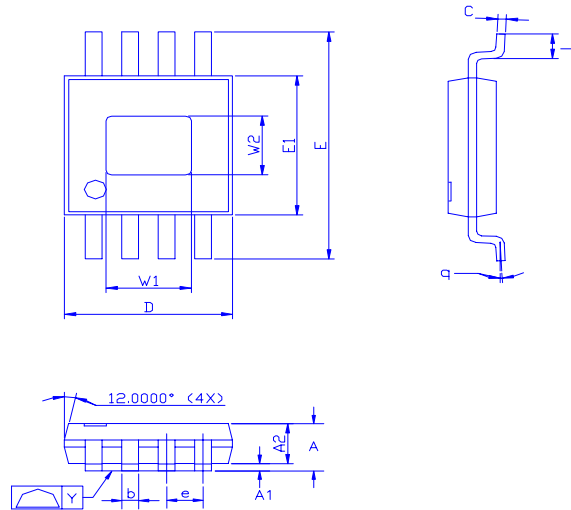
Test Conditions using SiGe PA2423MB-EV:  $V_{CC0}=V_{CC1}=V_{CC2}=V_{RAMP}=3.3V$ ,  $V_{CTL} = 3.3V$ ,  $P_{IN} = +2 \text{ dBm}$ ,  $T_A = 25^\circ\text{C}$ ,  $f = 2.45\text{GHz}$ , Input and Output externally matched to  $50\Omega$ , unless otherwise noted.





### Package Dimensions

The PA2423MB is packaged in a 3.0 mm x 3.0 mm 8 lead MSOP package. The underside of the package is an exposed die-pad structure. This allows for direct soldering to the PCB for enhanced thermal conductivity. The package dimensions are shown in the drawing below.



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	0.92	1.07	0.032	0.036	0.042
A1	0.00	---	0.10	0.000	---	0.004
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	---	0.65	---	---	0.026	---
L	0.40	0.53	0.66	0.016	0.021	0.026
y	---	---	0.10	---	---	0.004
q	0°	---	6°	0°	---	6°
W1	1.27	---	1.52	0.050	---	0.060
W2	1.02	---	1.27	0.040	---	0.050

**NOTE**

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
2. DIMENSION L IS MEASURED IN GAGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

REVISIONS				
ECN	REV	DESCRIPTION	DATE	APPROVED
	1.0	INITIAL RELEASE	Feb 16, 2000	DW



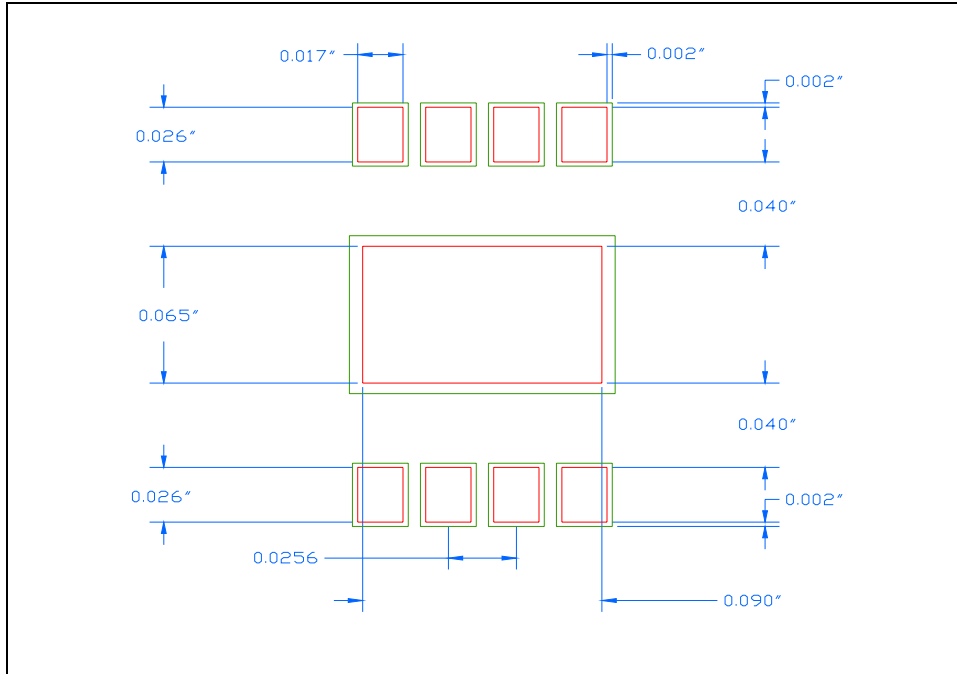
MSOP 8 I/O PACKAGE  
 3 mm X 3 mm BODY SIZE

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DRAWN BY: C.Y. WONG      DATE : Feb 16, 2001  
 APPROVED BY : David Woo      DATE : Feb 16, 2001  
 DIMENSIONS IN MM      PAGE 1 OF 1  
 DO NOT SCALE DRAWING      CODE :

DWG NO.: 01-PO-004      REV. 1.0

**MSOP 8 PCB Footprint Layout**



**Applications Information**

For test and design purposes, SiGe Semiconductor offers an evaluation board for the PA2423MB. The order part number is PA2423MB-EV. The evaluation board is intended to simplify the testing with respect to RF performance of this power amplifier.

The application note, 05AN005 provides the supporting information for using the evaluation board. It contains information on the schematic, bill of materials and recommended layout for the power amplifier and the input and output matching networks. To assist in the design process, this layout is available, upon request, in gerber file format.

In addition, a new optimized layout is available which reduces the number of components used. It achieves this reduction by using printed inductors on the PCB. This layout is available as a gerber file to aid in a quick design cycle. The application note, 05AN008, provides information on this space optimized layout.

**Using V<sub>RAMP</sub>**

V<sub>RAMP</sub> is a digital pin used to power-up and power-down the PA2423MB in Time Duplex systems such as Bluetooth™ 1.1. During receive mode, V<sub>RAMP</sub> voltage is pulled down, PA2423MB acts as a 25 dB isolation block between the radio and the antenna while consuming a modest 1uA. In transmit mode, V<sub>RAMP</sub> voltage is pulled to VCC and PA2423MB offers 19 dB to 21dB of large signal gain. The rise and fall time are in the order of 1-2usec.

**Using V<sub>CTL</sub>**

V<sub>CTL</sub> is an analog pin that is designed to control the gain of PA2423MB. Applying a voltage between 0V and Vcc will adjust the gain between -15dB and 21 dB. Used in combination with a variable drive level to



PA2423MB, the  $V_{CTL}$  function can greatly optimize the PAE of the system at all four Bluetooth™ transmitted power levels.

By applying approximately 1.4V to  $V_{CTL}$ , for example, a Class1 radio can be modified to a Class2 radio with the PA2423MB consuming only 15mA.

By implementing a resistor DAC, the  $V_{CTL}$  pin can interface with Bluetooth™ transceivers offering digital and programmable outputs.

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