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The S-29X91A Series is high speed, low power 1K/2K/4K-bit serial E<sup>2</sup>PROM with a wide operating voltage range. They are organized as 64-word × 16-bit, 128-word × 16-bit and 256-word × 16-bit, respectively. Each is capable of sequential read, where addresses are automatically incremented in 16-bit blocks.

The S-29X91A Series is capable of protecting the memory, 50% of which can be protected starting from address 00.

Interface is structured so that this IC can be directly connected to the CPU with serial ports. 8-bit instructions make it easy to prepare your own software.

■ Features

- Low power consumption
  - Standby : 1.0 μA Max. (V<sub>CC</sub> = 6.5 V)
  - Operating : 0.8 mA Max. (V<sub>CC</sub> = 5.5 V)
  - 0.4 mA Max. (V<sub>CC</sub> = 2.5 V)
- Wide operating voltage range
  - Write : 2.5 to 6.5 V
  - Read : 1.8 to 6.5 V
- Sequential read capable
- Memory Protection
- Can be easily connected to the serial port
- CS Active "H"
- Endurance : 10<sup>5</sup> cycles/word
- Data retention : 10 years
- S-29191A : 1 Kbits
- S-29291A : 2 Kbits
- S-29391A : 4 Kbits

■ Pin Assignment

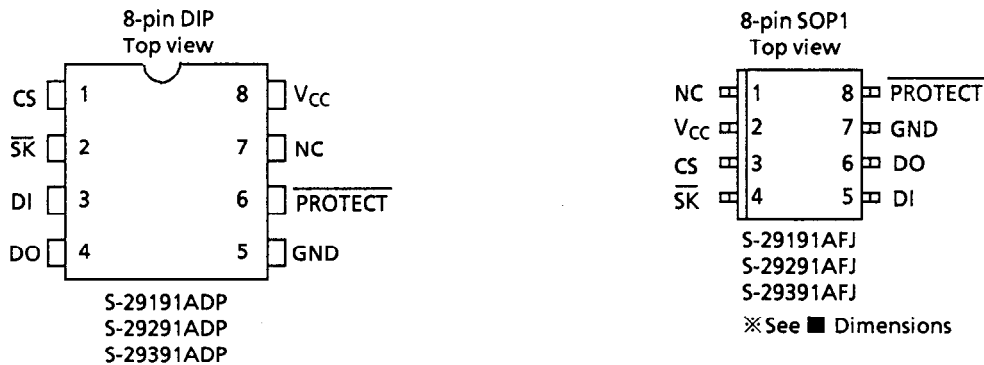


Figure 1

■ Pin Functions

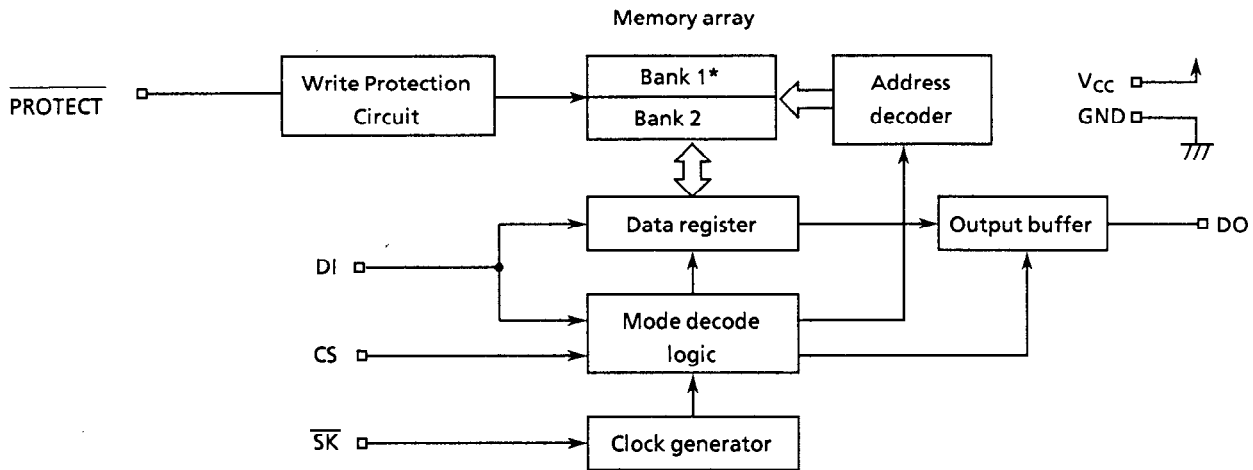
Table 1

Name	Pin Number		Function
	DIP	SOP1	
CS	1	3	Chip select input
SK	2	4	Serial clock input
DI	3	5	Serial data input
DO	4	6	Serial data output
GND	5	7	Ground
PROTECT	6	8	Memory Protection Control Input Connected to GND or Open : Protection Valid Connected to Vcc : Protection Invalid
NC	7	1	No Connection
V <sub>CC</sub>	8	2	Power supply

# CMOS SERIAL E<sup>2</sup>PROM

## S-29X91A Series

### ■ Block Diagram



\* 50% of the memory can be protected starting from address 00.

Figure 2

### ■ Instruction Set

Table 2

Instruction	Start Bit	Ope code	Address			Data
			S-29191A	S-29291A	S-29391A	
READ (Read data)	1	1000xxx	xx A5toA0	x A6toA0	A7toA0	D <sub>15</sub> to D <sub>0</sub> Output*
PROGRAM (Program data)	1	x100xxx	xx A5toA0	x A6toA0	A7toA0	D <sub>15</sub> to D <sub>0</sub> Input
WRAL (Write all)	1	0001xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	D <sub>15</sub> to D <sub>0</sub> Input
ERAL (Erase all)	1	0010xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PEN (Program enable)	1	0011xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PDS (Program disable)	1	0000xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—

x : Doesn't matter.

\* : When 16-bit data of the specified address is output, the data of the next address is output.

### ■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V <sub>CC</sub>	- 0.3 to + 7.0	V
Input voltage	V <sub>IN</sub>	- 0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	- 0.3 to V <sub>CC</sub>	V
Storage temperature under bias	T <sub>bias</sub>	- 50 to + 95	°C
Storage temperature	T <sub>stg</sub>	- 65 to + 150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V <sub>CC</sub>	Read Operation	1.8	—	6.5	V
		Write Enable/Disable				
		Write Operation	2.5	—	6.5	V
High level input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 5.5 to 6.5 V	0.8 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
		V <sub>CC</sub> = 4.5 to 5.5 V	2.0	—	V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.7 to 4.5 V	0.8 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8 to 2.7 V	0.8 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 5.5 to 6.5 V	0.0	—	0.2 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 4.5 to 5.5 V	0.0	—	0.8	V
		V <sub>CC</sub> = 2.7 to 4.5 V	0.0	—	0.2 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8 to 2.7 V	0.0	—	0.15 × V <sub>CC</sub>	V
Operating temperature	T <sub>OPR</sub>		-40	—	+85	°C

■ Pin Capacitance

Table 5

(T<sub>a</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	—	—	8	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V	—	—	10	pF

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N <sub>W</sub>	10 <sup>5</sup>	—	—	cycles/word

■ DC Characteristics

Table 7

Parameter	Smb1	Conditions	V <sub>CC</sub> = 5.5 V to 6.5 V			V <sub>CC</sub> = 4.5 to 5.5 V			V <sub>CC</sub> = 2.5 to 4.5 V			V <sub>CC</sub> = 1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I <sub>CC1</sub>	DO unloaded	—	—	1.0	—	—	0.8	—	—	0.6	—	—	0.4	mA
Current consumption (PROGRAM)	I <sub>CC2</sub>	DO unloaded	—	—	2.5	—	—	2.0	—	—	1.5				mA

Table 8

Parameter	Smb1	Conditions	V <sub>CC</sub> = 4.5 V to 6.5 V			V <sub>CC</sub> = 2.5 to 4.5 V			V <sub>CC</sub> = 1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I <sub>SB</sub>	CS = GND DO = Open Other input: Connected to V <sub>CC</sub> or GND	—	—	1.0	—	—	0.6	—	—	0.4	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	—	—	0.45							V
		I <sub>OL</sub> = 100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4	—	—							V
		I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.7	—	—				V
		I <sub>OH</sub> = -10 μA	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.3	—	—	V
Write enable latch data hold voltage	V <sub>DH</sub>	Only when program disable mode	1.5	—	—	1.5	—	—	1.5	—	—	V
Pull-down current	I <sub>PD</sub>	PROTECT terminal = V <sub>CC</sub>	15	—	100	3	—	50	1	—	10	μA

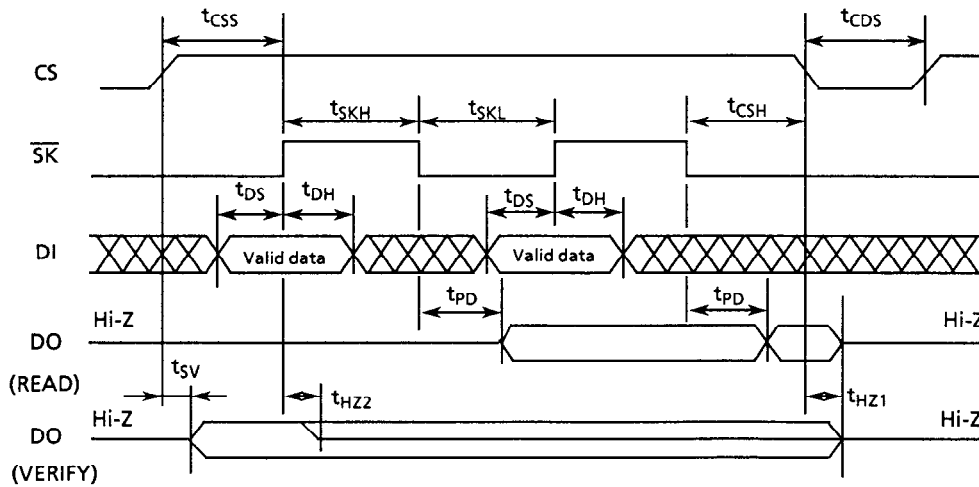
■ AC Characteristics

Table 9 Measuring conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100pF

Table 10

Parameter	Smb1	$V_{CC} = 4.5$ to $6.5V$			$V_{CC} = 2.5$ to $4.5V$			$V_{CC} = 1.8$ to $2.5V$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	$t_{CSS}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu s$
CS hold time	$t_{CSH}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu s$
CS deselect time	$t_{CDS}$	0.2	—	—	0.2	—	—	0.4	—	—	$\mu s$
Data setup time	$t_{DS}$	0.2	—	—	0.4	—	—	0.8	—	—	$\mu s$
Data hold time	$t_{DH}$	0.2	—	—	0.4	—	—	0.8	—	—	$\mu s$
Output delay time	$t_{PD}$	—	—	0.4	—	—	1.0	—	—	2.0	$\mu s$
Clock frequency	$f_{SK}$	0	—	2.0	0	—	0.5	—	—	0.25	MHz
Clock pulse width	$t_{SKH}$ $t_{SKL}$	0.25	—	—	1.0	—	—	2.0	—	—	$\mu s$
Output disable time	$t_{HZ1}$ $t_{HZ2}$	0	—	0.15	0	—	0.5	0	—	1.0	$\mu s$
Output enable time	$t_{SV}$	0	—	0.15	0	—	0.5	0	—	1.0	$\mu s$
Programming time	$t_{PR}$	—	4.0	10.0	—	4.0	10.0				ms



Input data is retrieved on the rising edge of  $\overline{SK}$ .  
Output data is triggered on the falling edge of  $\overline{SK}$ .

Figure 3 Timing Chart

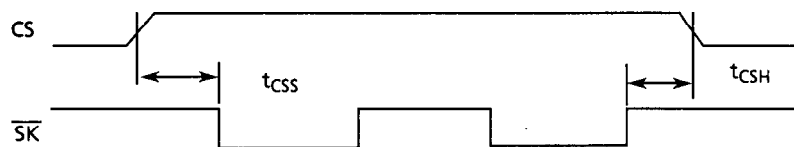


Figure 4 Timing Chart for  $t_{CSS}$  and  $t_{CSH}$  when  $\overline{SK}$  is "H"

■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of  $\overline{SK}$  after CS goes high. A start-bit can only be recognized when the high of DI is latched at the rising edge of  $\overline{SK}$  after changing CS to high, it is impossible for it to be recognized as long as DI is low, even if there are  $\overline{SK}$  pulses after CS goes high. Instruction finishes when CS goes low, where it must be low between commands during  $t_{CDS}$ .

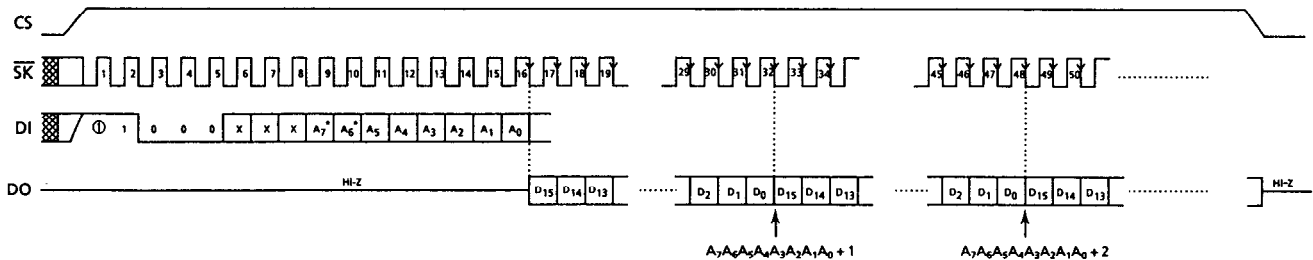
All input, including DI and  $\overline{SK}$  signals, is ignored while CS is low, which is stand-by mode. The start bit + instruction, address, and data are 8-bit instructions. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

1. READ

The READ instruction reads data from a specified address. After A0 is latched at the rising edge of  $\overline{SK}$ , 16-bit data is continuously output in synchronization with the falling edge of  $\overline{SK}$ .

When all of the data (D<sub>15</sub> to D<sub>0</sub>) in the specified address has been read, data in the next address can be read with the input of another  $\overline{SK}$  clock. Thus, the data over whole area of the memory can be read by continuously inputting  $\overline{SK}$  clocks as long as CS is high.

The last address (A<sub>n</sub> ... A<sub>1</sub> A<sub>0</sub> = 1 ... 11) rolls over to the top address (A<sub>n</sub> ... A<sub>1</sub> A<sub>0</sub> = 0 ... 00).



\* On the S-29191A, A<sub>7</sub> and A<sub>6</sub> are optional.  
On the S-29291A, A<sub>7</sub> is optional.

Figure 5 Read Timing (S-29391A)

2. Write (PROGRAM ,WRAL, ERAL)

The write instructions (PROGRAM, WRAL, ERAL) automatically begins writing to the non-volatile memory when CS goes low at the completion of the specified clock input.

The write operation is completed in 10 ms ( $t_{PR}$  Max.), and the typical write period is less than 5 ms. In the S-29X94A Series, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting CS to high and checking the DO pin, which is low during the write operation and high after its completion. This VERIFY procedure can be executed over and over again.

There are two methods to detect a change in the DO output. One is to detect a change from low to high setting CS to high, and the other is to detect a change from low to high as a result of repetitious operations of returning the CS to low after setting CS to high and checking the DO output.

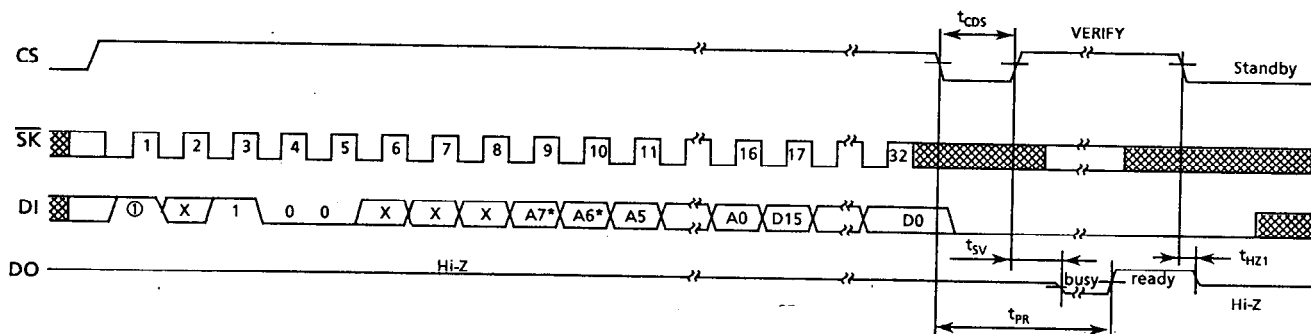
Because all  $\overline{SK}$  and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedence state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedence state upon the recognition of a high of DI (start-bit) attached to the rising edge of an  $\overline{SK}$  pulse.

DI input should be low during the VERIFY procedure.

2.1 PROGRAM

This instruction writes 16-bit data to a specified address.

After changing CS to high, input a start-bit, op-code (PROGRAM), address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing CS to low will start the PROGRAM operation. It is not necessary to make the data "1" before initiating the PROGRAM operation.



\* On the S-29191A, A<sub>7</sub> and A<sub>6</sub> are optional.  
On the S-29291A, A<sub>7</sub> is optional.

Figure 6 WRITE Timing (S-29391A)



# CMOS SERIAL E<sup>2</sup>PROM S-29X91A Series

## 2.2 Write all (WRAL)

This instruction writes the same 16-bit data into every address.

After changing CS to high, input a start-bit, op-code (WRAL), address (optional), and 16-bit data. If there is a data overflow of more than 16 bits, the write data is shifted for every clock in succession and only the last 16-bit data is valid. Changing CS to low starts the WRAL operation. It is not necessary to make the data "1" before initiating the WRAL operation.

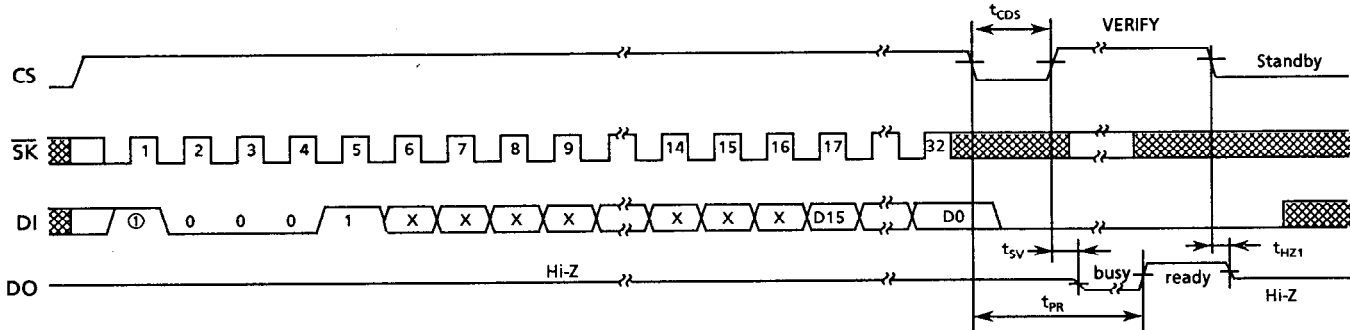


Figure 7 WRAL Timing

## 2.3 Erase all (ERAL)

This instruction erases the data in every address. All data changes to "1."

After changing CS to high, input a start-bit, op-code (ERAL), and address (optional). It is not necessary to input data. Changing CS to low starts the ERAL operation.

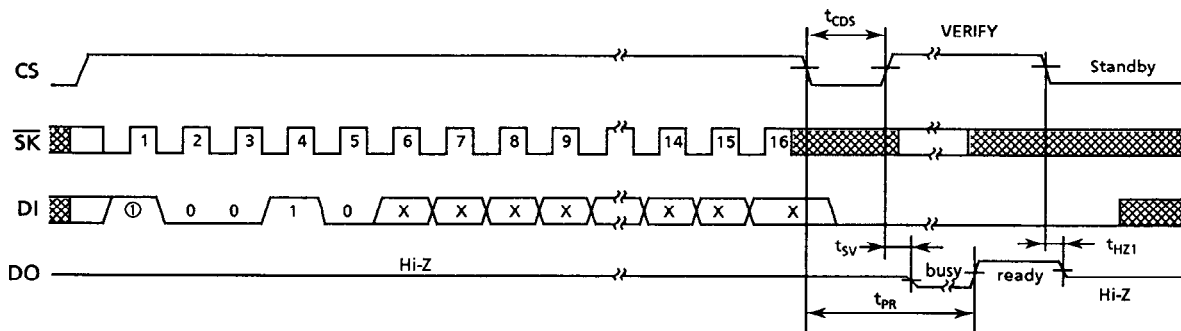


Figure 8 ERAL Timing

## 3. Write enable (PEN) and Write disable (PDS)

The PEN instruction puts the S-29X94A Series into write enable mode, which accepts PROGRAM, WRAL, and ERAL instruction. The PDS instruction puts the S-29X94A Series into write disable mode, which refuses PROGRAM, WRAL, and ERAL instruction.

The S-29X94A Series powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

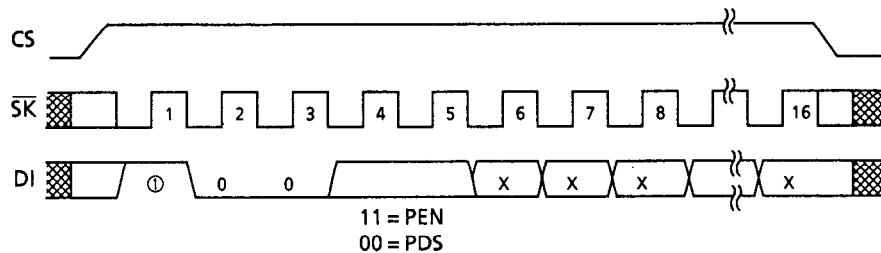


Figure 9 PEN/PDS Timing

### ■ Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of  $\overline{SK}$  after changing CS to high (Start-Bit Recognition). The write operation begins by inputting the write instruction and setting CS to low. The DO pin then outputs low during the write operation and high at its completion by setting CS to high (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having CS go high, the DO pin is switched from a state of high-impedence to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedence (see Figure 3).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

### ■ Three-Wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to CS,  $\overline{SK}$ , DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI (See Figure 10).

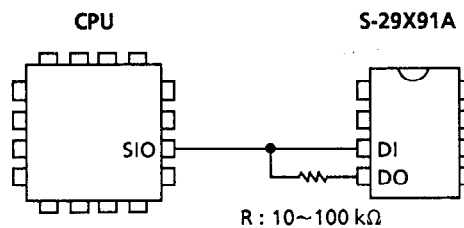
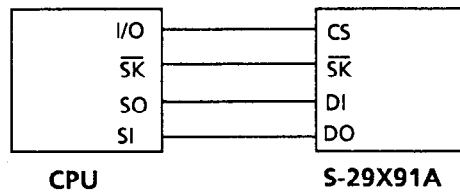
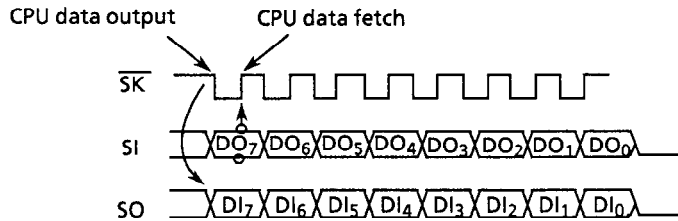


Figure 10 3-wire interface

■ **Connecting to the CPU with Serial Port**



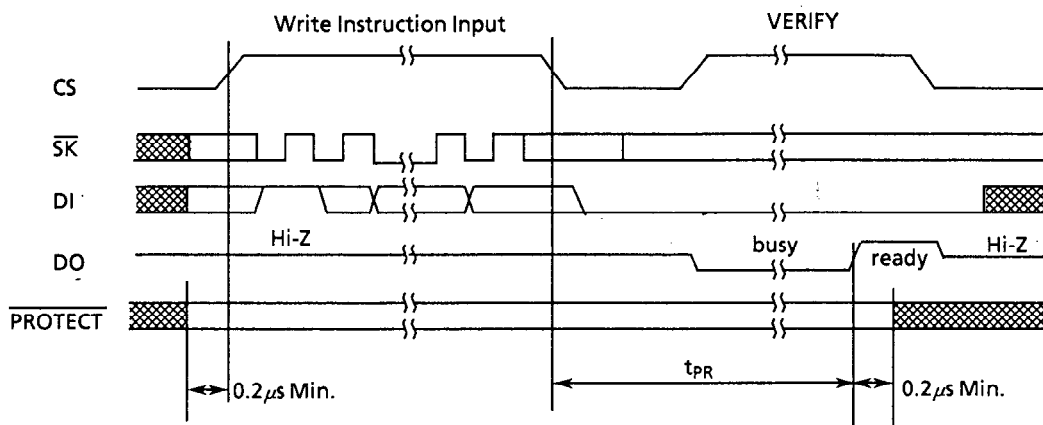
**Figure 11 Connectin Example**



**Figure 12 Serial Shift Timing**

■ **Memory Protection**

The S-29X91A Series is capable of protecting the memory. So, the contents of the memory will not be miswritten due to error run or malfunction of the CPU. When the  $\overline{\text{PROTECT}}$  terminal is connected to GND or OPEN, write to Bank 1 in the memory array is prohibited (50% of the memory can be protected starting from address 00). Because the pull-down resistance is connected to the  $\overline{\text{PROTECT}}$  terminal internally, the memory can be automatically protected when the  $\overline{\text{PROTECT}}$  terminal is OPEN. When the protection is valid, the data in the memory of Bank 1 will not be rewritten. However, because the write control circuit inside the IC functions, the next instruction cannot be executed during the time period of writing ( $t_{PR}$ ). While write instruction is being input and write is being executed, always connect the  $\overline{\text{PROTECT}}$  terminal to "H," "L" or OPEN, and leave the input signal unchanged (see Figure 13).



**Figure 13 PROTECT Terminal Input Signal Timing**

■ Dimensions (Unit : mm)

1. 8-pin DIP

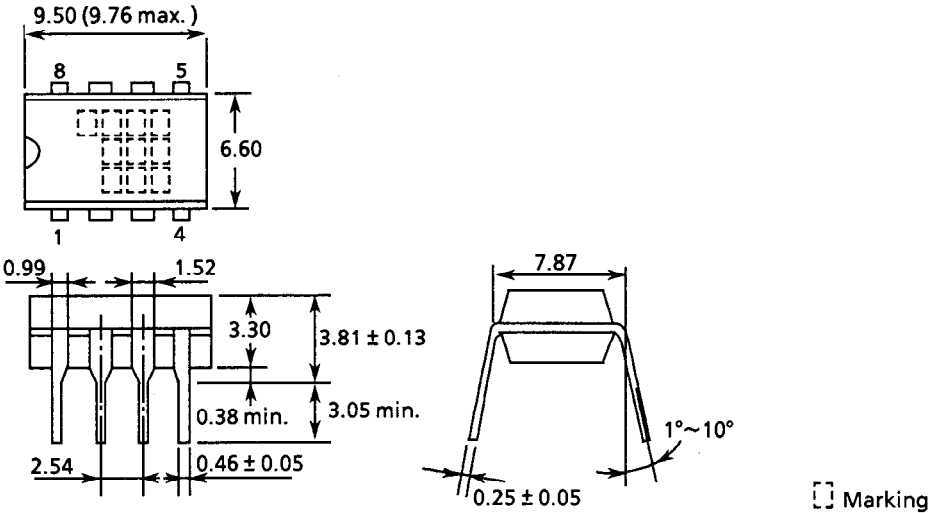


Figure 14

2. 8-pin SOP

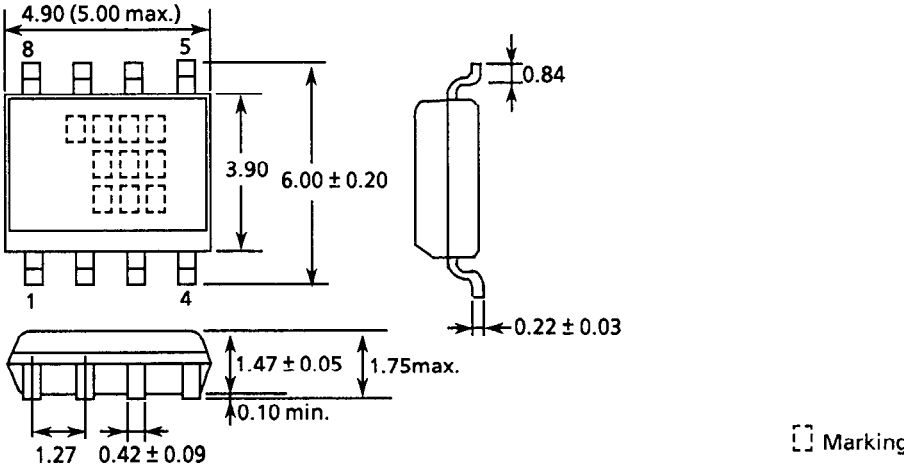
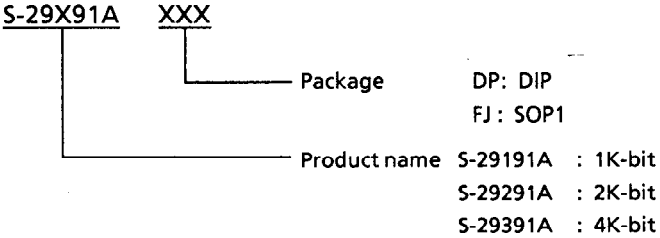


Figure 15

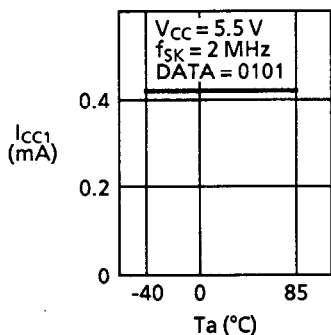
■ Ordering Information



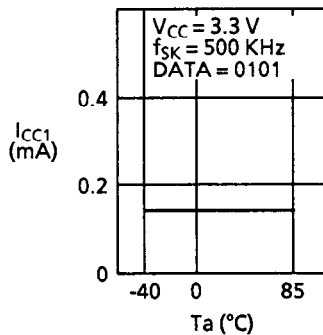
■ **Characteristics**

1. DC Characteristics

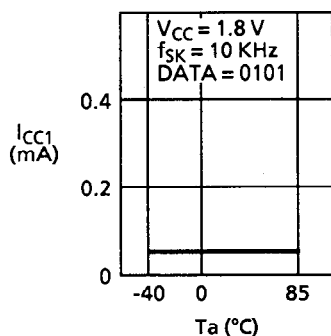
1.1 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



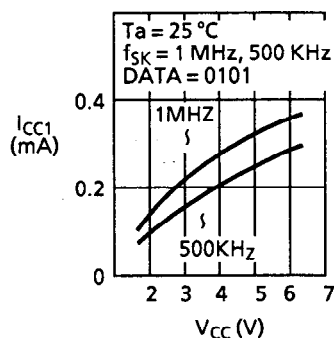
1.2 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



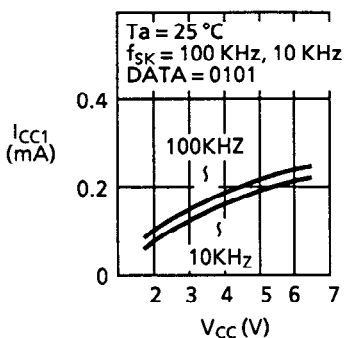
1.3 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



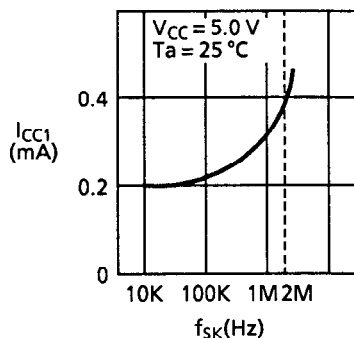
1.4 Current consumption (READ)  $I_{CC1}$  — Power supply voltage  $V_{CC}$



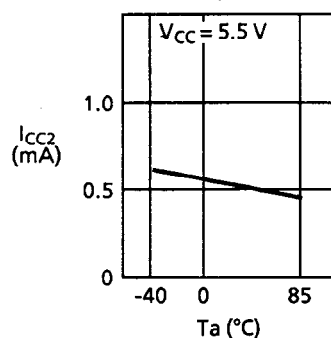
1.5 Current consumption (READ)  $I_{CC1}$  — Power supply voltage  $V_{CC}$



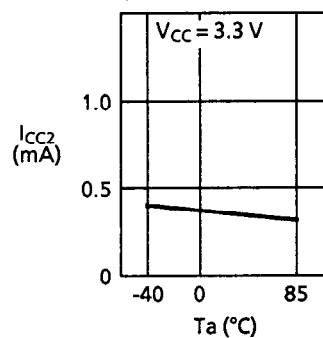
1.6 Current consumption (READ)  $I_{CC1}$  — Clock frequency  $f_{SK}$



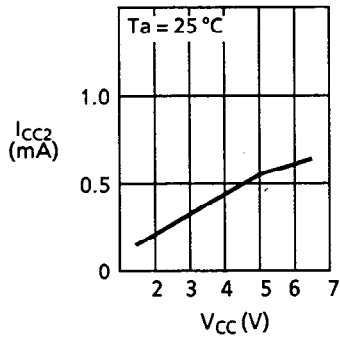
1.7 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



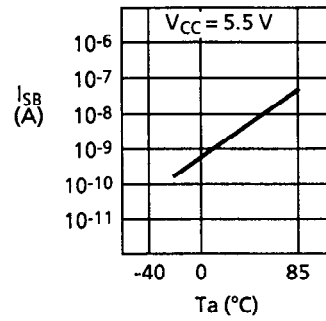
1.8 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



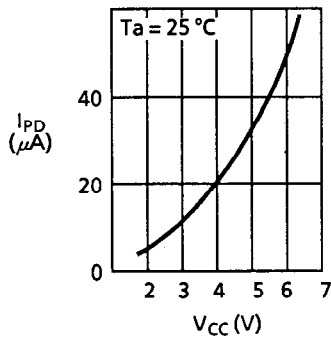
1.9 Current consumption (PROGRAM)  $I_{CC2}$  – Power supply voltage  $V_{CC}$



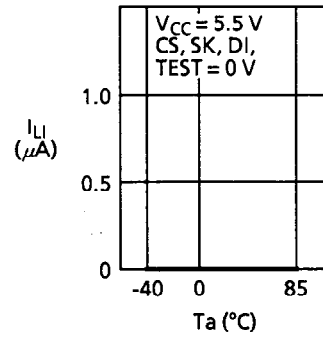
1.10 Standby current consumption  $I_{SB}$  – Ambient temperature  $T_a$



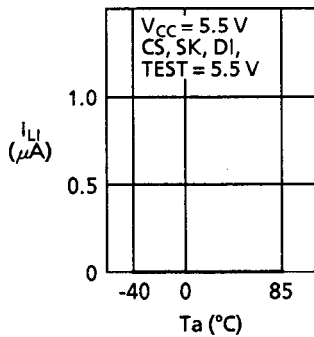
1.11 Pull-Down current  $I_{PD}$  – Power supply voltage  $V_{CC}$



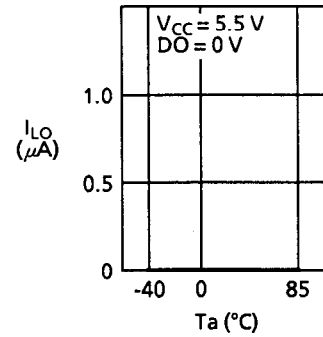
1.12 Input leakage current  $I_{LI}$  – Ambient temperature  $T_a$



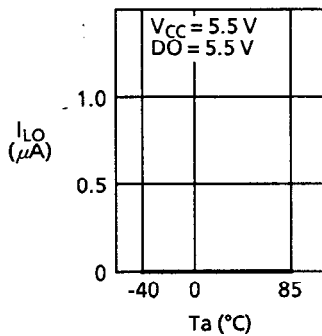
1.13 Input leakage current  $I_{LI}$  – Ambient temperature  $T_a$



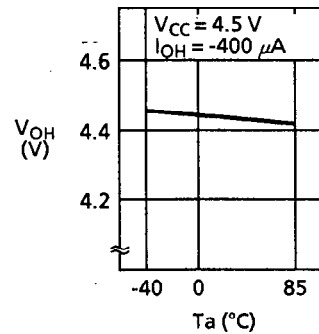
1.14 Output leakage current  $I_{LO}$  – Ambient temperature  $T_a$



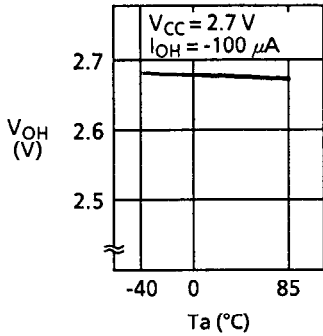
1.15 Output leakage current  $I_{LO}$  – Ambient temperature  $T_a$



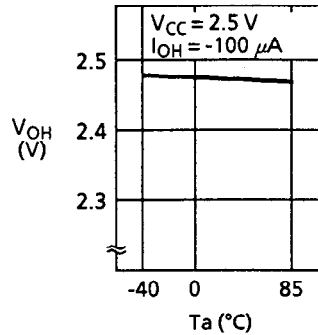
1.16 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



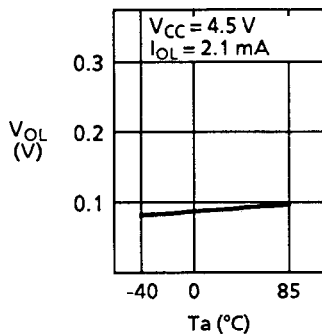
1.17 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



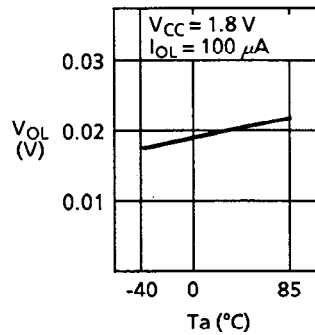
1.18 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



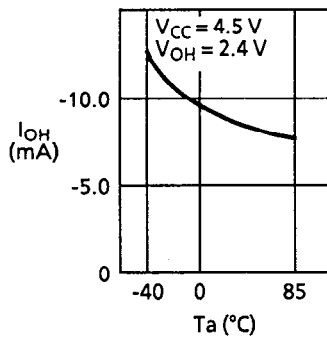
1.19 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



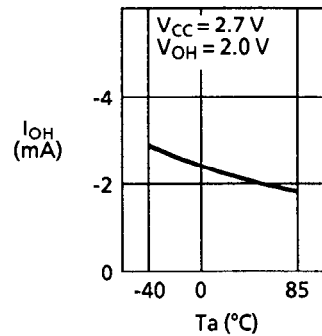
1.20 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



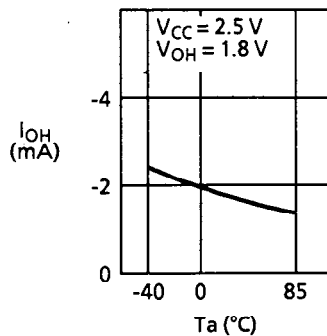
1.21 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



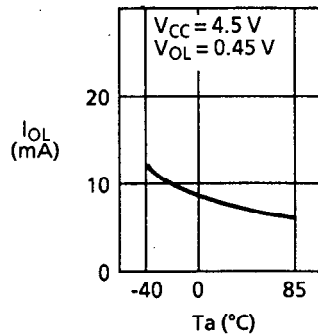
1.22 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



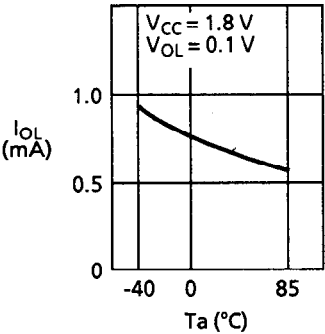
1.23 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



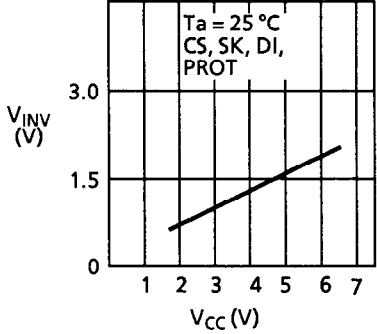
1.24 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



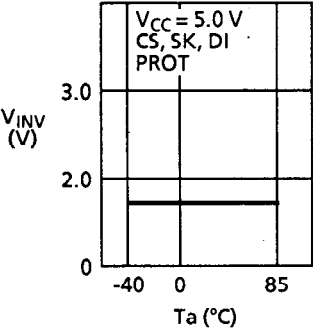
1.25 Low level output current  $I_{OL}$  - Ambient temperature  $T_a$



1.26 Input inversion voltage  $V_{INV}$  - Power supply voltage  $V_{CC}$



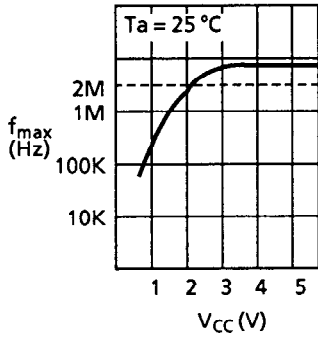
1.27 Input inversion voltage  $V_{INV}$  - Ambient temperature  $T_a$



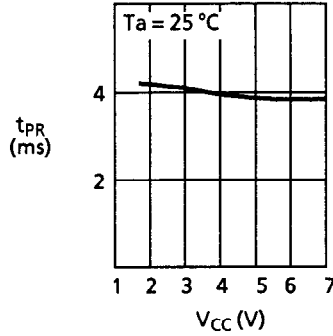


**2. AC Characteristics**

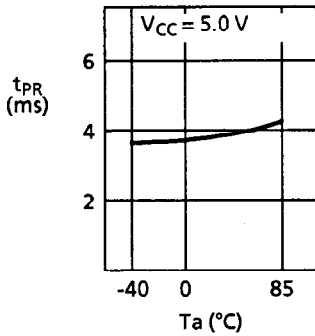
**2.1 Maximum operating frequency  $f_{max}$  - Power supply voltage  $V_{CC}$**



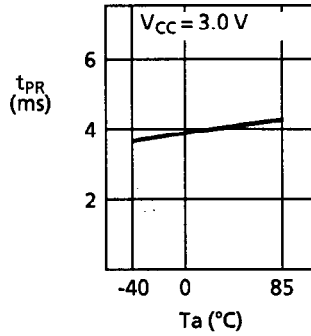
**2.2 Program time  $t_{PR}$  - Power supply voltage  $V_{CC}$**



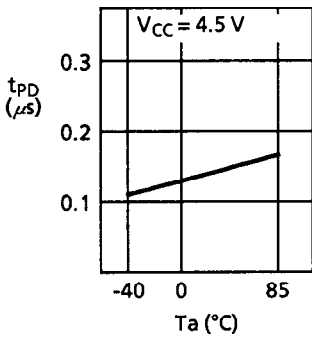
**2.3 Program time  $t_{PR}$  - Ambient temperature  $T_a$**



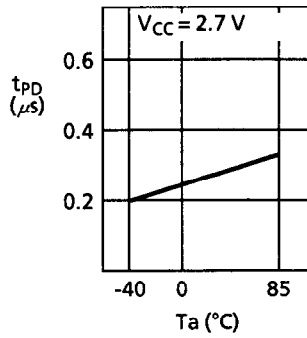
**2.4 Program time  $t_{PR}$  - Ambient temperature  $T_a$**



**2.5 Data output delay time  $t_{PD}$  - Ambient temperature  $T_a$**



**2.6 Data output delay time  $t_{PD}$  - Ambient temperature  $T_a$**



**2.7 Data output delay time  $t_{PD}$  - Ambient temperature  $T_a$**

