64-bit THERMAL HEAD DRIVER

S-4601A

The S-4601A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. The 75 μm driver output pad pitch allows for high density mounting up to 300dpi. It can be used for general purpose because "H" or "L" can be selected for the latch and the driver enable .

■ Features

- Low current consumption : 0.3 mA typ.
  (f_{CLK} = 2 MHz, SI : fixed)
- High speed operation : 7 MHz (chip)
  5MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 15 mA typ.
  (V_{OL} = 1.5 V, Ta = -10 to 80°C)
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls
- Selectable "H/L" for latch and driver enable

■ Block Diagram

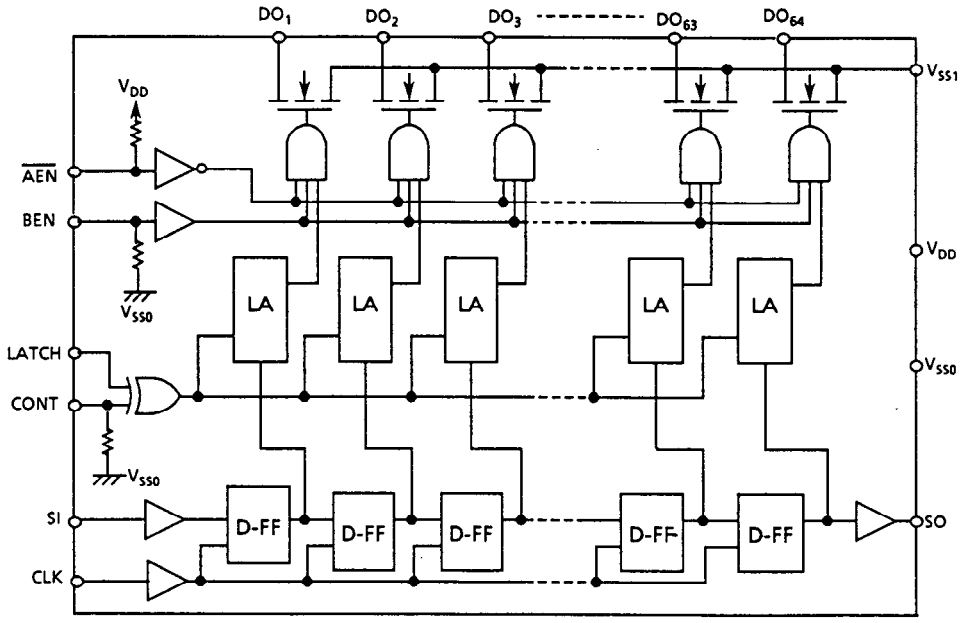


Figure 1

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit operates depending on the levels of CONT and LATCH ; it reads the data of the shift register when their levels are the same, and it holds the data of the shift register when they differ.

The latch data are output to the respective drivers when $\overline{AEN}$ is low and BEN is high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{AEN}$ high or BEN low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO_1 to DO_{64} (DOn)	Driver output terminals (Nch open-drain)
65, 66, 73, 74, 80, 81	V_{SS1}	GND for driver (0 V)
71, 78	V_{DD}	Positive power supply for logic (+ 5 V)
67, 75	V_{SS0}	GND for logic (0 V)
77	CLK	Clock input terminal for 64-bit shift register
79	SI	Serial data input terminal for 64-bit shift register
68	SO	Serial data output terminal for 64-bit shift register
69	LATCH	Data latch signal input terminal When CONT = "L" or open LATCH = "L": reads the data of the shift register LATCH = "H": holds the preceding data When CONT = "H" LATCH = "L": holds the preceding data LATCH = "H": reads the data of the shift register
72	CONT	Data latch signal control terminal : selects "H" or "L" for LATCH(pull-down resistor is built in)
76	$\overline{AEN}$	Driver enable terminal : outputs the latch data to the driver when "L" (pull-up resistor is built in)
70	BEN	Driver enable terminal : outputs the latch data to the driver when "H" (pull-down resistor is built in)

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{SS0,1} - V_{DD}$	-0.4 to + 7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	30	mA
Input voltage	V_{IN}	V_{SS0}-0.5 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS0}-0.5 to V_{DD} + 0.5	V
Max. junction temperature	T_{jMAX}	125	°C
Operating temperature	T_{opr}	-10 to + 80	°C
Storage temperature	T_{stg}	-40 to + 125	°C

■ DC Electrical Characteristics

Table 3

(Unless otherwise specified : V_{DD} = 5.0 V ± 10%, Ta = -10°C to 80°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
High level input voltage	V_{IH}			0.7 × V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}			V_{SS}	—	0.3 × V_{DD}	V
High level input current	I_{IH}	V_{DD} = 5.0 V, V_{IH} = 5.0 V, Ta = 25°C	BEN, CONT	—	—	35	μA
				—	—	0.5	μA
Low level input current	I_{IL}	V_{DD} = 5.0 V, V_{IL} = 0 V, Ta = 25°C	$\overline{AEN}$	-35	—	—	μA
				-0.5	—	—	μA
High level output voltage	V_{OH}	SO terminal, no load		4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load		—	—	0.05	V
High level output current	I_{OH}	SO terminal, V_{OH} = V_{DD}-0.4 V		—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, V_{OL} = 0.4 V		0.5	—	—	mA
High level driver output voltage	V_{DOH}			—	24	26	V
Low level driver output voltage	V_{DOL}	I_{DOL} = 15 mA		—	0.7	1.5	V
Driver leakage current	I_{LEAK}	V_{DOH} = 26 V, Per 1-bit of driver output		—	—	1.0	μA
Current consumption	I_{DD}	f_{CLK} = 2 MHz, Ta = 25°C, SI : fixed		—	0.3	1.0	mA
Lower V_{DD} detection voltage	V_{DET}			2.0	—	4.0	V

■ AC Electrical Characteristics

Table 4

(V_{DD} = 5.0 V ± 10%, Ta = -10°C to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	V_{IH} = V_{DD}, V_{IL} = V_{SS0}	50	—	—	ns
Data hold time	t_{HD}	V_{IH} = V_{DD}, V_{IL} = V_{SS0}	10	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	C_L = 3 pF	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L = 3 kΩ, V_{DOH} = 24 V	—	—	2.0	μs
DOn rise time	t_{rDO}	R_L = 3 kΩ, V_{DOH} = 24 V	—	1.0	2.0	μs
DOn fall time	t_{fDO}	R_L = 3 kΩ, V_{DOH} = 24 V	—	0.4	1.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

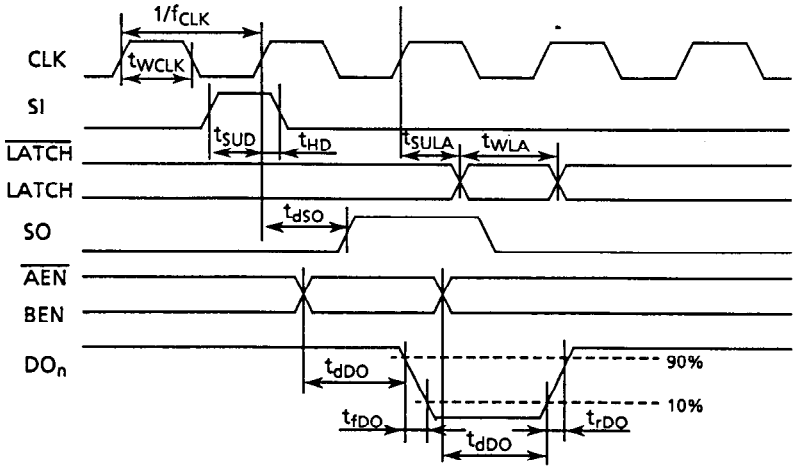
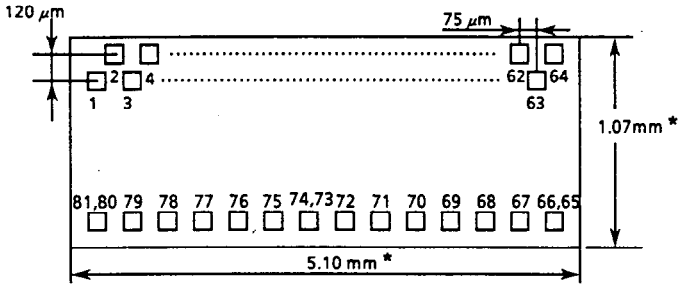


Figure 2

■ Dimensions



Pad size : 80 μm × 80 μm
(passivation opening)
Pad pitch : 75 μm
Chip thickness : 350 ± 30 μm

*Before dicing

Figure 3

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5

Unit : μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO_1	-2362.5	310	28	DO_{28}	-337.5	430	55	DO_{55}	1687.5	310
2	DO_2	-2287.5	430	29	DO_{29}	-262.5	310	56	DO_{56}	1762.5	430
3	DO_3	-2212.5	310	30	DO_{30}	-187.5	430	57	DO_{57}	1837.5	310
4	DO_4	-2137.5	430	31	DO_{31}	-112.5	310	58	DO_{58}	1912.5	430
5	DO_5	-2062.5	310	32	DO_{32}	-37.5	430	59	DO_{59}	1987.5	310
6	DO_6	-1987.5	430	33	DO_{33}	37.5	310	60	DO_{60}	2062.5	430
7	DO_7	-1912.5	310	34	DO_{34}	112.5	430	61	DO_{61}	2137.5	310
8	DO_8	-1837.5	430	35	DO_{35}	187.5	310	62	DO_{62}	2212.5	430
9	DO_9	-1762.5	310	36	DO_{36}	262.5	430	63	DO_{63}	2287.5	310
10	DO_{10}	-1687.5	430	37	DO_{37}	337.5	310	64	DO_{64}	2362.5	430
11	DO_{11}	-1612.5	310	38	DO_{38}	412.5	430	65	V_{SS1}	2395.0	-430
12	DO_{12}	-1537.5	430	39	DO_{39}	487.5	310	66	V_{SS1}	2275.0	-430
13	DO_{13}	-1462.5	310	40	DO_{40}	562.5	430	67	V_{SS0}	2112.5	-430
14	DO_{14}	-1387.5	430	41	DO_{41}	637.5	310	68	SO	1788.5	-430
15	DO_{15}	-1312.5	310	42	DO_{42}	712.5	430	69	LATCH	1268.5	-430
16	DO_{16}	-1237.5	430	43	DO_{43}	787.5	310	70	BEN	1012.5	-430
17	DO_{17}	-1162.5	310	44	DO_{44}	862.5	430	71	V_{DD}	640.5	-430
18	DO_{18}	-1087.5	430	45	DO_{45}	937.5	310	72	CONT	292.5	-430
19	DO_{19}	-1012.5	310	46	DO_{46}	1012.5	430	73	V_{SS1}	16.5	-430
20	DO_{20}	-937.5	430	47	DO_{47}	1087.5	310	74	V_{SS1}	-103.5	-430
21	DO_{21}	-862.5	310	48	DO_{48}	1162.5	430	75	V_{SS0}	-273.5	-430
22	DO_{22}	-787.5	430	49	DO_{49}	1237.5	310	76	$\overline{AEN}$	-545.5	-430
23	DO_{23}	-712.5	310	50	DO_{50}	1312.5	430	77	CLK	-981.5	-430
24	DO_{24}	-637.5	430	51	DO_{51}	1387.5	310	78	V_{DD}	-1819.5	-430
25	DO_{25}	-562.5	310	52	DO_{52}	1462.5	430	79	SI	-2041.5	-430
26	DO_{26}	-487.5	430	53	DO_{53}	1537.5	310	80	V_{SS1}	-2275.0	-430
27	DO_{27}	-412.5	310	54	DO_{54}	1612.5	430	81	V_{SS1}	-2395.0	-430