64-bit THERMAL HEAD DRIVER

S-4620A

The S-4620A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It can be used for general purpose because "H" or "L" can be selected for the latch and the driver enable. It is ideal for the bar-code printer and the thermal print head of high-speed printing because of its large driver output current of 50 mA.

■ Features

- Low current consumption : 0.4 mA typ. (f_{CLK} = 5 MHz, SI : fixed)
- High speed operation : 7 MHz (chip) 5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 50 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls
- Selectable "H/L" for latch and driver enable

■ Block Diagram

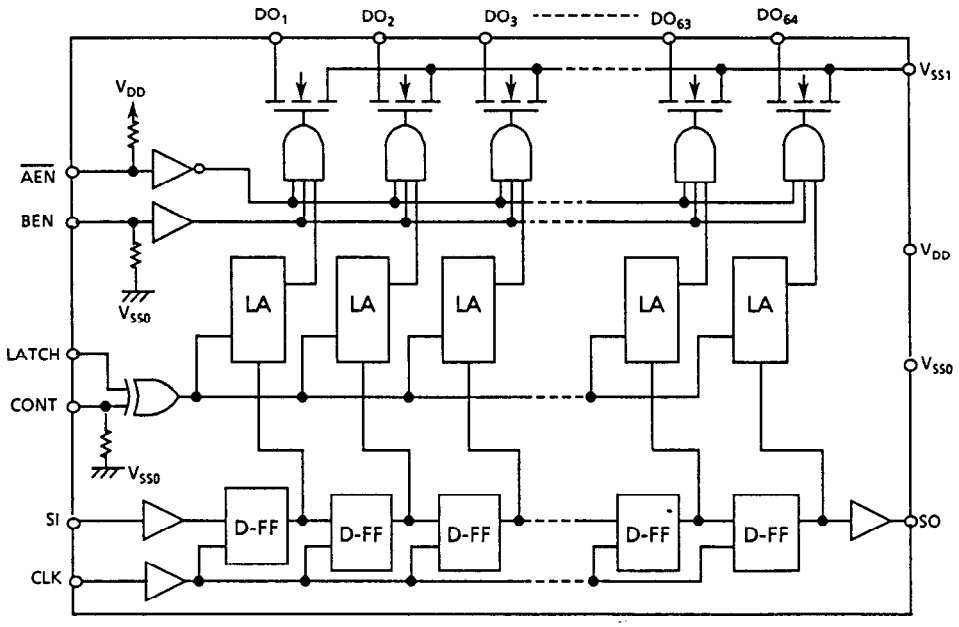


Figure 1

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit operates depending on the levels of CONT and LATCH ; it reads the data of the shift register when their levels are the same, and it holds the data of the shift register when they differ.

The latch data are output to the respective drivers when $\overline{AEN}$ is low and BEN is high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{AEN}$ high or BEN low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO_1 to DO_{64} (DO_n)	Driver output terminals (Nch open-drain)
65, 66, 73, 74, 80, 81	V_{SS1}	GND for driver (0 V)
71, 78	V_{DD}	Positive power supply for logic (+ 5 V)
67, 75	V_{SS0}	GND for logic (0 V)
77	CLK	Clock input terminal for 64-bit shift register
79	SI	Serial data input terminal for 64-bit shift register
68	SO	Serial data output terminal for 64-bit shift register
69	LATCH	Data latch signal input terminal When CONT = "L" or open LATCH = "L": reads the data of the shift register LATCH = "H": holds the preceding data When CONT = "H" LATCH = "L": holds the preceding data LATCH = "H": reads the data of the shift register
72	CONT	Data latch signal control terminal : selects "H" or "L" for LATCH (pull-down resistor is built in)
76	$\overline{AEN}$	Driver enable terminal : outputs the latch data to the driver when low (pull-up resistor is built in)
70	BEN	Driver enable terminal : outputs the latch data to the driver when high (pull-down resistor is built in)

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{SS0,1} - V_{DD}$	-0.4 to + 7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	50	mA
Input voltage	V_{IN}	V_{SS0}-0.5 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS0}-0.5 to V_{DD} + 0.5	V
Max. junction temperature	T_{jMAX}	125	°C
Operating temperature	T_{opr}	-10 to + 80	°C
Storage temperature	T_{stg}	-40 to + 125	°C

■ DC Electrical Characteristics

Table 3

(Unless otherwise specified : V_{DD} = 5.0 V ± 10%, Ta = -10°C to 80°C)

Parameter	Sybl	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
High level input voltage	V_{IH}			0.7 × V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}			V_{SS}	—	0.3 × V_{DD}	V
High level input current	I_{IH}	V_{DD} = 5.0 V, V_{IH} = 5.0 V, Ta = 25°C	BEN, CONT	—	—	35	μA
				—	—	0.5	μA
Low level input current	I_{IL}	V_{DD} = 5.0 V, V_{IL} = 0 V, Ta = 25°C	$\overline{AEN}$	-35	—	—	μA
				-0.5	—	—	μA
High level output voltage	V_{OH}	SO terminal, no load		4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load		—	—	0.05	V
High level output current	I_{OH}	SO terminal, V_{OH} = V_{DD}-0.4 V		—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, V_{OL} = 0.4 V		0.5	—	—	mA
High level driver output voltage	V_{DOH}			—	24	26	V
Low level driver output voltage	V_{DOL}	I_{DOL} = 30 mA, V_{DD} = 5.0 V		—	0.7	1.5	V
Driver leakage current	I_{LEAK}	V_{DOH} = 26 V, Per 1-bit of driver output		—	—	1.0	μA
Current consumption	I_{DD}	Ta = 25°C	f_{CLK} = 2 MHz, SI : fixed	—	0.2	0.6	mA
			f_{CLK} = 5 MHz, SI : fixed	—	0.4	1.2	mA
			f_{CLK} = 5 MHz, SI = 1/2f_{CLK}	—	1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}			2.0	—	4.0	V

■ AC Electrical Characteristics

Table 4

(V_{DD} = 5.0 V ± 10%, Ta = -10°C to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	V_{IH} = V_{DD}, V_{IL} = V_{SS0}	50	—	—	ns
Data hold time	t_{HD}	V_{IH} = V_{DD}, V_{IL} = V_{SS0}	10	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	C_L = 3 pF	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L = 1.5 kΩ, V_{DOH} = 24 V	—	—	3.0	μs
DOn rise time	t_{rDO}	R_L = 1.5 kΩ, V_{DOH} = 24 V	—	1.0	3.0	μs
DOn fall time	t_{fDO}	R_L = 1.5 kΩ, V_{DOH} = 24 V	—	1.0	3.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

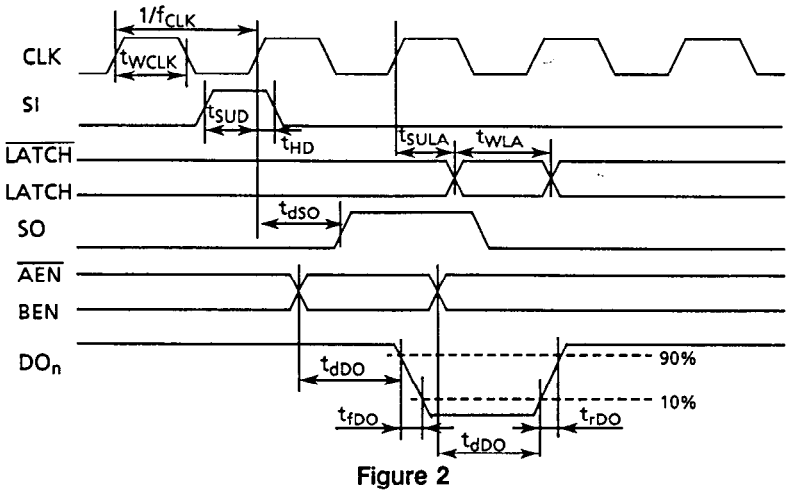
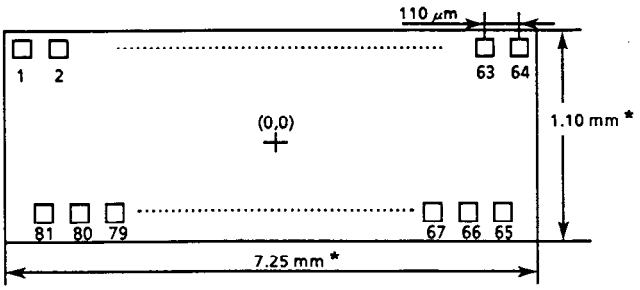


Figure 2

■ Dimensions



Pad size : 80 μm × 80 μm
(passivation opening)
Pad pitch :
110 μm (driver output pad)
Chip thickness : 350 ± 30 μm

*Before dicing

Figure 3

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5

Unit: μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO_1	-3465	445	28	DO_{28}	-495	445	55	DO_{55}	2475	445
2	DO_2	-3355	445	29	DO_{29}	-385	445	56	DO_{56}	2585	445
3	DO_3	-3245	445	30	DO_{30}	-275	445	57	DO_{57}	2695	445
4	DO_4	-3135	445	31	DO_{31}	-165	445	58	DO_{58}	2805	445
5	DO_5	-3025	445	32	DO_{32}	-55	445	59	DO_{59}	2915	445
6	DO_6	-2915	445	33	DO_{33}	55	445	60	DO_{60}	3025	445
7	DO_7	-2805	445	34	DO_{34}	165	445	61	DO_{61}	3135	445
8	DO_8	-2695	445	35	DO_{35}	275	445	62	DO_{62}	3245	445
9	DO_9	-2585	445	36	DO_{36}	385	445	63	DO_{63}	3355	445
10	DO_{10}	-2475	445	37	DO_{37}	495	445	64	DO_{64}	3465	445
11	DO_{11}	-2365	445	38	DO_{38}	605	445	65	V_{SS1}	3455	-445
12	DO_{12}	-2255	445	39	DO_{39}	715	445	66	V_{SS1}	3335	-445
13	DO_{13}	-2145	445	40	DO_{40}	825	445	67	V_{SS0}	2855	-445
14	DO_{14}	-2035	445	41	DO_{41}	935	445	68	SO	2455	-445
15	DO_{15}	-1925	445	42	DO_{42}	1045	445	69	LATCH	2005	-445
16	DO_{16}	-1815	445	43	DO_{43}	1155	445	70	BEN	1605	-445
17	DO_{17}	-1705	445	44	DO_{44}	1265	445	71	V_{DD}	1135	-445
18	DO_{18}	-1595	445	45	DO_{45}	1375	445	72	CONT	685	-445
19	DO_{19}	-1485	445	46	DO_{46}	1485	445	73	V_{SS1}	60	-445
20	DO_{20}	-1375	445	47	DO_{47}	1595	445	74	V_{SS1}	-60	-445
21	DO_{21}	-1265	445	48	DO_{48}	1705	445	75	V_{SS0}	-460	-445
22	DO_{22}	-1155	445	49	DO_{49}	1815	445	76	$\overline{AEN}$	-940	-445
23	DO_{23}	-1045	445	50	DO_{50}	1925	445	77	CLK	-1360	-445
24	DO_{24}	-935	445	51	DO_{51}	2035	445	78	V_{DD}	-2445	-445
25	DO_{25}	-825	445	52	DO_{52}	2145	445	79	SI	-2845	-445
26	DO_{26}	-715	445	53	DO_{53}	2255	445	80	V_{SS1}	-3335	-445
27	DO_{27}	-605	445	54	DO_{54}	2365	445	81	V_{SS1}	-3455	-445