The S-4630A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It can be easily used for general purpose because "H" or "L" can be selected for the driver enable and the latch is fixed to "L". It is ideal for the thermal print head of 200 dpi or 8 dots/mm because of its driver output pad pitch of 110 μm.

■ Features

- Low current consumption : 0.4 mA typ.
  (f_{CLK} = 5 MHz, SI : fixed)
- High speed operation : 7 MHz (chip)
  5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 9 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls

■ Block Diagram

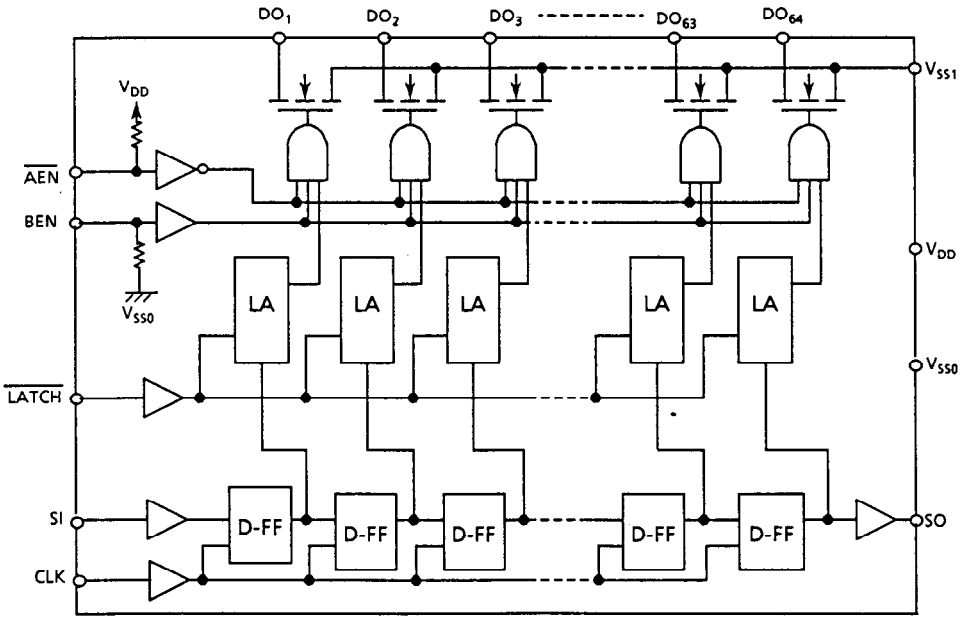


Figure 1

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit reads the data of the shift register when it is "L" level, and it holds the preceding data when it is "H" level.

The latch data are output to the respective drivers when $\overline{AEN}$ is low and BEN is high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{AEN}$ high or BEN low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO_1 to DO_{64} (DO_n)	Driver output terminals (Nch open-drain)
65, 66, 71, 72, 79, 80	V_{SS1}	GND for driver (0 V)
68, 75	V_{DD}	Positive power supply for logic (+ 5 V)
70, 73	V_{SS0}	GND for logic (0 V)
76	CLK	Clock input terminal for 64-bit shift register
78	SI	Serial data input terminal for 64-bit shift register
67	SO	Serial data output terminal for 64-bit shift register
77	$\overline{LATCH}$	Data latch signal input terminal $\overline{LATCH}$ = "L": reads the data of the shift register $\overline{LATCH}$ = "H": holds the preceding data
74	$\overline{AEN}$	Driver enable terminal : outputs the latch data to the driver when low(pull-up resistor is built in)
69	BEN	Driver enable terminal : outputs the latch data to the driver when high(pull-down resistor is built in)

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{SS0,1} - V_{DD}$	-0.4 to + 7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	15	mA
Input voltage	V_{IN}	V_{SS0}-0.5 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS0}-0.5 to V_{DD} + 0.5	V
Max. junction temperature	T_{jMAX}	125	°C
Operating temperature	T_{opr}	-10 to + 80	°C
Storage temperature	T_{stg}	-40 to + 125	°C

■ DC Electrical Characteristics

Table 3

(Unless otherwise specified : V_{DD} = 5.0 V ± 10%, Ta = -10°C to 80°C)

Parameter	Sybl	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
High level input voltage	V_{IH}			0.7 × V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}			V_{SS}	—	0.3 × V_{DD}	V
High level input current	I_{IH}	V_{DD} = 5.0 V, V_{IH} = 5.0 V, Ta = 25°C	BEN	—	—	35	μA
				—	—	0.5	μA
Low level input current	I_{IL}	V_{DD} = 5.0 V, V_{IL} = 0 V, Ta = 25°C	$\overline{AEN}$	-35	—	—	μA
				-0.5	—	—	μA
High level output voltage	V_{OH}	SO terminal, no load		4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load		—	—	0.05	V
High level output current	I_{OH}	SO terminal, V_{OH} = V_{DD}-0.4 V		—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, V_{OL} = 0.4 V		0.5	—	—	mA
High level driver output voltage	V_{DOH}			—	24	26	V
Low level driver output voltage	V_{DOL}	I_{DOL} = 9 mA, V_{DD} = 5.0 V		—	0.7	1.5	V
Driver leakage current	I_{LEAK}	V_{DOH} = 26 V, Per 1-bit of driver output		—	—	1.0	μA
Current consumption	I_{DD}	Ta = 25°C	f_{CLK} = 2 MHz, SI : fixed	—	0.2	0.6	mA
			f_{CLK} = 5 MHz, SI : fixed	—	0.4	1.2	mA
			f_{CLK} = 5 MHz, SI = 1/2f_{CLK}	—	1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}			2.0	—	4.0	V

■ AC Electrical Characteristics

Table 4

(V_{DD} = 5.0 V ± 10%, Ta = -10°C to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	V_{IH} = V_{DD}, V_{IL} = V_{SS0}	40	—	—	ns
Data hold time	t_{HD}	V_{IH} = V_{DD}, V_{IL} = V_{SS0}	40	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	C_L = 3 pF	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L = 3.0 kΩ, V_{DOH} = 24 V	—	—	3.0	μs
DOn rise time	t_{rDO}	R_L = 3.0 kΩ, V_{DOH} = 24 V	—	1.0	3.0	μs
DOn fall time	t_{fDO}	R_L = 3.0 kΩ, V_{DOH} = 24 V	—	1.0	3.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

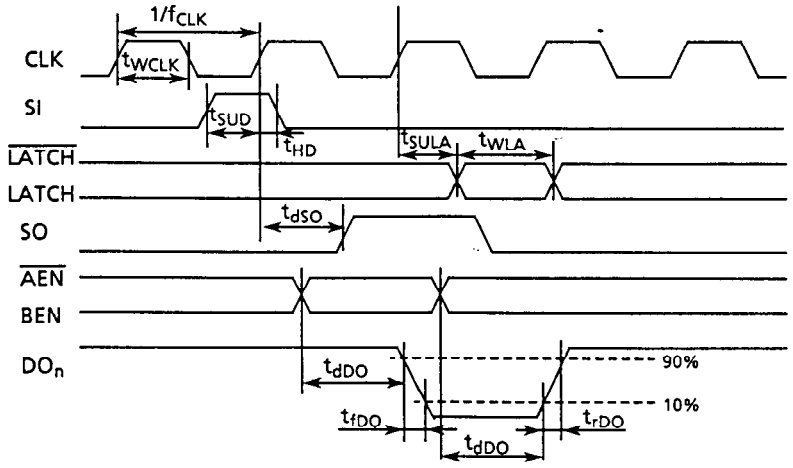
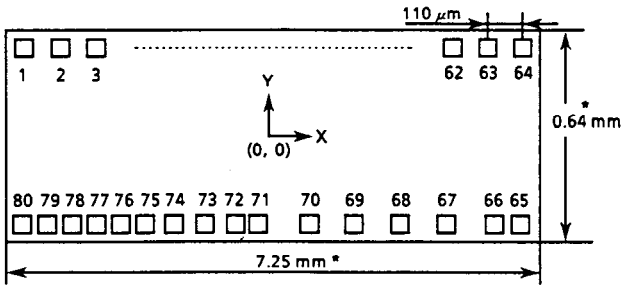


Figure 2

■ Dimensions



Pad size : 80 μm × 80 μm
(passivation opening)
Pad pitch :
110 μm (driver output pad)
Chip thickness : 350 ± 30 μm

*Before dicing

Figure 3

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5

Unit : μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO_1	-3465	210	28	DO_{28}	-495	210	55	DO_{55}	2475	210
2	DO_2	-3355	210	29	DO_{29}	-385	210	56	DO_{56}	2585	210
3	DO_3	-3245	210	30	DO_{30}	-275	210	57	DO_{57}	2695	210
4	DO_4	-3135	210	31	DO_{31}	-165	210	58	DO_{58}	2805	210
5	DO_5	-3025	210	32	DO_{32}	-55	210	59	DO_{59}	2915	210
6	DO_6	-2915	210	33	DO_{33}	55	210	60	DO_{60}	3025	210
7	DO_7	-2805	210	34	DO_{34}	165	210	61	DO_{61}	3135	210
8	DO_8	-2695	210	35	DO_{35}	275	210	62	DO_{62}	3245	210
9	DO_9	-2585	210	36	DO_{36}	385	210	63	DO_{63}	3355	210
10	DO_{10}	-2475	210	37	DO_{37}	495	210	64	DO_{64}	3465	210
11	DO_{11}	-2365	210	38	DO_{38}	605	210	65	V_{SS1}	3466	-210
12	DO_{12}	-2255	210	39	DO_{39}	715	210	66	V_{SS1}	3286	-210
13	DO_{13}	-2145	210	40	DO_{40}	825	210	67	SO	2870	-210
14	DO_{14}	-2035	210	41	$DO4_1$	935	210	68	V_{DD}	1696	-210
15	DO_{15}	-1925	210	42	DO_{42}	1045	210	69	BEN	1160	-210
16	DO_{16}	-1815	210	43	DO_{43}	1155	210	70	V_{SS0}	580	-210
17	DO_{17}	-1705	210	44	DO_{44}	1265	210	71	V_{SS1}	130	-210
18	DO_{18}	-1595	210	45	DO_{45}	1375	210	72	V_{SS1}	-50	-210
19	DO_{19}	-1485	210	46	DO_{46}	1485	210	73	V_{SS0}	-500	-210
20	DO_{20}	-1375	210	47	DO_{47}	1595	210	74	$\overline{AEN}$	-1000	-210
21	DO_{21}	-1265	210	48	DO_{48}	1705	210	75	V_{DD}	-1500	-210
22	DO_{22}	-1155	210	49	DO_{49}	1815	210	76	CLK	-2000	-210
23	DO_{23}	-1045	210	50	DO_{50}	1925	210	77	$\overline{LATCH}$	-2500	-210
24	DO_{24}	-935	210	51	DO_{51}	2035	210	78	SI	-3016	-210
25	DO_{25}	-825	210	52	DO_{52}	2145	210	79	V_{SS1}	-3286	-210
26	DO_{26}	-715	210	53	DO_{53}	2255	210	80	V_{SS1}	-3466	-210
27	DO_{27}	-605	210	54	DO_{54}	2365	210				