64-bit THERMAL HEAD DRIVER

S-4640A

The S-4640A is a CMOS thermal print head driver with a 64-bit shift register and a latch. The 100 μm driver output pad pitch allows for high density mounting up to 200 dpi or 8 dots/mm.

■ Features

- Low current consumption : 0.5 mA typ. (f_{CLK} = 4 MHz, SI: stabilized)
- High speed operation : 7 MHz (single) 5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current: 8 mA typ.
- A 64-bit shift register and a latch are built in
- Driver enable
- Driver-off function when supply voltage falls

■ Block Diagram

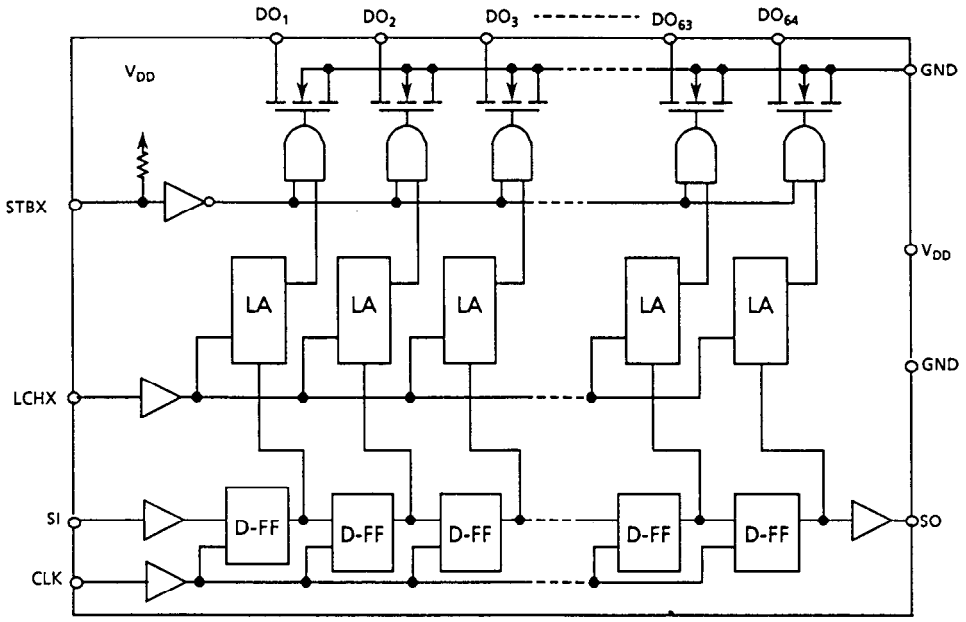


Figure 1

■ Operation

The 64-bit shift register reads the data input to the SI pin at the rising edge of the CLOCK input. The latch circuit reads the data of the shift register when it is "L", and it holds the preceding data when it is "H". The latch data are output to the respective drivers when STBX is low. The driver output transistor turns on when the latch data is high and turns off when low. Turning STBX to high makes all driver output transistors go off. All driver output transistors go off when the power supply voltage goes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1	CLK	Clock input terminal for 64-bit shift register
2	LCHX	Data latch signal input terminal LCHX = "L": Reads the data of the shift register LCHX = "H": Holds the preceding data
3, 4, 5	GND	GND (0 V)
6	VDD	Positive power supply for logic (+5 V)
7	STBX	Driver strobe input terminal: Outputs the latch data to the driver when "low". (Pull-up register R_P = 300KΩ TYP built in)
8	SO	Serial data output terminal for 64-bit shift register
9 to 72	DO1 to DO64	Driver output terminals (Nch open-drain)
73	SI	Serial data input terminal for 64-bit shift register

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	GND to V_{DD}	-0.4 to 7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	17 *1	mA
Input voltage	VIN	GND-0.5 to V_{DD} + 0.5	V
Output voltage	VOUT	GND-0.5 to V_{DD} + 0.5	V
Max. junction temperature	Tjmax	125	°C
Operating temperature	Topr	-10 to +80	°C
Storage temperature	Tstg	-40 to +125	°C

*1 When only 1 bit output terminal is "ON".
When 64 bit output terminals are all "ON": Print duty ratio < 50%, $I_{DOL} \leq 8$ mA
Print duty ratio < 25%, $I_{DOL} \leq 12$ mA

■ DC Electrical Characteristics

Table 3

(V_{DD} = 5.0 V ± 10%, Ta = -10 to 80 °C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High level driver output voltage	V_{DOH}				26	V
High level input voltage	V_{IH}	CLK: f_{CLK} = fmax duty 50% $T_{SUD} = T_{HD}$ = 100 nsec SI: f_{SI} = 1/2 fmax LCHX: T_{WLA} = 100 nsec STBX: DC level	0.7V_{DD}		V_{DD}	V
Low level input voltage	V_{IL}		GND		0.3V_{DD}	V
High level input current	I_{IH}	$V_{IH} = V_{DD}$			0.5	μA
Low level input current	I_{IL}	*STBX terminal V_{IL} = GND	−55	−17		μA
		Except STBX terminal V_{IL} = GND	−0.5			μA
High level output voltage	V_{OH}	SO terminal I_{OH} = −0.5 mA	4.1			V
Low level output voltage	V_{OL}	SO terminal I_{OL} = 0.5 mA			0.4	V
Low level driver output voltage	V_{DOL}	V_{DD} = 5.0 V, I_{DOL} = 8 mA		0.7	1.2	V
Driver leakage current	I_{LEAK}	V_{DOH} = 26 V			1.0	μA
Current consumption	I_{DD}	f_{CLK} = 4 MHz SI: stabilized		0.5	1.5	mA
		f_{CLK} = 4 MHz SI: HLHL		1.5	4.5	mA
Static current	I_S	SI, CLK, LCHX = GND Other terminalS = OPEN		0.1	0.3	mA
Falling supply voltage detection voltage	V_{DET}		0.8		4.0	V

* Pull-up resistor is built in

■ AC Electrical Characteristics

Table 4

(V_{DD} = 5.0 V ± 10%, Ta = -10° C to 80 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}	$V_{IH} = V_{DD}$ V_{IL} = 0V Rising, Falling Under 15nsec Output load RL = 1 MΩ CL = 10 pF	70	—	—	ns
Data setup time	t_{SUD}		40	—	—	ns
Data hold time	t_{HD}		40	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}		—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L = 3.0 kΩ, V_{DOH} = 24 V	—	—	4.3	μs
DOn rise time	t_{rDO}	R_L = 3.0 kΩ, V_{DOH} = 24 V	—	1.0	3.0	μs
DOn fall time	t_{fDO}	R_L = 3.0 kΩ, V_{DOH} = 24 V	—	1.0	3.3	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

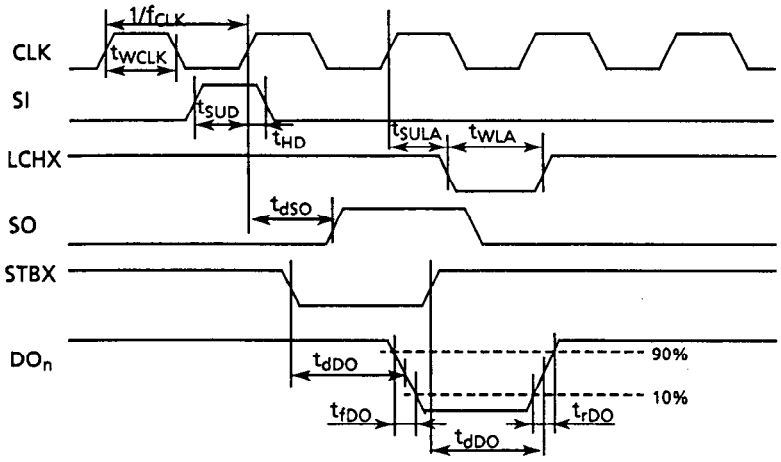
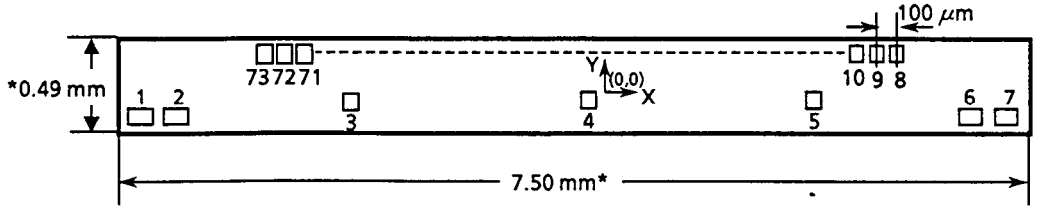


Figure 2

■ Dimensions



Pad size: 80 μm x 76 μm (passivation opening) No.8 to 73
76 μm x 76 μm (passivation opening) No.3 to 5
120 μm x 76 μm (passivation opening) No.1, 2, 6, 7
Pad pitch: 100 μm (driver output pad)
Chip thickness: 350 ± 30 μm
*Before dicing

Figure 3

■ **Pad Coordinates** (The origin (0, 0) is the center of the chip)

Table 5

Unit: μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	CLK	-3595.0	-147.5	26	DO47	1462.0	152.5	51	DO22	-1038.0	152.5
2	LCHX	-3433.0	-147.5	27	DO46	1362.0	152.5	52	DO21	-1138.0	152.5
3	GND	-2202.5	-77.0	28	DO45	1262.0	152.5	53	DO20	-1238.0	152.5
4	GND	-57.5	-77.0	29	DO44	1162.0	152.5	54	DO19	-1338.0	152.5
5	GND	2099.0	-77.0	30	DO43	1062.0	152.5	55	DO18	-1438.0	152.5
6	VDD	3400.0	-147.5	31	DO42	962.0	152.5	56	DO17	-1538.0	152.5
7	STBX	3562.0	-147.5	32	DO41	862.0	152.5	57	DO16	-1638.0	152.5
8	SO	3262.0	152.5	33	DO40	762.0	152.5	58	DO15	-1738.0	152.5
9	DO64	3162.0	152.5	34	DO39	662.0	152.5	59	DO14	-1838.0	152.5
10	DO63	3062.0	152.5	35	DO38	562.0	152.5	60	DO13	-1938.0	152.5
11	DO62	2962.0	152.5	36	DO37	462.0	152.5	61	DO12	-2038.0	152.5
12	DO61	2862.0	152.5	37	DO36	362.0	152.5	62	DO11	-2138.0	152.5
13	DO60	2762.0	152.5	38	DO35	262.0	152.5	63	DO10	-2238.0	152.5
14	DO59	2662.0	152.5	39	DO34	162.0	152.5	64	DO9	-2338.0	152.5
15	DO58	2562.0	152.5	40	DO33	62.0	152.5	65	DO8	-2438.0	152.5
16	DO57	2462.0	152.5	41	DO32	-38.0	152.5	66	DO7	-2538.0	152.5
17	DO56	2362.0	152.5	42	DO31	-138.0	152.5	67	DO6	-2638.0	152.5
18	DO55	2262.0	152.5	43	DO30	-238.0	152.5	68	DO5	-2738.0	152.5
19	DO54	2162.0	152.5	44	DO29	-338.0	152.5	69	DO4	-2838.0	152.5
20	DO53	2062.0	152.5	45	DO28	-438.0	152.5	70	DO3	-2938.0	152.5
21	DO52	1962.0	152.5	46	DO27	-538.0	152.5	71	DO2	-3038.0	152.5
22	DO51	1862.0	152.5	47	DO26	-638.0	152.5	72	DO1	-3138.0	152.5
23	DO50	1762.0	152.5	48	DO25	-738.0	152.5	73	SI	-3238.0	152.5
24	DO49	1662.0	152.5	49	DO24	-838.0	152.5				
25	DO48	1562.0	152.5	50	DO23	-938.0	152.5				