AN.No.G482C-870E

LIQUID CRYSTAL DISPLAY MODULE

G 4 8 2 C

USER MANUAL

Seiko Instruments Inc.

NOTICE

This manual describes the technical information, the function, and the operation of the G482C Liquid Crystal Display Module of Seiko Instruments Inc. Please read this manual carefully to familialize yourself with the functions and to make best use of them.
The descriptions here are subject to change without notice.

Revision Record

Edition	Revision	Date
1	Original	July 1988

Printed in Japan

CONTENTS

1. SPECIFICATIONS

1.1 General

The G482C is a thin liquid crystal display (LCD) module that consists of a full dot-matrix LCD panel and CMOS LSIs. The panel features a wide viewing angle and high contrast. The full dot-matrix structure allows both graphics and character display. In addition, the display is clear and stable, with no image warping or position skew, because the display position is specified by the intersection of transparent electrodes in a matrix.

1.2 Features

- Full dot-matrix structure with 480 dots×128 dots
- 1 / 128 duty
- One-bit serial data × 2 (right-half and left-half) input
- Two power supplies : V_{DD}= 5 V, V_{LC}= -13 V (for driving liquid crystal)

1.3 Absolute Maximum Ratings

Vss = 0 V

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply voltage	V_{DD}		− 0.3	6.0	V
	V_{LC}		V_{DD} − 19.0	V_{DD} + 0.3	V
	V_O	$V_O \geqq V_{LC}$	V_{DD} − 19.0	V_{DD} + 0.3	V
Input voltage	V_{IN}		− 0.3	V_{DD} + 0.3	V
Operating temperature	T_{opr}		0	+ 50	°C
Storage temperature	T_{stg}		− 20	+ 60	°C

1.4 Electrical Characteristics

Vss = 0 V, Ta = 0°C ~ 50°C

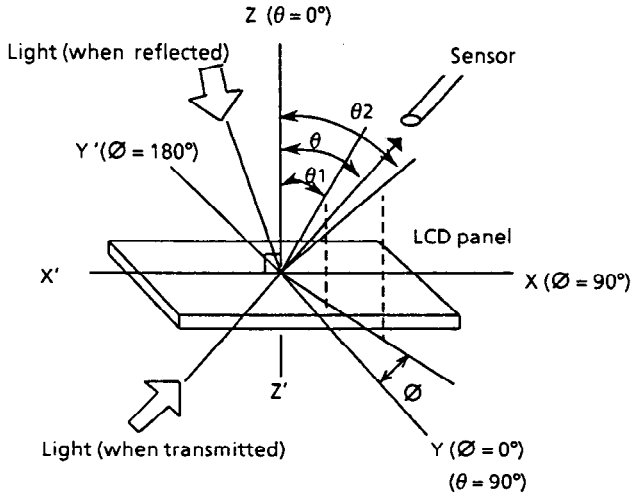
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	V_{DD} = 5 V ± 5%	− 13.5	− 13.0	− 12.5	V
		V_O	V_{DD} = 5 V ± 5% $V_O \geqq V_{LC}$	—	—	− 3.0	V
Input voltage	High	V_{IH}	V_{DD} = 5 V ± 5%	0.7 V_{DD}	—	V_{DD}	V
	Low	V_{IL}	V_{DD} = 5 V ± 5%	0	—	0.3 V_{DD}	V
Current consumption		I_{DD}	V_{DD} = 5.0 V V_{LC} = − 13.0 V V_O = − 11.2 V	—	11	16	mA
		I_{LC}		—	7.5	11	mA
Frame frequency		f_{FRM}	V_{DD} = 5 V ± 5%	65	70	75	Hz

1.5 Optical Characteristics (Measured with Yellow-green Type Module)

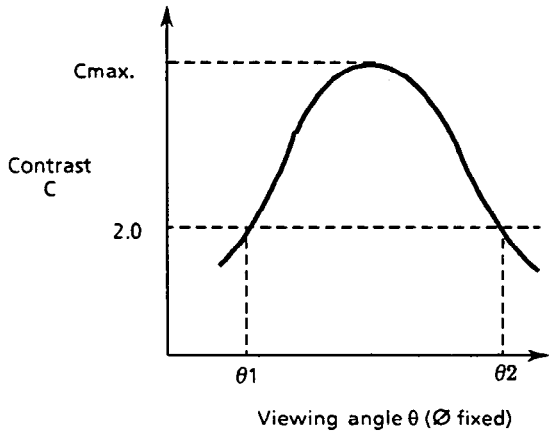
1 / 128 duty, 1 / 9 bias, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	C ≧ 2.0, Ø = 0°	50°	–	–	Notes 1 & 2
Contrast	C	θ = 15°, Ø = 0°	4	5	–	Note 3
Response time (rise)	t_{on}	θ = 15°, Ø = 0°	–	130 ms	–	Note 4
Response time (fall)	t_{off}	θ = 15°, Ø = 0°	–	330 ms	–	Note 4

Note 1 : Definition of angles θ and Ø



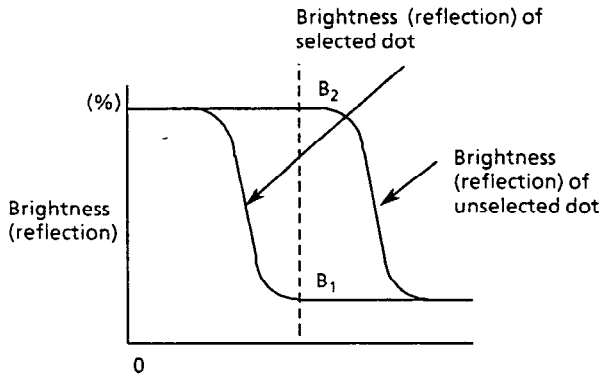
Note 2 : Definition of viewing angles $\theta 1$ and $\theta 2$



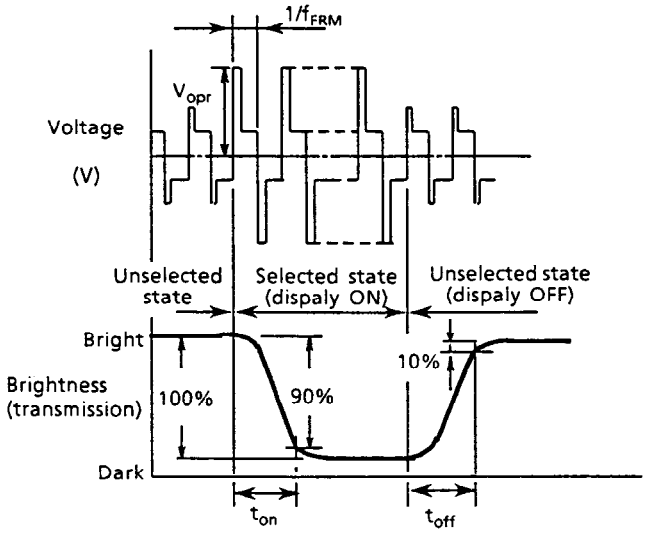
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. above are not always the same.

Note 3 : Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot } (B_2)}{\text{Brightness (reflection) of selected dot } (B_1)}$$



Note 4 : Definition of response time



Note : Measured with a transmissive LCD panel which is displayed 1 cm²

V_{opr} : Operating voltage f_{FRM} : Frame frequency
t_{on} : Response time (rise) t_{off} : Response time (fall)

1.6 Dimensions

Unit : mm/inch
General tolerance : ± 0.5 mm

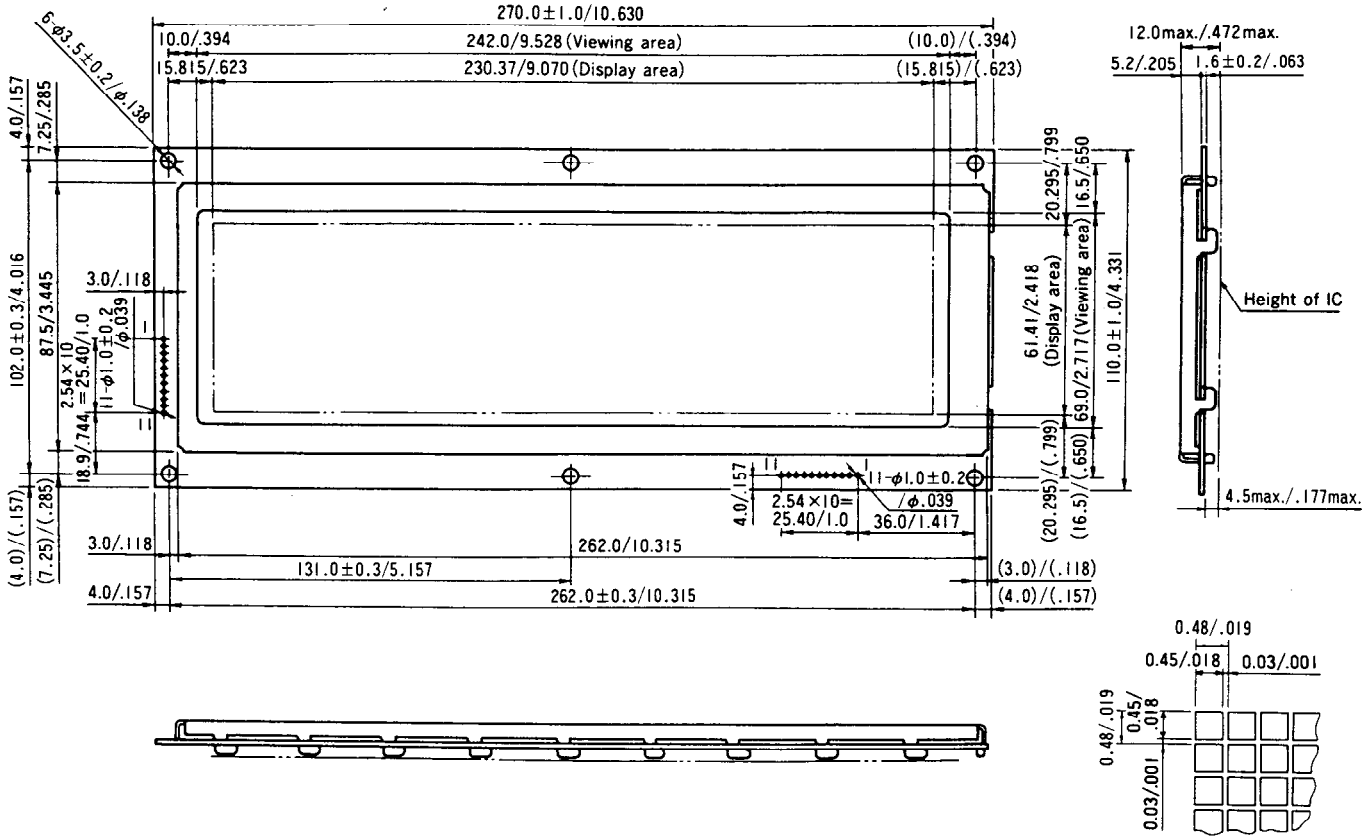


Figure 1 Dimensions

[I/O Terminal Functions]

No	Symbol	Function
1	D_1	Left-half screen display data input
2	D_2	Right-half screen display data input
3	FLM	One-frame timing signal
4	M	Liquid crystal drive waveform AC signal
5	CL1	One-common-line timing signal

No	Symbol	Function
6	CL2	Display data shift clock
7	V_{DD}	Power supply voltage (1) : + 5 V
8	V_{SS}	GND : 0 V
9	V_{LC}	Power supply voltage (2) : − 13 V
10	V_O	Liquid crystal drive voltage adjustment terminal
11	F_{GND}	Frame ground*

* The F_{GND} terminal is connected to the metal frame of the module. Use this terminal to ground the frame.

2. CIRCUIT STRUCTURE

2.1 Liquid Crystal Driving Circuit

The drive waveform of the LCD panel is shown in Figure 2 on the next page. Since DC may damage the liquid crystal, the drive waveform polarity is reversed at alternate frames, and AC is applied between two frames. The signal controlling this is the liquid crystal drive waveform AC signal (M). The frame frequency is normally set to about 70±5 Hz to prevent screen flicker.

The G482C has a 1/128 duty cycle, and the common electrodes are selected within a frame by time division from electrode 1 to electrode 128. This is called line sequential scanning. The voltage level of the segment electrodes determines whether the dots at the intersection of the segment electrodes are selected or not, when the common electrode is selected. As shown in Table 1, there are six drive waveform voltage levels, V_a to V_f. The voltage level is determined by the bias value. The voltage between the segment and common electrodes is thus applied to the liquid crystal. The selection waveform for SEG_0-COM_0 and the non-selection waveform for SEG_1-COM_1 are shown in Figure 2. The size of the effective voltage of the waveform determines whether the liquid crystal under the selected dots is in the selection or non-selection state.

Table 1

V_a	Common and segment selection level
V_b	Common non-selection level
V_c	Segment non-selection level
V_d	Segment non-selection level
V_e	Common non-selection level
V_f	Common and segment selection level

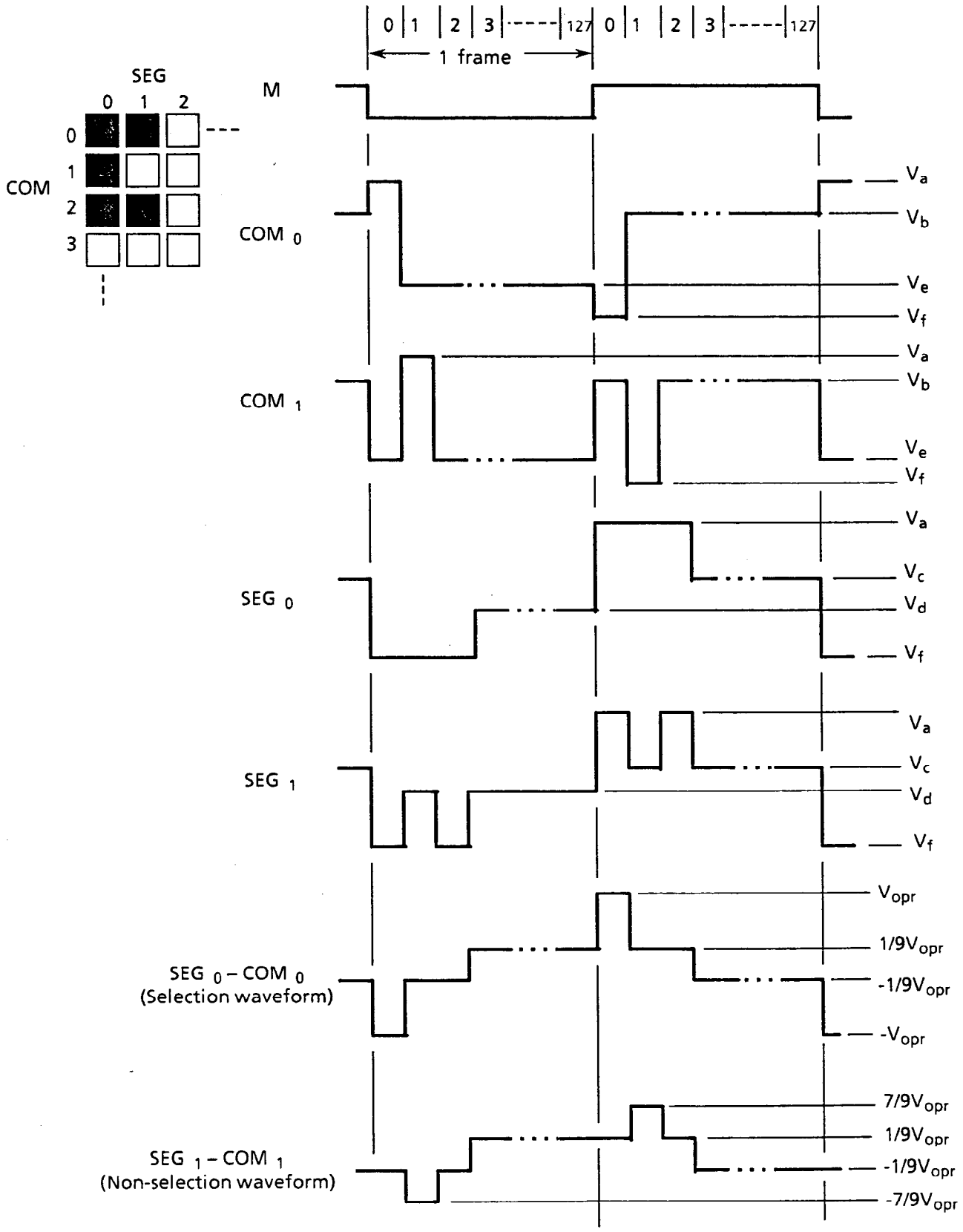


Figure 2 Drive waveform

2.2 Circuit Structure

The G482C consists of common drivers, segment drivers, a bias voltage generation circuit and a V_{opr} control circuit. Figure 3 shows the block diagram.

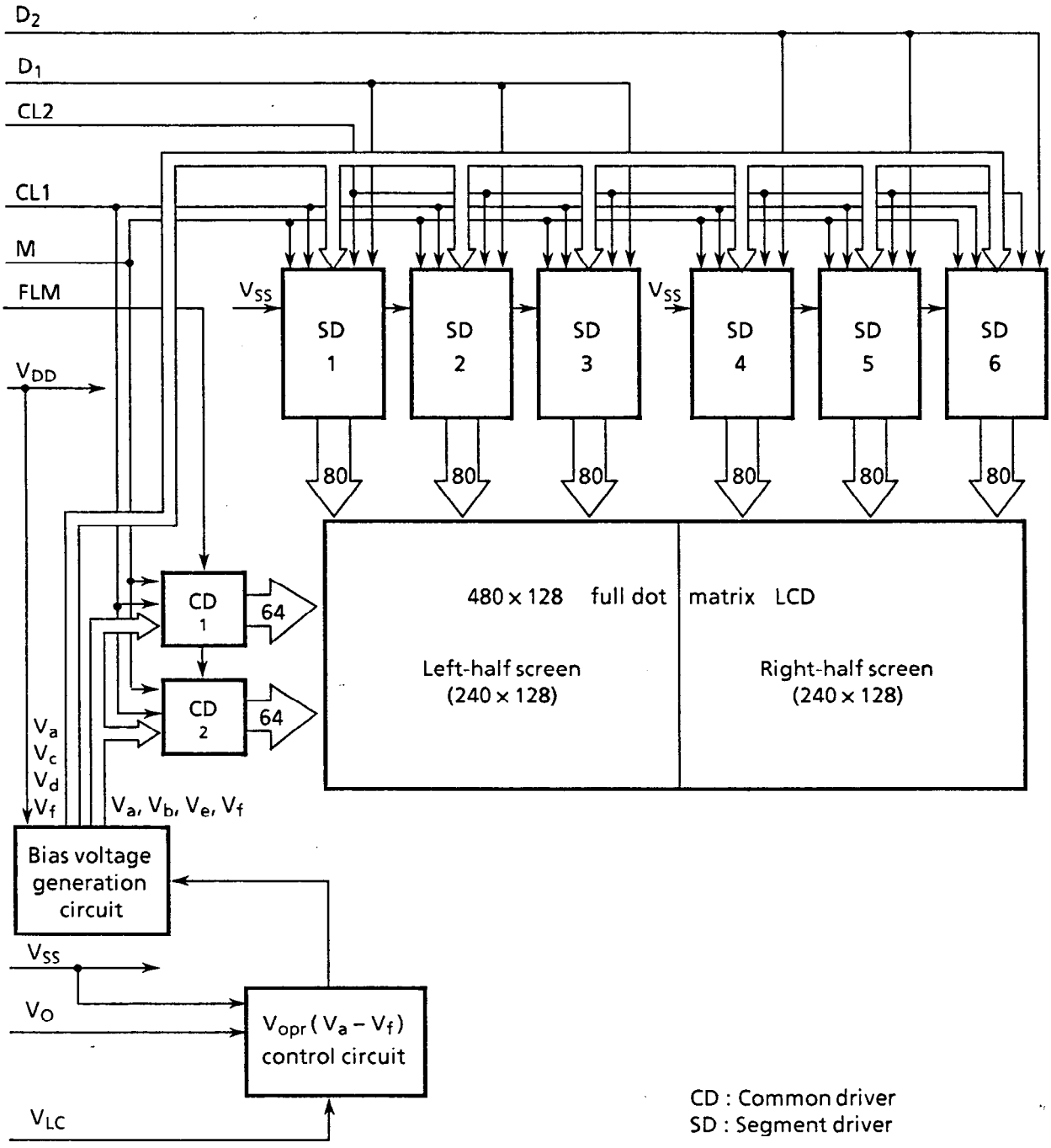


Figure 3 Block diagram

(1) Common driver

A common driver (CD) is a CMOS IC with 64 drive outputs. The G482C has two CDs, whose internal registers are connected each other. They operate as follows. Input one-frame timing signal (FLM) is taken into the internal shift register by the falling edge trigger of the one-common-line timing signal (CL1), and sequentially shifted. After 128-CL1 input, the next FLM is input and the same operation is repeated. As shown in Table 2, the common output is selected according to the shift register contents and the liquid crystal drive waveform AC signal (M) in the drive circuit, and the common drive waveform is formed.

Table 2

Shift register content	M	COM output
H	H	V_f
	L	V_a
L	H	V_b
	L	V_e

(2) Segment driver

A segment driver (SD) is a CMOS IC with 80 drive outputs. It operates as follows. Input four-bit data is sequentially taken into the internal register by the falling edge trigger of the display data shift clock (CL2). The G482C has six SDs. SD1 to SD3 are for left-half screen and SD4 to SD6 are for right-half screen. SD has a chip enable function. In the case of left-half screen, after 80 bits of data are taken into SD1, the next data is automatically taken into SD2. 240 bits of data can be taken into three SDs. Data for right-half screen is taken into in the same way as data for left-half screen. The display data taken into internal register are latched by the falling edge trigger of CL1. As shown in the Table 3, the segment output is selected according to the display data and M in the drive circuit, and the segment drive waveform is formed.

Table 3

Display data	M	SEG output
H	H	V_a
	L	V_f
L	H	V_c
	L	V_d

(3) V_{opr} control circuit

Display screen contrast and viewing angle are affected by changes in the liquid crystal driving voltage (V_{opr}). As shown in Figure 4, external V_{LC} is supplied to the operational amplifier and V_{opr} (V_a to V_f) applied to the LCD panel is generated.

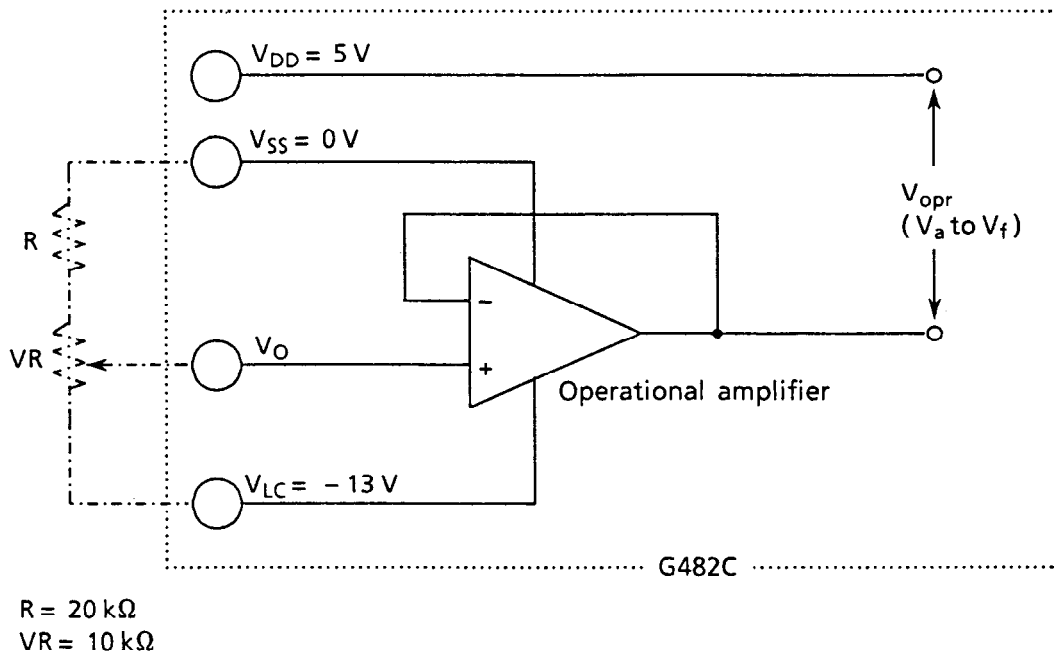


Figure 4

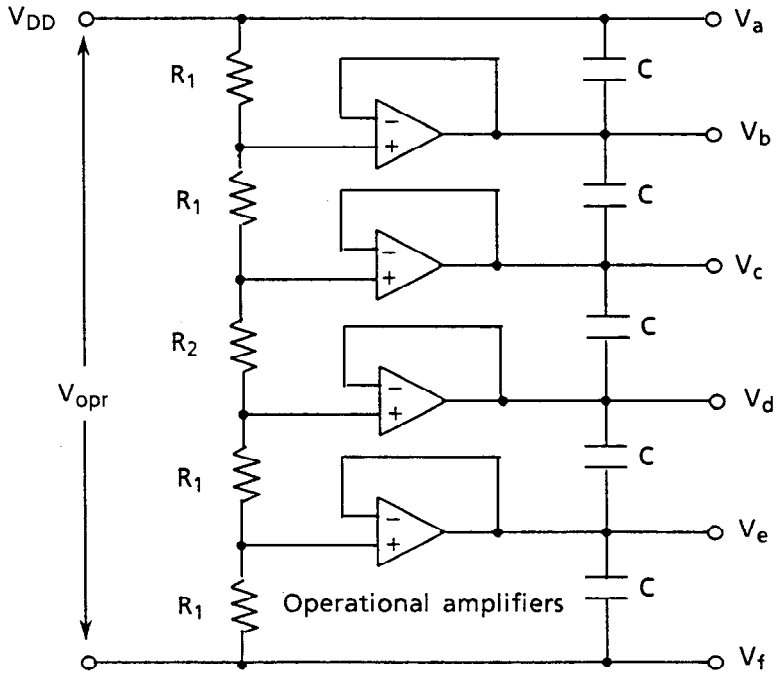
Also, display screen contrast and viewing angle are influenced by the ambient temperature. The recommended V_{opr} level at different temperatures is as follows.

Temperature (°C)	0	25	50
V_{opr} (V)	17.0	16.2	14.5

$V_{opr} \approx V_{DD} - V_O$

(4) Bias voltage generation circuit

Six levels of voltage, V_a to V_f, are applied to the common and segment drivers. The voltage is generated through operational amplifier by resistance-division from liquid crystal operating voltage (V_{opr}). Here, an operational amplifier is used as a voltage follower.



1/9 bias : $R_2 = (9-4)R_1 = 5R_1$

Figure 5 Bias voltage generation circuit

2.3 Timing Characteristics

Ta = 0°C ~ 50°C V_{DD} = 5.0 V ± 5%

Item	Symbol	Min.	Max.	Unit
CL1 high pulse width	twcl1h	150	—	ns
CL1 low pulse width	twcl1l	450	—	ns
Data setup time 1	tds1	100	—	ns
Data hold time 1	tdh1	100	—	ns
Allowable M delay time	tdm	− 2000	300	ns
Input signal rise time	t_r	—	30	ns
Input signal fall time	t_f	—	30	ns
CL2 period	tccl2	400	—	ns
CL2 high pulse width	twcl2h	150	—	ns
CL2 low pulse width	twcl2l	150	—	ns
Data setup time 2	tds2	80	—	ns
Data hold time 2	tdh2	100	—	ns
CL2 rise to CL1 rise	tld	100	—	ns
CL2 fall to CL1 fall	tsl	100	—	ns
CL1 fall to CL2 fall	tlh	100	—	ns

Timing chart 1 Timing of signal input into common driver

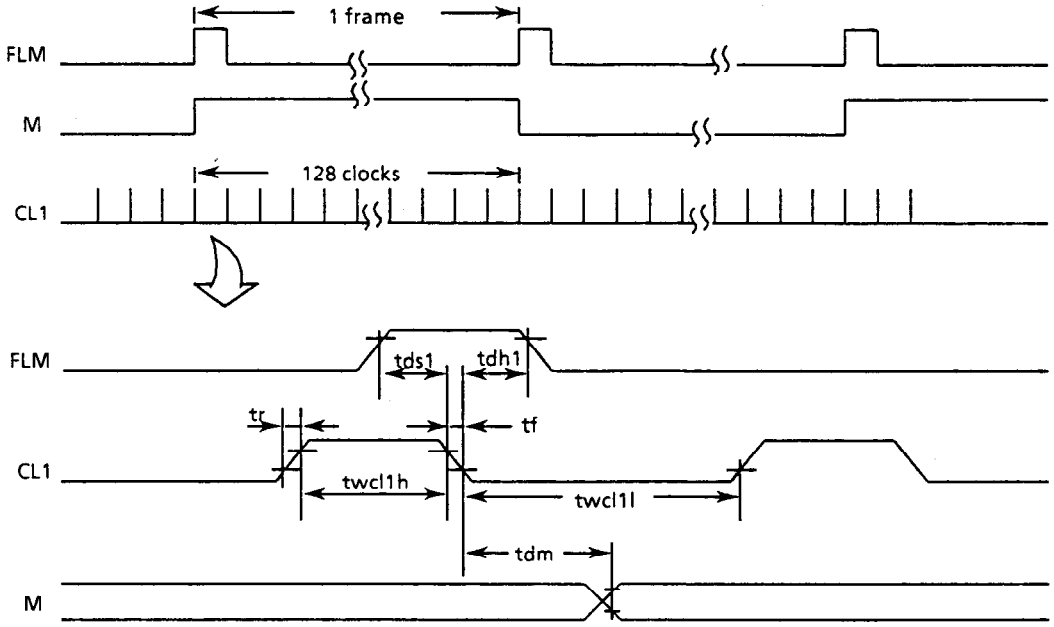


Figure 6

Timing chart 2 Timing of signal input into segment driver

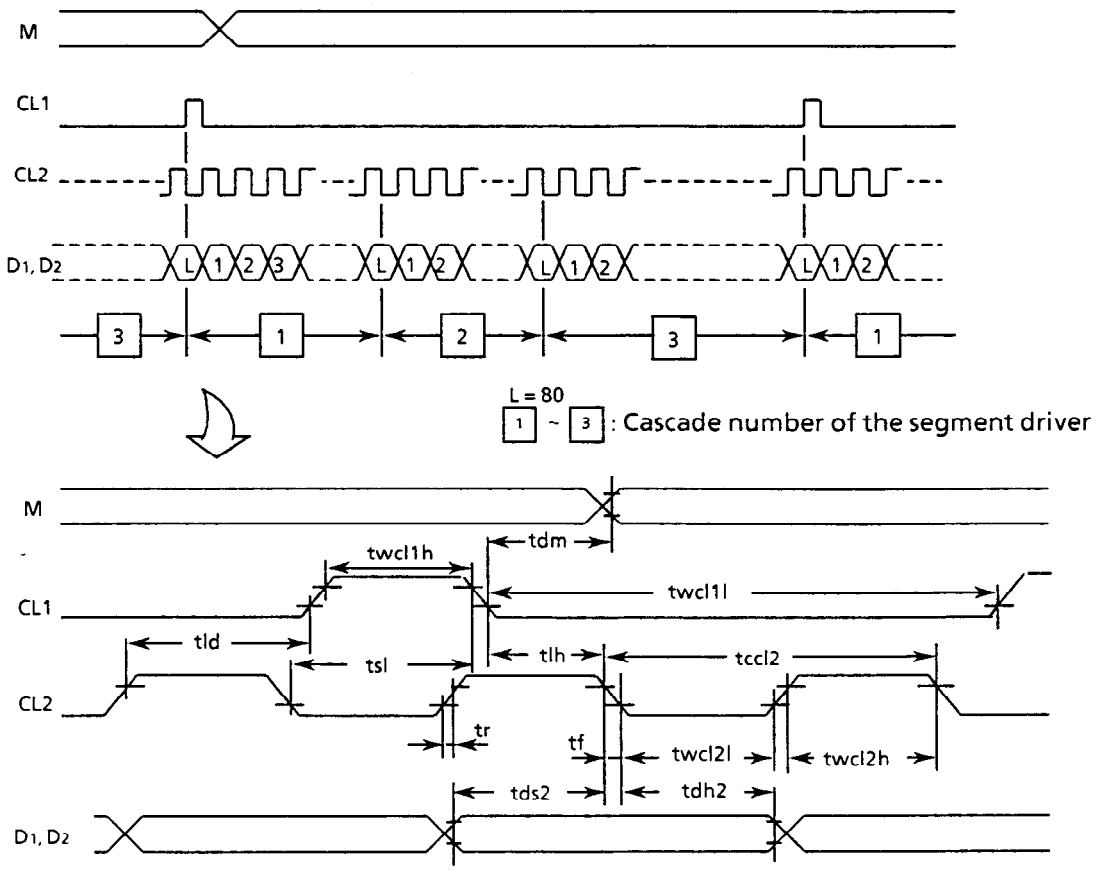


Figure 7

2.4 Interface Circuit

The G482C is controlled by the MPU circuit, whose interface is easily set up when the LCD controller is used. The LCD controller has basic functions such as receiving information related to the display from the MPU circuit, and sending display timing signals and display data to the LCD module, and other functions such as cursor display.

The G482C must use LCD controllers conforming to the following conditions.

- For a full dot-matrix LCD module
- Where data is transferred to the LCD module in 2 one-bit serials
- Where G482C display screen has 1/128 duty

The following section gives examples of interfaces using the OKI MSM6255GSK and HITACHI HD61830B controllers.

(1) OKI MSM6255GSK

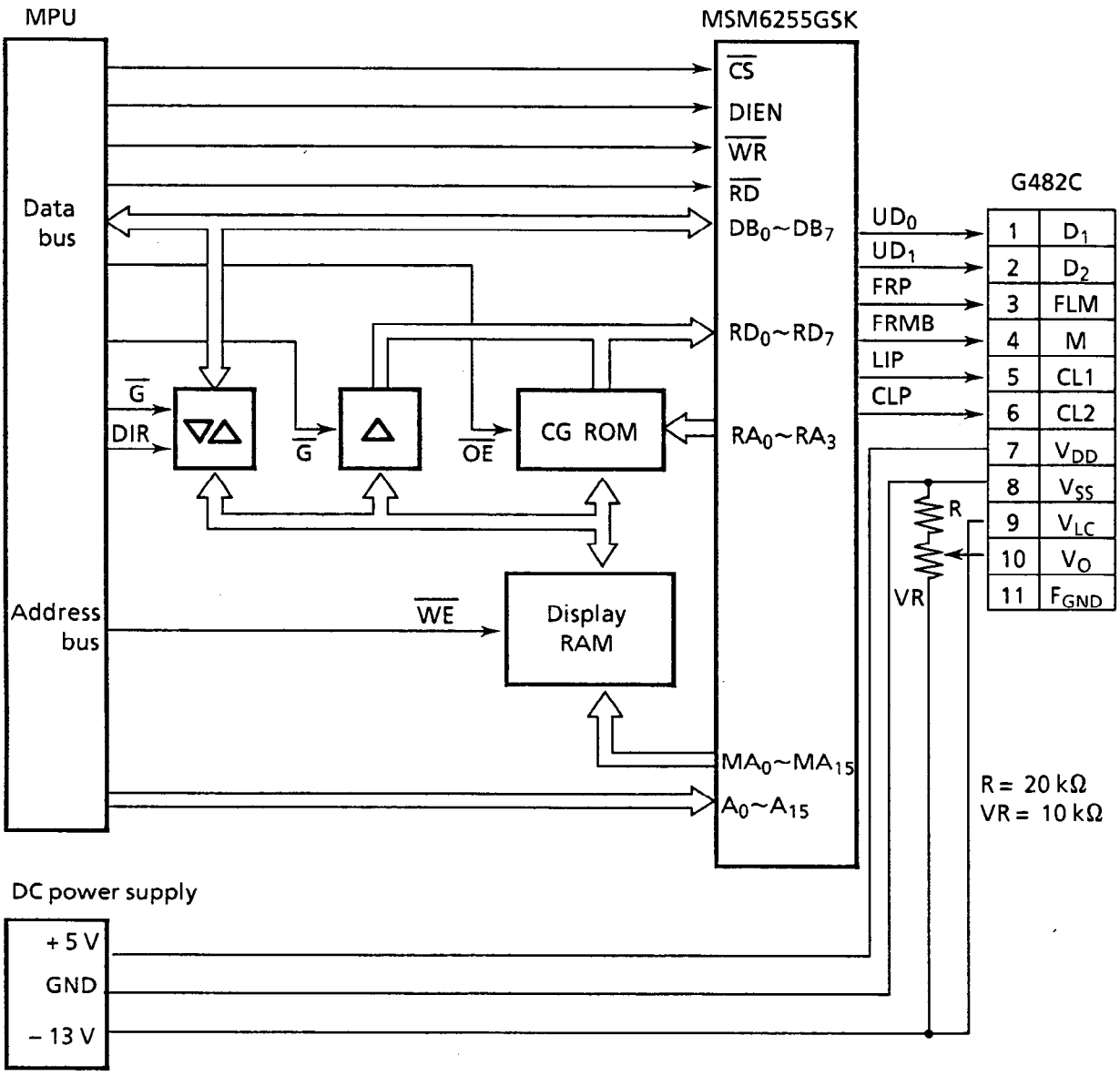


Figure 8 Interface circuit with MSM6255GSK

[Features of the MSM6255GSK]

- Interface with 80-series MPU possible
- Cursor
  - ON/OFF/Blink; blinking speed, form, and position are programmable
- Scrolling and paging
- CMOS process
- 5-V single power supply

(2) HITACHI HD61830B

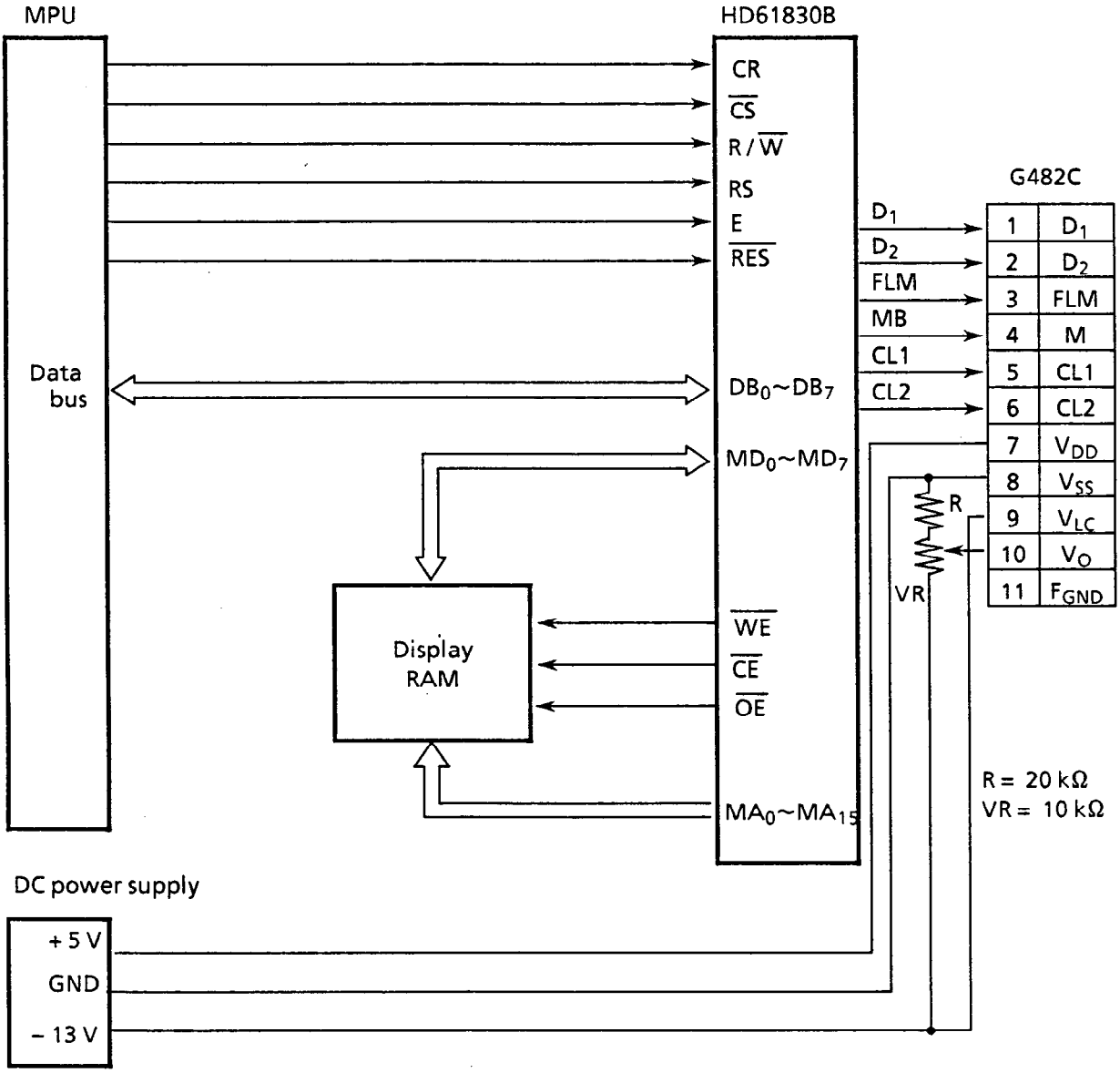


Figure 9 Interface circuit with HD61830B

[Features of the HD61830B]

- Interface with eight-bit MPU possible
- Built-in character generator ROM : 7360 bits
  - Character font : 192 kinds
    (5×7 dot-matrix) ×160 kinds
    (5×11 dot-matrix) ×32 kinds
  - External ROM : can be extended to 4KB
- Scrolling
- Cursor
  ON/OFF/Blink
- Character Blink
- Bit manipulation
- CMOS process
- 5-V single power supply

3. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

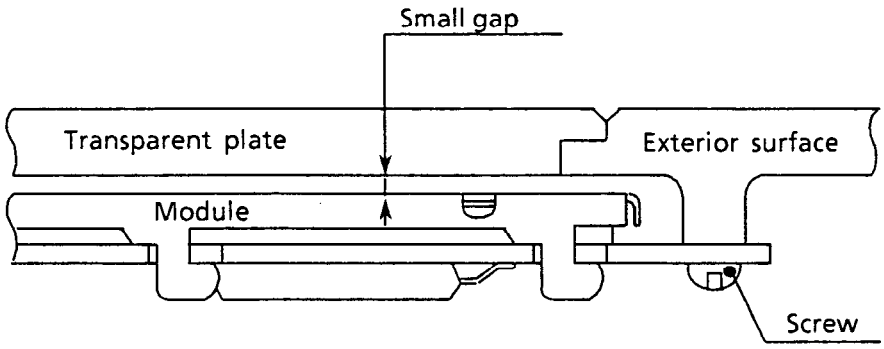
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is made of plate glass; do not hit or press aginst it.
- Do not remove the panel or frame from the module.
- The polarizer on the display is very fragile; handle it very carefully.

Mounting and Design

- Mount the module in the specified installation sections and holes.
- To protect the module from external pressure, put a plate of transparent material such as acrylic or glass over the display surface, frame, and polarizer. Leave a small gap between the transparent plate and the module.

☆Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Condensation can damage the transparent electrodes .

Storage

- Store the module in a dark place where the temperature is 25°C ±10°C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module or its components.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizer.

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