Si5022/Si5023

PRELIMINARY DATA SHEET

MULTI-RATE SONET/SDH CDR IC WITH LIMITING AMP

Features

High Speed Clock and Data Recovery device with Integrated Limiting Amp:

- Supports OC-48/12/3, STM-16/4/1, Gigabit Ethernet, and 2.7 Gbps FEC
- DSPLL™ Technology
- Low Power—370 mW (TYP)
- Small Footprint: 5 mm x 5 mm
- Bit-Error-Rate Alarm
- External Reference Not Required
- Jitter Generation 3.0 mUI_{RMS}(TYP)
- Loss-of-signal Level Alarm
- Data Slicing Level Control
- 10 mV_{PP} Differential Sensitivity
- 2.5 V (Si5022) or 3.3 V (Si5023) Supply

Ordering Information:

See page 14.

Applications

- SONET/SDH/ATM Routers
- Add/Drop Multiplexers
- Digital Cross Connects
- Gigabit Ethernet Interfaces
- SONET/SDH Test Equipment
- Optical Transceiver Modules
- SONET/SDH Regenerators
- Board Level Serial Links

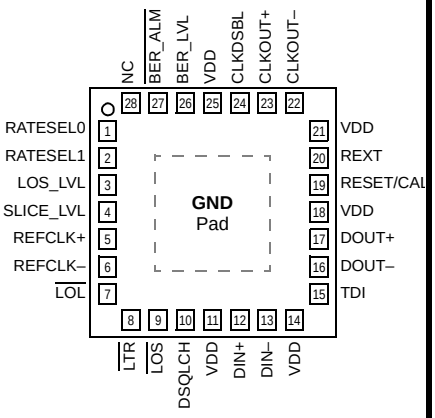
Description

The Si5022/23 is a fully integrated, high performance limiting amp and clock and data recovery (CDR) IC for high-speed serial communication systems. It extracts timing information and data from a serial input at OC-48/12/3, STM-16/4/1, or Gigabit Ethernet (GbE) rates. Support for 2.7 Gbps data streams is also provided for OC-48/STM-16 applications that employ forward error correction (FEC). An external reference clock is not required; applications with or without an external reference clock are supported. Silicon Laboratories' DSPLL™ technology eliminates sensitive noise entry points thus making the PLL less susceptible to board-level interaction and helping to ensure optimal jitter performance.

The Si5022/23 represents a new standard in low jitter, low power, small size, and integration for high speed LA/CDRs. It operates from either a 3.3 V (Si5023) or 2.5 V (Si5022) supply over the industrial temperature range (–40°C to 85°C).

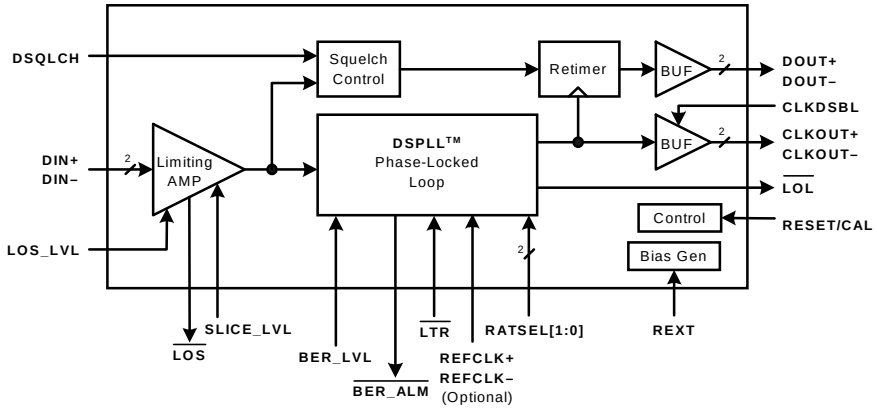
Pin Assignments

Si5022/23



Top View

Functional Block Diagram



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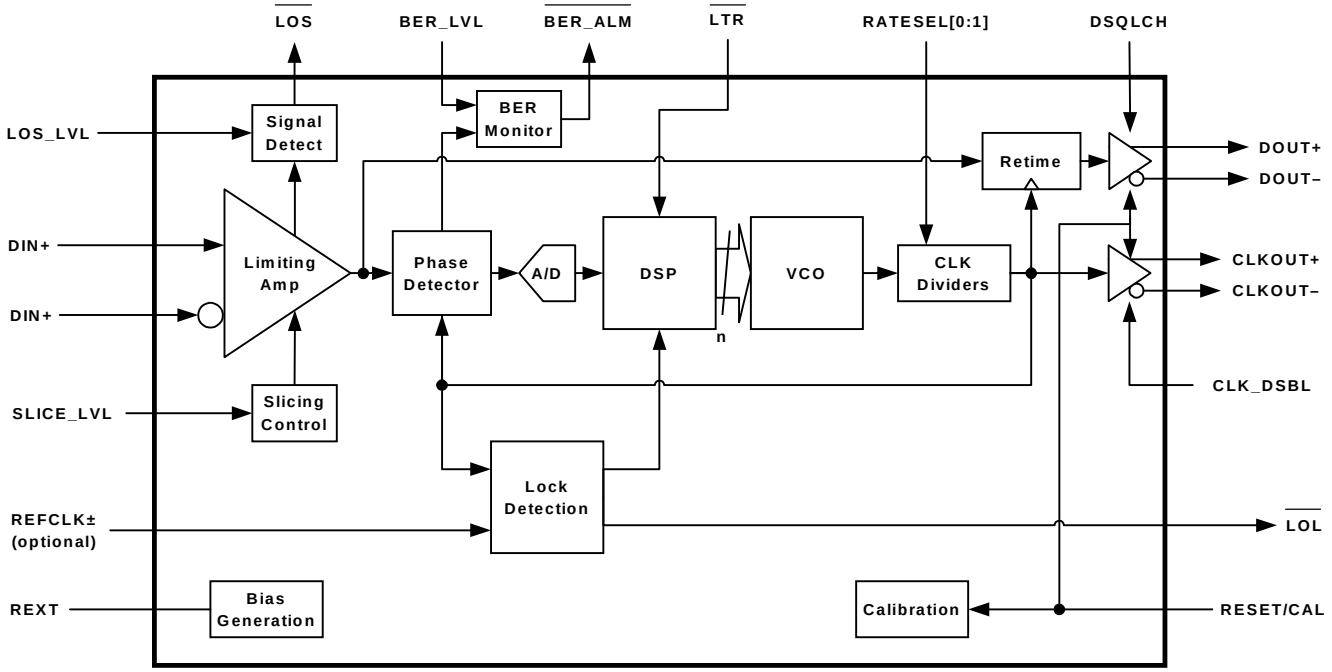


Figure 1. Detailed Block Diagram

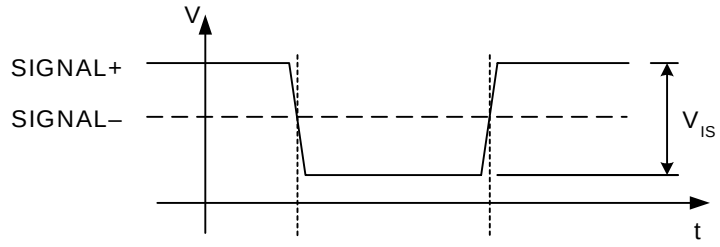
Electrical Specifications

Table 1. Recommended Operating Conditions

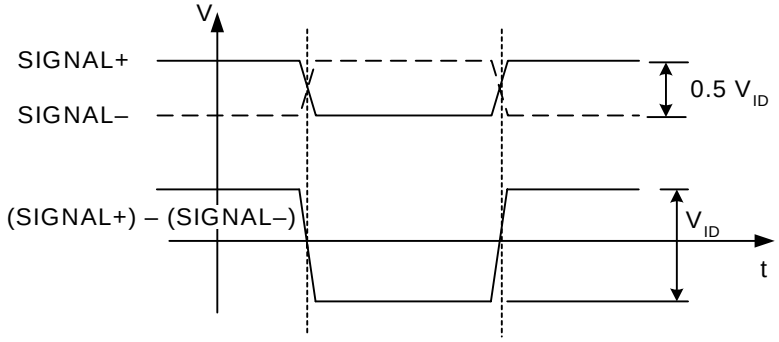
Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40	25	85	°C
Si5022 Supply Voltage[2]	V_{DD}		2.375	2.5	2.625	V
Si5023 Supply Voltage[2]	V_{DD}		3.135	3.3	3.465	V

Notes:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
2. The Si5022/23 specifications are guaranteed when using the recommended application circuit (including component tolerance) of Figure 5 on page 10.



A. Operation with Single-Ended Inputs



B. Operation with Differential Inputs and Outputs

Figure 2. Differential Voltage Measurement (DIN, REFCLK, DOUT, CLKOUT)

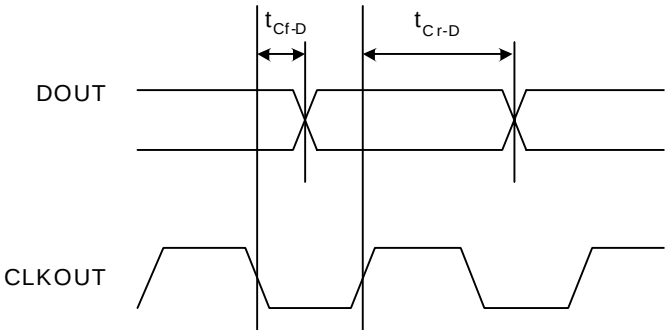


Figure 3. Clock to Data Timing

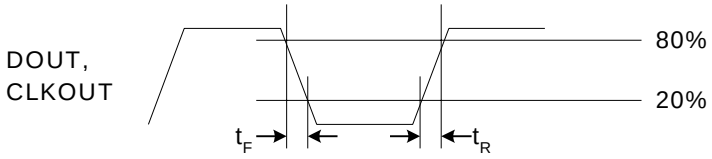


Figure 4. DOUT and CLKOUT Rise/Fall Times

Table 2. DC Characteristics

(V_{DD}=2.5 V ± 5% for Si5022 or 3.3 V ± 5% for Si5023, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}					
OC-48 and FEC (2.7 GHz)			—	148	160	mA
GigE			—	150	162	
OC-12			—	152	164	
OC-3			—	154	165	
Power Dissipation	P_D	VDD =				
OC-48 and FEC (2.7 GHz)		2.5 V (± 5%)	—	370	400	mW
GigE			—	375	405	
OC-12			—	380	410	
OC-3			—	385	414	
Power Dissipation	P_D	VDD =				
OC-48 and FEC (2.7 GHz)		3.3 V (± 5%)	—	488	554	mW
GigE			—	495	561	
OC-12			—	502	568	
OC-3			—	508	572	
Common Mode Input Voltage (DIN)*	V_{ICM}	See Figure 11	1.42	1.50	1.58	V
Common Mode Input Voltage (REFCLK)*	V_{ICM}	See Figure 10	1.90	2.00	2.10	V
DIN Single-ended Input Voltage Swing*	V_{IS}	See Figure 2A	10	—	500	mV
DIN Differential Input Voltage Swing*	V_{ID}	See Figure 2B	10	—	1000	mV
REFCLK Single-ended Input Voltage Swing*	V_{IS}	See Figure 2A	200	—	750	mV
REFCLK Differential Input Voltage Swing*	V_{ID}	See Figure 2B	200	—	1500	mV
Input Impedance (DIN, REFCLK)	R_{IN}	Line-to-Line	84	100	116	Ω
Differential Output Voltage Swing (DOUT)	V_{OD}	100 Ω Load Line-to-Line	TBD	940	TBD	mV (pk-pk)
Differential Output Voltage Swing (CLKOUT)	V_{OD}	100 Ω Load Line-to-Line	TBD	900	TBD	mV (pk-pk)
Output Common Mode Voltage (DOUT,CLKOUT)	V_{OCM}	100 Ω Load Line-to-Line	TBD	1.825	TBD	V
Output Impedance (DOUT,CLKOUT)	R_{OUT}	Single-ended	84	100	116	Ω
Output Current Short to GND (DOUT,CLKOUT)	$I_{SC(–)}$		—	25	TBD	mA
Output Current Short to V_{DD} (DOUT,CLKOUT)	$I_{SC(+)}$		TBD	–15	—	mA
Input Voltage Low (LVTTL Inputs)	V_{IL}		—	—	.8	V
Input Voltage High (LVTTL Inputs)	V_{IH}		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I_{IL}		—	—	10	µA
Input High Current (LVTTL Inputs)	I_{IH}		—	—	10	µA
Output Voltage Low (LVTTL Outputs)	V_{OL}	I_O = 2 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V_{OH}	I_O = 2 mA	2.0	—	—	V
Input Impedance (LVTTL Inputs)	R_{IN}		10	—	—	kΩ
PWRDN/CAL Leakage Current	I_{PWRDN}	$V_{PWRDN} \geq 0.8$ V	TBD	25	TBD	µA
LOS_LVL, BER_LVL, SLICE_LVL Input Impedance	R_{IN}		TBD	100	TBD	kΩ

***Note:** These inputs may be driven differentially or single-endedly. When driven single-endedly, the unused input must be ac coupled to ground.

Table 3. AC Characteristics (Clock and Data)

(V_{DD}=2.5 V ± 5% for Si5022 or 3.3 V ± 5% for Si5023, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clock Rate	f_{CLK}		.15	—	2.7	GHz
Output Rise Time	t_R	Figure 4	—	100	TBD	ps
Output Fall Time	t_F	Figure 4	—	100	TBD	ps
Clock to Data Delay FEC (2.7 GHz) OC-48 GigE OC-12 OC-3	t_{Cr-D}	Figure 3	 TBD TBD TBD TBD TBD	 250 255 500 890 4100	 TBD TBD TBD TBD TBD	ps
Clock to Data Delay FEC (2.7 GHz) OC-48	t_{Cf-D}	Figure 3	 TBD TBD	 TBD TBD	 TBD TBD	ps
Input Return Loss		100 kHz–2.5 GHz 2.5 GHz–4.0 GHz	TBD TBD	— —	— —	dB dB
Slicing Level Offset* (relative to the internally set input common mode voltage)	V_{SLICE}	SLICE_LVL = 750 mV to 2.25 V	–15	—	15	mV
Slicing Level Accuracy		SLICE_LVL = 750 mV to 2.25 V	–500	—	500	µV

***Note:** Adjustment voltage (relative to the internally set input common mode voltage) is calculated as follows: V_{SLICE} = (SLICE_LVL – 1.50 V)/50.

Table 4. AC Characteristics (PLL Characteristics)
(V_{DD}=2.5 V ± 5% for Si5022 or 3.3 V ± 5% for Si5023, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance (OC-48)*	$J_{TOL(PP)}$	f = 600 Hz	40	TBD	—	UI_{PP}
		f = 6000 Hz	4	TBD	—	UI_{PP}
		f = 100 kHz	4	TBD	—	UI_{PP}
		f = 1 MHz	0.4	TBD	—	UI_{PP}
Jitter Tolerance (OC-12 Mode)*	$J_{TOL(PP)}$	f = 30 Hz	40	TBD	—	UI_{PP}
		f = 300 Hz	4	TBD	—	UI_{PP}
		f = 25 kHz	4	TBD	—	UI_{PP}
		f = 250 kHz	0.4	TBD	—	UI_{PP}
Jitter Tolerance (OC-3 Mode)*	$J_{TOL(PP)}$	f = 30 Hz	60	TBD	—	UI_{PP}
		f = 300 Hz	6	TBD	—	UI_{PP}
		f = 6.5 kHz	6	TBD	—	UI_{PP}
		f = 65 kHz	0.6	TBD	—	UI_{PP}
Jitter Tolerance (Gigabit Ethernet) Receive Data Total Jitter Tolerance	$T_{JT(PP)}$	IEEE 802.3z Clause 38.68	600	TBD	—	ps
Jitter Tolerance (Gigabit Ethernet) Receive Data Deterministic Jitter Tolerance	$D_{JT(PP)}$	IEEE 802.3z Clause 38.69	370	TBD	—	ps
RMS Jitter Generation*	$J_{GEN(RMS)}$	with no jitter on serial data	—	3.0	5.0	mUI
Peak-to-Peak Jitter Generation*	$J_{GEN(PP)}$	with no jitter on serial data	—	25	55	mUI
Jitter Transfer Bandwidth*	J_{BW}	OC-48 Mode	—	—	2.0	MHz
		OC-12 Mode	—	—	500	kHz
		OC-3 Mode	—	—	130	kHz
Jitter Transfer Peaking*	J_P		—	0.03	0.1	dB
Acquisition Time (Reference clock applied)	T_{AQ}	After falling edge of PWRDN/CAL	1.45	1.5	1.7	ms
		From the return of valid data	40	60	150	µs
Acquisition Time (Reference-less operation)	T_{AQ}	After falling edge of PWRDN/CAL	TBD	TBD	TBD	ms
		From the return of valid data	TBD	TBD	TBD	ms
Reference Clock Range			19.44	—	168.75	MHz
Input Reference Clock Frequency Tolerance	C_{TOL}		–100	—	100	ppm
Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock)			TBD	600	TBD	ppm
Frequency Difference at which Receive PLL goes into Lock (REF-CLK compared to the divided down VCO clock)			TBD	300	TBD	ppm

***Note:** As defined in Bellcore specifications: GR-253-CORE, Issue 2, December 1995. Using PRBS 2^{23} – 1 data pattern.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.8 (Si5022) –0.5 to 3.5 (Si5023)	V
LVTTL Input Voltage	V_{DIG}	–0.3 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
Lead Temperature (soldering 10 seconds)		300	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		1	kV

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

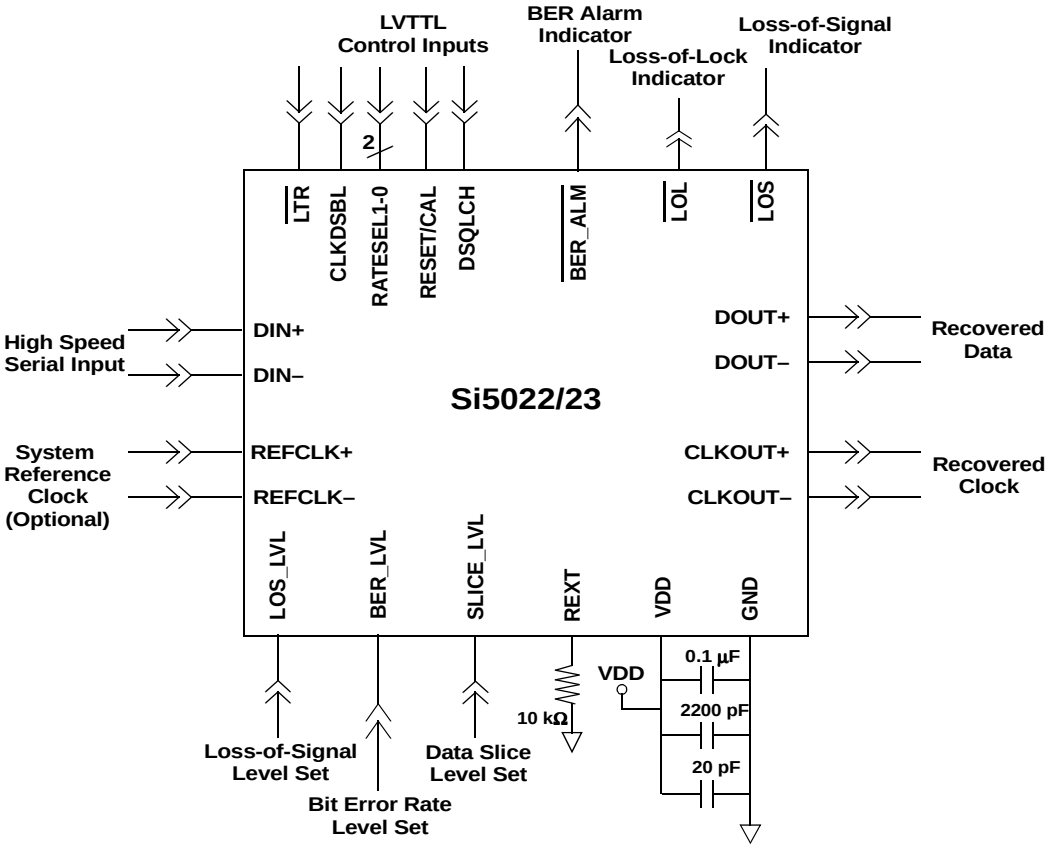


Figure 5. Si5022/23 Typical Application Circuit

Functional Description

The Si5022/23 integrates a high-speed limiting amplifier (LA) with a multi-rate clock and data recovery unit (CDR) that operates up to 2.7 Gbps. No external reference clock is required for clock and data recovery. The limiting amplifier magnifies very low-level input data signals so that accurate clock and data recovery can be performed. The CDR uses Silicon Laboratories' DSPLL technology to recover a clock synchronous to the input data stream. The recovered clock is used to retime the incoming data, and both are output synchronously via current-mode logic (CML) drivers. Silicon Laboratories' DSPLL technology ensures superior jitter performance while eliminating the need for external loop filter components found in traditional phase-lock loop implementations.

The limiting amplifier includes a control input for adjusting the 0/1 data slicing level and provides a loss-of-signal level alarm output. The CDR includes a bit-error-rate performance monitor which signals a high bit-error-rate condition (associated with excessive incoming jitter) relative to an externally adjustable bit-error-rate threshold.

The optional reference clock minimizes the CDR acquisition time and provides a stable reference for maintaining the output clock when locking to reference is desired.

Limiting Amplifier

The limiting amplifier accepts the low-level signal output from a transimpedance amplifier (TIA). The low-level signal is amplified to a usable level for the clock and data recovery unit. The minimum input swing requirement is specified in Table 2. Larger input amplitudes (up to the maximum input swing specified in Table 2) are accommodated without degradation of performance. The limiting amplifier ensures optimal data slicing by using a digital dc offset cancellation technique to remove any dc bias introduced by the amplification stage.

DSPLL™

The Si5022/23 PLL structure (shown in Figure 1 on page 4) utilizes Silicon Laboratories' DSPLL technology to maintain superior jitter performance while eliminating the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage controlled oscillator (VCO). This technology enables clock and data recovery with far less jitter than is generated using traditional methods and it eliminates performance degradation caused by external component aging. In addition, because external loop filter components are not required, sensitive noise entry points are eliminated, thus making the DSPLL less susceptible to board-level noise sources and making SONET/SDH jitter compliance easier to attain in the application.

Multi-Rate Operation

The Si5022/23 supports clock and data recovery for OC-48 and STM-16 data streams. In addition, the PLL was designed to operate at data rates up to 2.7 Gbps to support OC-48/STM-16 applications that employ forward error correction (FEC).

Multi-rate operation is achieved by configuring the device to divide down the output of the VCO to the desired data rate. The divide factor is configured by the RATESEL[0:1] pins. The RATESEL[0:1] configuration and associated data rates are given in Table 7.

Table 7. Multi-Rate Configuration

RATESEL [0:1]	SONET/ SDH	Gigabit Ethernet	OC-48 with 15/14 FEC	CLK Divider
11	2.488 Gbps	—	2.67 Gbps	1
10	1.244 Gbps	1.25 Gbps	—	2
01	622.08 Mbps	—	—	4
00	155.52 Mbps	—	—	16

Operation Without an External Reference

The Si5022/23 can perform clock and data recovery without an external reference clock. Tying the REFCLK inputs to GND configures the device to operate without an external reference clock. Clock recovery is achieved by monitoring the timing quality of the incoming data relative to the VCO frequency. Lock is maintained by continuously monitoring the incoming data timing quality and adjusting the VCO accordingly. Details of the lock detection and the lock-to-reference functions while in this mode are described in their respective sections below.

Note: Without an external reference the acquisition of data is dependent solely on the data itself and will typically require more time to acquire lock than when a reference is applied.

Operation With an External Reference

The Si5022/23 device's optional external reference clock centers the DSPLL, minimizes the acquisition time, and maintains a stable output clock (CLKOUT) when lock-to-reference (LTR) is asserted.

When the reference clock is present, the Si5022/23 will use the reference clock to center the VCO output frequency so that clock and data can be recovered from the input data stream. The device will self configure for operation with one of three reference clock frequencies. This eliminates the need to externally configure the device to operate with a particular reference clock.

The reference clock centers the VCO for a nominal output between 2.5 and 2.7 GHz. The VCO frequency is centered at 16, 32, or 128 times the reference clock frequency. Detection circuitry continuously monitors the reference clock input to determine whether the device should be configured for a reference clock that is 1/16, 1/32, or 1/128 the nominal VCO output. Approximate reference clock frequencies for some target applications are given in Table 8.

Table 8. Typical REFCLK Frequencies

SONET/SDH	Gigabit Ethernet	SONET/ SDH with 15/14 FEC	Ratio of VCO to REFCLK
19.44 MHz	19.53 MHz	20.83 MHz	128
77.76 MHz	78.125 MHz	83.31 MHz	32
155.52 MHz	156.25 MHz	166.63 MHz	16

Lock Detect

The Si5022/23 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. The operation of the lock-detector depends on the reference clock option used.

When an external reference clock is provided, the circuit compares the frequency of a divided down version of the recovered clock with the frequency of the supplied reference clock (REFCLK). If the recovered clock frequency deviates from that of the reference clock by the amount specified in Table 4 on page 9, the PLL is declared out of lock, and the loss-of-lock (LOL) pin is asserted. In this state, the DSPLL will periodically try to reacquire lock with the incoming data stream. During reacquisition, the recovered clock frequency (CLKOUT) will drift over a 1% range relative to the supplied reference clock. The LOL output will remain asserted until the recovered clock frequency is within the REFCLK frequency by the amount specified in Table 4 on page 9. In applications requiring a more stable output clock during out-of-lock conditions, the lock-to-reference (LTR) input can be used to force the PLL to lock to the externally supplied reference.

In the absence of an external reference, the lock detect circuitry uses a data quality measure to determine when frequency lock has been lost with the incoming data stream. Once LOL has been asserted, it will remain active until data is reacquired. During this reacquisition period, CLKOUT may vary by approximately ±10% from the nominal data rate. For applications requiring a more stable output clock during out-of-lock conditions, LTR can be used to stabilize the output clock.

Lock-to-Reference

The lock-to-reference input (LTR) can be used to force a stable output clock when an alarm condition, like LOS, exists. In typical applications, the LOS output would be tied to the LTR input to force a stable output clock when the input data signal is lost. When LTR is asserted, the DSPLL is prevented from acquiring the data signal present on DIN. The operation of the LTR control input depends on which reference clocking mode is used.

When an external reference clock is present, assertion of LTR will force the DSPLL to lock CLKOUT to the provided reference. If no external reference clock is used, LTR will force the DSPLL to hold the digital frequency control input to the VCO at the last value. This produces an output clock that is stable as long as supply and temperature are constant.

Loss-of-Signal

The Si5022/23 indicates a loss-of-signal condition on the LOS output pin when the input peak-to-peak signal level on DIN falls below an externally controlled threshold. The LOS threshold range is specified in Table 3 and is set by applying a voltage on the LOS_LVL pin. The graph in Figure 6 illustrates the LOS_LVL mapping to the LOS threshold. The LOS output is asserted when the input signal drops below the programmed peak-to-peak value.

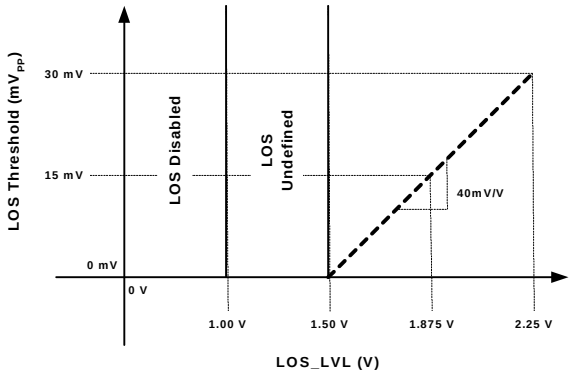


Figure 6. LOS_LVL Mapping

Approximately 6 dB of level detection hysteresis prevents unnecessary switching on LOS when marginal input data swing peak-to-peak levels are present. Hysteresis is defined as the difference between the LOS deassert level (LOSD) and the LOS assert level (LOSA). The hysteresis in decibels is calculated as 20log((LOSD – LOSA)/LOSA). The relationship between the LOS assert level and the LOS deassert level is shown in Figure 7. When the LOS assert level is set below 10 mV, the amount of hysteresis is fixed at 5 mV. When the LOS assert level is set above 10 mV, the amount of hysteresis is approximately 6 dB.

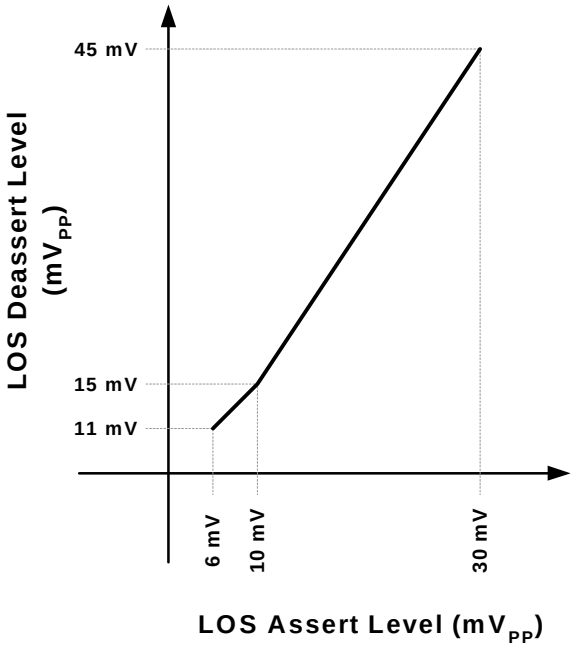


Figure 7. Hysteresis Dependency

Bit-Error-Rate (BER) Detection

The Si5022/23 uses a proprietary Silicon Laboratories algorithm to generate a bit-error-rate (BER) alarm on the BER_ALM pin if the observed BER is greater than a user programmable threshold. Bit error detection relies on the input data edge timing; edges occurring outside of the expected event window are counted as bit errors. The BER alarm threshold can be set to one of 64 discrete values between 10^{-3} and 10^{-4}. The BER threshold is programmed by applying a voltage to the BER_LVL pin between 500 mV and 2.25 V corresponding to 10^{-3} and 10^{-4} respectively.

Data Slicing Level

The Si5022/23 provides the ability to externally adjust the 0/1 slicing level for applications that require bit-error-rate (BER) optimization. Adjustments in slicing level of ±15 mV (relative to the internally set input common mode voltage) are supported. The 0/1 slicing level is set by applying a voltage between 0.75 V and 2.25 V to the SLICE_LVL input. The voltage present on SLICE_LVL maps to the 0/1 slicing level as follows:

$$V_{SLICE} = \frac{(V_{SLICE\_LVL} - 1.5\ V)}{50}$$

where V_{SLICE} is the slicing level and V_{SLICE_LVL} is the voltage applied to the SLICE_LVL pin.

When SLICE_LVL is driven below 500 mV, the 0/1 slicing level adjustment is disabled, and the slicing level is set to the cross-point of the differential input signal.

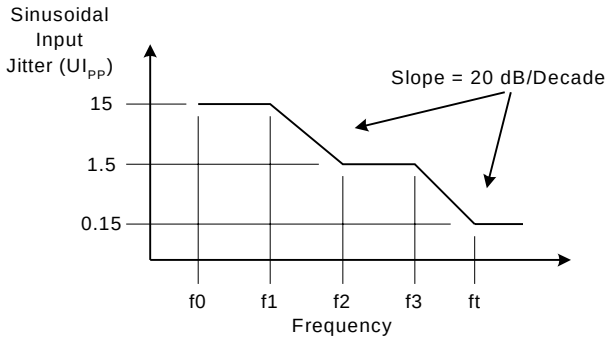
PLL Performance

The PLL implementation used in the Si5022/23 is fully compliant with the jitter specifications proposed for SONET/SDH equipment by Bellcore GR-253-CORE, Issue 2, December 1995 and ITU-T G.958.

Jitter Tolerance

The Si5022/23's tolerance to input jitter exceeds that of the Bellcore/ITU mask shown in Figure 8. This mask defines the level of peak-to-peak sinusoid jitter that must be tolerated when applied to the differential data input of the device.

Note: There are no entries in the mask table for the data rate corresponding to OC-24 as that rate is not specified by either GR-253 or G.958.



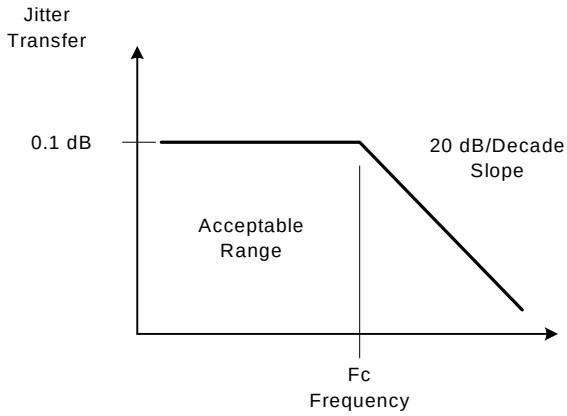
SONET Data Rate	F0 (Hz)	F1 (Hz)	F2 (kHz)	F3 (kHz)	Ft (kHz)
OC-48	10	600	6000	100	1000
OC-12	10	30	300	25	250
OC-3	10	30	300	6.5	65

Figure 8. Jitter Tolerance Specification

Jitter Transfer

The Si5022/23 exceeds all relevant Bellcore/ITU specifications related to SONET/SDH jitter transfer. Jitter transfer is defined as the ratio of output signal jitter to input signal jitter as a function of jitter frequency. (See Figure 9.) These measurements are made with an input

test signal that is degraded with sinusoidal jitter whose magnitude is defined by the mask in Figure 9.



SONET Data Rate	Fc (kHz)
OC-48	2000
OC-12	500
OC-3	130

Figure 9. Jitter Transfer Specification

Jitter Generation

The Si5022/23 exceeds all relevant specifications for jitter generation proposed for SONET/SDH equipment. The jitter generation specification defines the amount of jitter that may be present on the recovered clock and data outputs when a jitter free input signal is provided. The Si5022/23 typically generates less than 3.0 mUI_{RMS} of jitter when presented with jitter-free input data.

RESET/DSPLL Calibration

The Si5022/23 achieves optimal jitter performance by using self-calibration circuitry to set the loop gain parameters within the DSPLL. For the self-calibration circuitry to operate correctly, the power supply voltage must exceed TBD V when calibration occurs. Self-calibration is initiated by a high-to-low transition on the RESET/CAL pin. The RESET/CAL pin must be held high for at least 1 µS after the supply has stabilized on power-up for optimum device operation. When RESET/CAL is released (set to low) the digital logic resets to a known initial condition, recalibrates the DSPLL, and will begin to lock to the incoming data stream.

Clock Disable

The Si5022/23 provides a clock disable pin, CLK_DSBL, that is used to disable the recovered clock output, CLKOUT. When the CLK_DSBL pin is asserted, the positive and negative terminals of CLKOUT are tied to VDD through 100 Ω on-chip resistors. This feature is used to reduce power consumption in applications that do not use the recovered clock.

Data Squelch

The Si5022/23 provides a data squelching pin, DSQLCH, that is used to set the recovered data output, DOUT, to binary zero. When the DSQLCH pin is asserted, the DOUT logic signal is held at a binary zero. This pin can be is used to squelch corrupt data during LOS and LOL situations. Care must be taken when ac coupling these outputs; a long string of zeros will not be held through ac coupling capacitors.

Device Grounding

The Si5022/23 uses the GND pad on the bottom of the 28-pin micro leaded package (MLP) for device ground. This pad should be connected directly to the analog supply ground. See Figures 13 and 14 for the ground (GND) pad location.

Bias Generation Circuitry

The Si5022/23 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption versus traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

Voltage Regulator

The Si5022 and Si5023 operate from different external supply voltages. Internally the devices are identical and operate from a 2.5 V supply. The Si5022 takes the 2.5 V supply directly from the external supply connections. The Si5023 regulates 2.5 V internally down from the external 3.3 V supply. Both devices consume 148 mA typically.

In addition to supporting 3.3 V systems, the on-chip linear regulator offers better power supply noise rejection versus the direct 2.5 V supply.

Differential Input Circuitry

The Si5022/23 provides differential inputs for both the high speed data (DIN) and the reference clock (REFCLK) inputs. An example termination for these inputs is shown in Figure 10 and Figure 11 respectively. In applications where direct dc coupling is possible, the 0.1 µF capacitors may be omitted. (LOS operation is only guaranteed when ac coupled.) The data input limiting amplifier requires an input signal with a differential peak-to-peak voltage as specified in Table 2 to ensure a BER of at least 10^{-12}. The REFCLK input differential peak-to-peak voltage requirement is specified in Table 2.

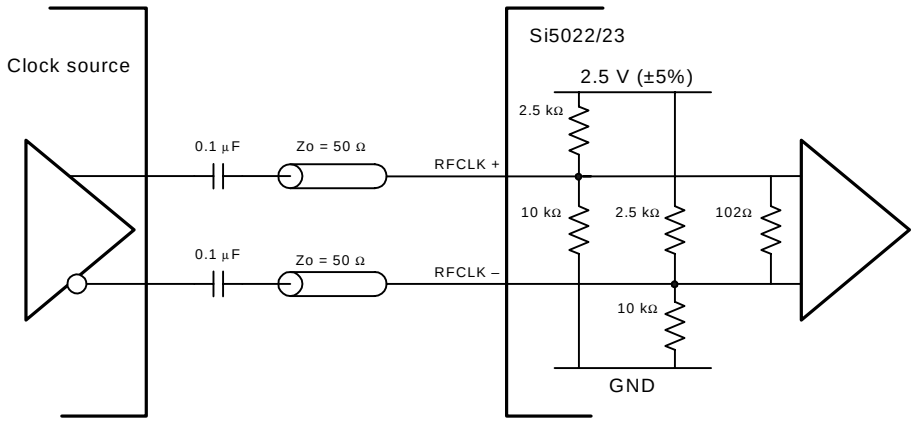


Figure 10. Input Termination for REFCLK (AC Coupled)

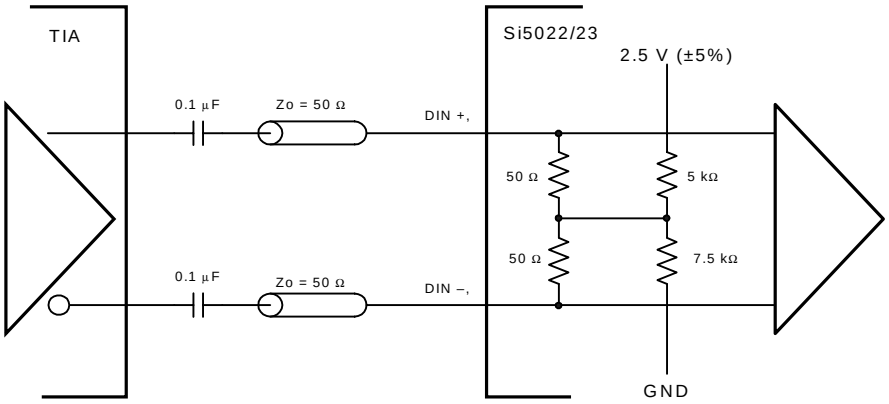


Figure 11. Input Termination for DIN (AC Coupled)

Differential Output Circuitry

The Si5022/23 utilizes a current-mode logic (CML) architecture to output both the recovered clock (CLKOUT) and data (DOUT). An example of output termination with ac coupling is shown in Figure 12. In applications in which direct dc coupling is possible, the 0.1 µF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is specified in Table 2.

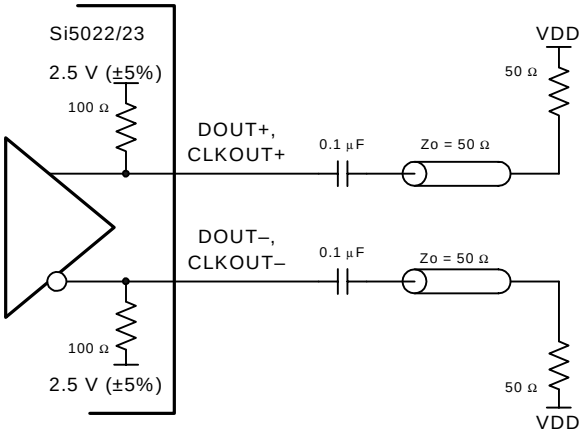
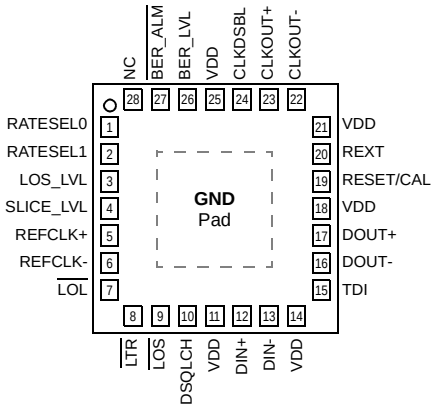


Figure 12. Output Termination for DOUT and CLKOUT (AC Coupled)

Pin Descriptions: Si5022/23



Top View

Figure 13. Si5022/23 Pin Configuration

Table 9. Si5022/23 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1,2	RATESEL0, RATESEL1	I	LVTTL	**Data Rate Select.** These pins configure the onboard PLL for clock and data recovery at one of four user selectable data rates. See Table 7 for configuration settings. **Note:** These inputs have weak internal pull-ups.
3	LOS_LVL	I		**LOS Level Control.** The LOS threshold is set by the input voltage level applied to this pin. Figure 6 on page 12 shows the input setting to output threshold mapping. LOS is disabled when the voltage applied is less than 500 mV.
4	SLICE_LVL	I		**Slicing Level Control.** The slicing threshold level is set by applying a voltage to this pin as described in the Slicing Level section of the data sheet. If this pin is tied to GND, slicing level adjustment is disabled, and the slicing level is set to the midpoint of the differential input signal on DIN. Slicing level becomes active when the voltage applied to the pin is greater than 500 mV.
5,6	REFCLK+, REFCLK–	I	See Table 2	**Differential Reference Clock (Optional).** When present, the reference clock sets the center operating frequency of the DSPLL for clock and data recovery. Tie these pins to ground to configures the DSPLL to operate without an external reference clock. See Table 8 for typical reference clock frequencies.

Table 9. Si5022/23 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
7	$\overline{\text{LOL}}$	O	LVTTL	**Loss-of-Lock.** This output is driven low when the recovered clock frequency deviates from the reference clock by the amount specified in Table 4 on page 9. If no external reference is supplied, this signal will be active when the internal PLL is no longer locked to the incoming data.
8	$\overline{\text{LTR}}$	I	LVTTL	**Lock-to-Reference.** When this pin is low, the DSPLL will disregard the data inputs. If an external reference is supplied, the output clock will be locked to the supplied reference. If no external reference is used, the DSPLL will lock the control loop until LTR is released. **Note:** This input has a weak internal pull-up.
9	$\overline{\text{LOS}}$	O	LVTTL	**Loss-of-Signal.** This output pin is driven low when the input signal is below the threshold set via LOS_LVL. The LOS state will nominally have 3 dB of hysteresis relative to the level set on LOS_LVL. (LOS operation is guaranteed only when ac coupling is used on the clock input.)
10	DSQLCH		LVTTL	**Data Squelch.** When driven high, this pin forces the data present on DOUT to zero. For normal operation, this pin should be low. DSQLCH can be used during LOS/LOL conditions to prevent random data from being presented to the system. **Note:** This input has a weak internal pull-down.
11,14,18,21, 25	VDD		2.5 V or 3.3 V	**Supply Voltage.** Nominally 2.5 V for Si5022 and 3.3 V for Si5023.
12,13	DIN+, DIN–	I	See Table 2	**Differential Data Input.** Clock and data are recovered from the differential signal present on these pins. ac coupling is recommended.
15	TDI	I	LVTTL	**Production Test Input.** This pin is used during production testing and **must** be tied to GND for normal operation.
16,17	DOUT+, DOUT–	O	CML	**Differential Data Output.** The data output signal is a retimed version of the data recovered from the signal present on DIN. It is phase aligned with CLKOUT and is updated on the rising edge of CLKOUT.

Table 9. Si5022/23 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
19	RESET/CAL	I	LVTTL	**Reset/Calibrate.** Driving this input high for at least 1 µS will reset internal device circuitry. A high to low transition on this pin will force a DSPLL calibration. For normal operation, drive this pin low. This pin should be used to force a DSPLL calibration on power-up to ensure optimal jitter performance. **Note:** This input has a weak internal pull-down.
20	REXT			**External Bias Resistor.** This resistor is used to establish internal bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.
22,23	CLKOUT–, CLKOUT+	O	CML	**Differential Clock Output.** The output clock is recovered from the data signal present on DIN except when LTR is asserted or the LOL state has been entered.
24	CLKDSBL	I	LVTTL	**Clock Disable.** When this input is high, the CLKOUT output drivers are disabled. For normal operation, this pin should be low. **Note:** This input has a weak internal pull-down.
26	BER_LVL	I		**Bit Error Rate Level Control.** The BER threshold level is set by applying a voltage to this pin. The applied voltage is mapped to one of 64 BER threshold levels. When the BER exceeds the programmed threshold, BER_ALM is driven low. If this pin is tied to GND, BER_ALM is disabled. If it is tied to V_{DD}, BER_LVL defaults to 10^{-3} BER
27	$\overline{\text{BER\_ALM}}$	O	LVTTL	**Bit Error Rate Alarm.** This pin will be driven low to indicate that the BER threshold set by BER_LVL has been exceeded. The alarm will clear after the BER rate has improved by approximately a factor of 2.
28	NC			**No Connect.** Leave this pin unconnected.
GND Pad	GND		GND	**Supply Ground.** Nominally 0.0 V. The GND pad found on the bottom of the 28-lead micro leaded package (see Figure 14) must be connected directly to supply ground. Minimize the ground path inductance for optimal performance.

Ordering Guide

Table 10. Ordering Guide

Part Number	Package	Voltage	Temperature
Si5022-BM	28-lead MLP	2.5	–40°C to 85°C
Si5023-BM	28-lead MLP	3.3	–40°C to 85°C

Package Outline

Figure 14 illustrates the package details for the Si5022 and Si5023. Table 11 lists the values for the dimensions shown in the illustration.

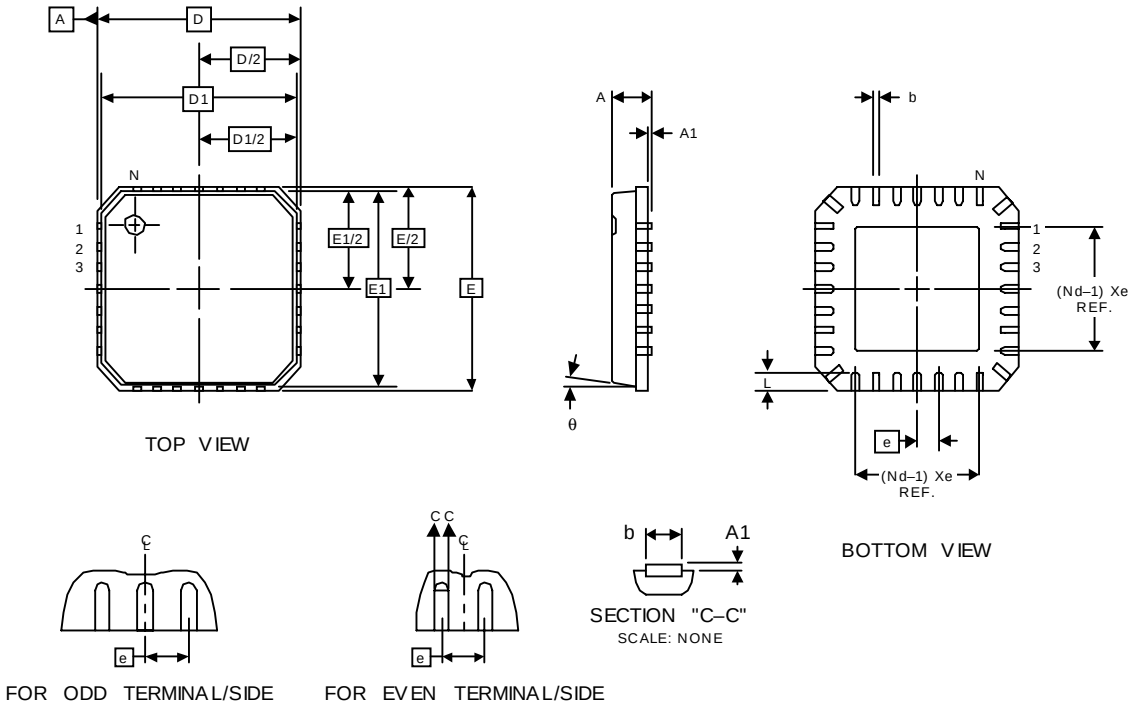


Figure 14. 28-Lead Micro Leaded Package (MLP)

Table 11. Package Diagram Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	—	0.90	1.00
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D	5.00 BSC		
D1	4.75 BSC		
E	5.00 BSC		
E1	4.75 BSC		
N	28		
Nd	7		
Ne	7		
e	0.50 BSC		
L	0.50	0.60	0.75
θ			12°

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