SILICON LABORATORIES

PRECISION HIGH SPEED CLOCK MULTIPLIER/REGENERATOR IC

Features

Complete precision high speed clock multiplier and regenerator device:

- Performs Clock Multiplication to One of Four Frequency Ranges: 150–167 MHz, 600–668 MHz, 1.2–1.33 GHz, or 2.4–2.67 GHz
- Jitter Generation as low as 0.5 ps_{RMS} for 622 MHz Output
- Accepts Input Clock from 9.4–668 MHz

- Regenerates a "Clean", Jitter-Attenuated Version of Input Clock
- DSPLL™ Technology Provides Superior Jitter Performance
- Small Footprint: 4 mm x 4 mm
- Low Power: 310 mW typical
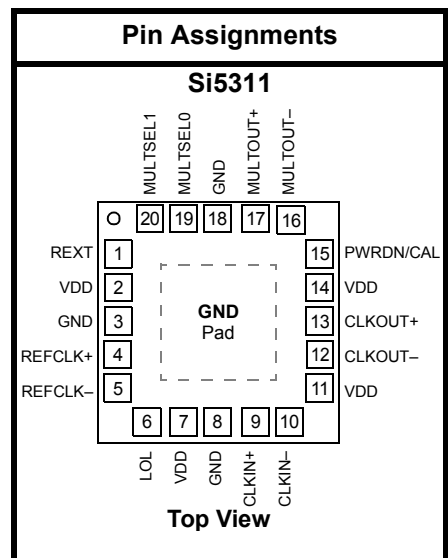
Ordering Information:
See page 22.
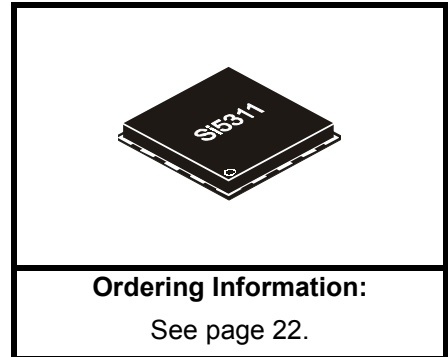
Applications

- SONET/SDH Systems
- Terabit Routers
- Digital Cross Connects
- Optical Transceiver Modules
- Gigabit Ethernet Systems
- Hybrid VCO Modules

Description

The Si5311 is a fully integrated high-speed clock multiplier and clock regenerator IC. The clock multiplier generates an output clock that is an integer multiple of the input clock. When the clock multiplier is operating in either the 150–167 MHz range or the 600–668 MHz range, the clock regenerator operates simultaneously. The clock regenerator creates a "clean" version of the input clock by using the clock synthesis phase-locked loop (PLL) to remove unwanted jitter and square up the input clock's rising and falling edges. The Si5311 uses Silicon Laboratories patented DSPLL™ architecture to achieve superior jitter performance while eliminating the analog loop filter found in traditional PLL designs.

The Si5311 represents a new standard in low jitter, small size, low power, and ease-of-use for high speed clock devices. It operates from a single 2.5 V supply over the industrial temperature range (–40°C to 85°C).

Pin Assignments
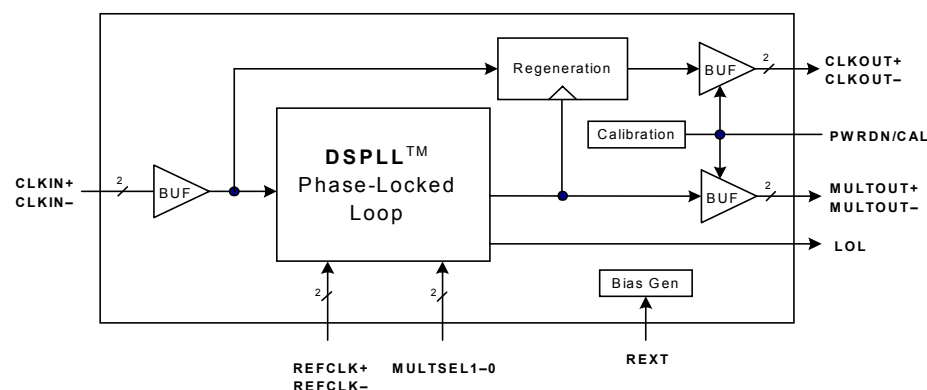#### Si5311

Top View

Functional Block Diagram

This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

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Detailed Block Diagram

Figure 1. Detailed Block Diagram

Preliminary Rev. 0.6

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40	25	85	°C
Si5311 Supply Voltage[2]	V_{DD}		2.375	2.5	2.625	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
2. The Si5311 specifications are guaranteed when using the recommended application circuit (including component tolerance) of Figure 5 on page 13.
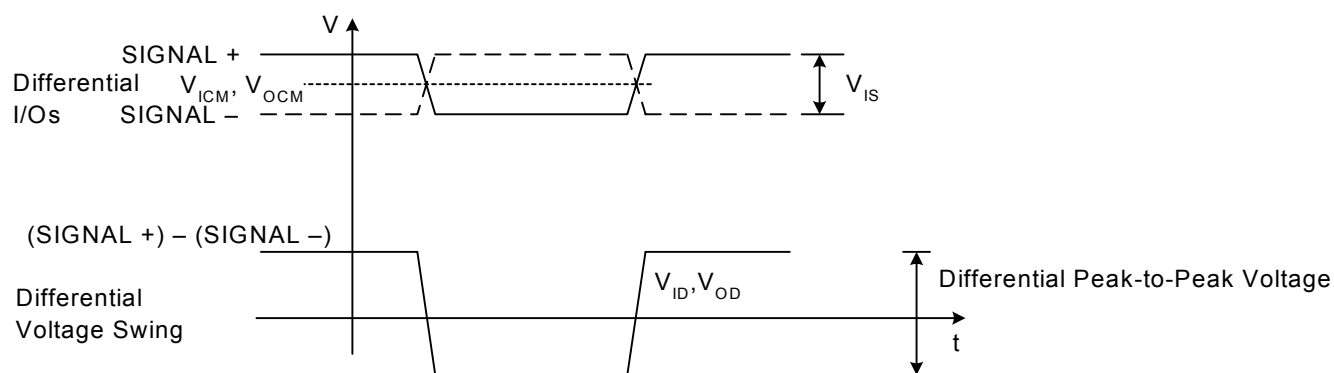

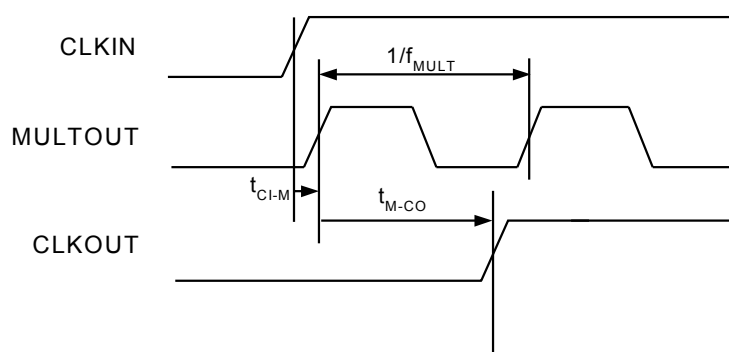**Figure 2. Differential Voltage Measurement (CLKIN, REFCLK, CLKOUT, MULTOUT)**

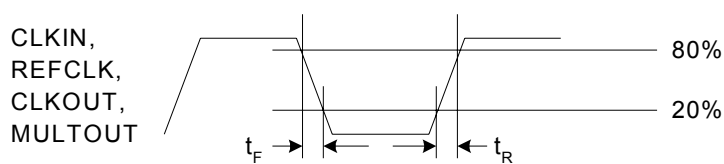**Figure 3. CLKIN to CLKOUT, MULTOUT Phase Relationship**

Figure 4. Clock Input and Output Rise/Fall Times

Table 2. DC Characteristics, V$_{DD}$ = 2.5 V

(V$_{DD}$ = 2.5 V ± 5%, T$_A$ = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current MULTSEL[1:0] = 00 MULTSEL[1:0] = 01 MULTSEL[1:0] = 10 MULTSEL[1:0] = 11	I$_{DD}$		 — — — —	 108 113 117 124	 118 123 127 134	mA
Power Dissipation MULTSEL[1:0] = 00 MULTSEL[1:0] = 01 MULTSEL[1:0] = 10 MULTSEL[1:0] = 11	P$_D$		 — — — —	 270 283 293 310	 310 323 333 352	mW
Common Mode Input Voltage (CLKIN, REFCLK)	V$_{ICM}$	See Figure 2	—	.80 • V$_{DD}$	—	V
Input Voltage Range* (CLKIN+, CLKIN–, REFCLK+, REFCLK–)	V$_{IS}$	See Figure 2	—	—	750	mV
Differential Input Voltage Swing* (CLKIN, REFCLK)	V$_{ID}$	See Figure 2	200	—	1500	mV (pk-pk)
Input Impedance (CLKIN, REFCLK)	R$_{IN}$	Line-to-Line	84	100	116	Ω
Differential Output Voltage Swing (CLKOUT)	V$_{OD}$	100 Ω Load Line-to-Line	TBD	940	TBD	mV (pk-pk)
Differential Output Voltage Swing (MULTOUT)	V$_{OD}$	100 Ω Load Line-to-Line	TBD	900	TBD	mV (pk-pk)
Output Common Mode Voltage (CLKOUT, MULTOUT)	V$_{OCM}$	100 Ω Load Line-to-Line	—	V$_{DD}$ – 0.7	—	V
Output Impedance (CLKOUT, MULTOUT)	R$_{OUT}$	Single-ended	84	100	116	Ω
Output Short to GND (CLKOUT, MULTOUT)	I$_{SC(–)}$		—	25	TBD	mA
Output Short to V$_{DD}$ (CLKOUT, MULTOUT)	I$_{SC(+)}$		TBD	–15	—	mA
Input Voltage Low (LVTTL Inputs)	V$_{IL}$		—	—	.8	V
Input Voltage High (LVTTL Inputs)	V$_{IH}$		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I$_{IL}$		—	25	TBD	μA
Input High Current (LVTTL Inputs)	I$_{IH}$		—	25	TBD	μA
Output Voltage Low (LVTTL Outputs)	V$_{OL}$	I$_O$ = 2 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V$_{OH}$	I$_O$ = 2 mA	2.0	—	—	V
Input Impedance (LVTTL Inputs)	R$_{IN}$		100	—	—	kΩ
PWRDN/CAL Internal Pulldown Current	I$_{PWRDN}$	V$_{PWRDN}$ ≥ 0.8 V	TBD	25	TBD	μA

*Note: The CLKIN and REFCLK inputs may be driven differentially or single-endedly. When driving single-endedly, the voltage swing of the signal applied to the active input must exceed the specified minimum Differential Input Voltage Swing (V$_{ID}$ min) and the unused input must be ac-coupled to ground. When driving differentially, the difference between the positive and negative input signals must exceed V$_{ID}$ min. (Each individual input signal needs to swing only half of this range.) In either case, the voltage applied to any individual pin (CLKIN+, CLKIN–, REFCLK+, or REFCLK–) must not exceed the specified maximum Input Voltage Range (V$_{IS}$ max).

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Table 3. AC Characteristics

(V_{DD} = 2.5 V ± 5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKIN Frequency Range[*]			9.375	—	668	MHz
CLKIN Duty Cycle			TBD	—	TBD	%
REFCLK Range[*]			9.375	—	167	MHz
REFCLK Duty Cycle	C_{DUTY}		40	50	60	%
REFCLK Frequency Tolerance	C_{TOL}		–100	—	100	ppm
MULTOUT Clock Rate MULTSEL[1:0] = 00 MULTSEL[1:0] = 01 MULTSEL[1:0] = 10 MULTSEL[1:0] = 11	f_{MULT}		2400 1200 600 150	— — — —	2672 1336 668 167	MHz
Output Rise Time (CLKOUT, MULTOUT)	t_R	Figure 4	—	100	TBD	ps
Output Fall Time (CLKOUT, MULTOUT)	t_F	Figure 4	—	100	TBD	ps
Input Rise Time (CLKIN, REFCLK)	t_R	Figure 4	—	—	TBD	ps
Input Fall Time (CLKIN, REFCLK)	t_F	Figure 4	—	—	TBD	ps
CLKIN to MULTOUT Delay MULTSEL[1:0] = 00 MULTSEL[1:0] = 01 MULTSEL[1:0] = 10 MULTSEL[1:0] = 11	t_{CI-M}	Figure 3	TBD TBD TBD TBD	0 120 150 3.4	TBD TBD TBD TBD	ps ps ps ns
MULTOUT to CLKOUT Delay MULTSEL[1:0] = 00 MULTSEL[1:0] = 01 MULTSEL[1:0] = 10 MULTSEL[1:0] = 11	t_{M-CO}	Figure 3	— — TBD TBD	— — $1/f_{MULT}$ + 160 960	— — TBD TBD	 ps ps
Input Return Loss		100 kHz–2.5 GHz 2.5 GHz–4.0 GHz	18.7 TBD	— —	— —	dB
*Note: See Table 11.						

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Table 4. AC Characteristics (PLL Performance Characteristics)

(V_{DD} = 2.5 V ± 5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance (MULTSEL[1:0] = 00, MULTOUT = 2400 to 2672 MHz)	$J_{TOL(PP)}$	See Table 5				
Jitter Tolerance (MULTSEL[1:0] = 01, MULTOUT = 1200 to 1336 MHz)	$J_{TOL(PP)}$	See Table 6				
Jitter Tolerance (MULTSEL[1:0] = 10, MULTOUT = 600 to 668 MHz)	$J_{TOL(PP)}$	See Table 7				
Jitter Tolerance (MULTSEL[1:0] = 11, MULTOUT = 150 to 167 MHz)	$J_{TOL(PP)}$	See Table 8				
Jitter Generation (MULTOUT) (MULTSEL[1:0] = 00, MULTOUT = 2400 to 2672 MHz)*	$J_{GEN(rms)}$	Clock Input (MHz) = 600.000 to 668.000	—	TBD	TBD	ps$_{RMS}$
Jitter Generation (MULTOUT) (MULTSEL[1:0] = 01, MULTOUT = 1200 to 1336 MHz)*	$J_{GEN(rms)}$	Clock Input (MHz) = 300.000 to 334.000	—	TBD	TBD	ps$_{RMS}$
		Clock Input (MHz) = 600.000 to 668.000	—	TBD	TBD	ps$_{RMS}$
Jitter Generation (MULTOUT, CLKOUT) (MULTSEL[1:0] = 10, MULTOUT = 600 to 668 MHz)*	$J_{GEN(rms)}$	Clock Input (MHz) = 37.500 to 41.750	—	1.9	TBD	ps$_{RMS}$
		Clock Input (MHz) = 75.000 to 83.500	—	1.2	TBD	ps$_{RMS}$
		Clock Input (MHz) = 150.000 to 167.000	—	0.9	TBD	ps$_{RMS}$
		Clock Input (MHz) = 300.000 to 334.000	—	0.5	TBD	ps$_{RMS}$
		Clock Input (MHz) = 600.000 to 668.000	—	0.5	TBD	ps$_{RMS}$
Jitter Generation (MULTOUT, CLKOUT) (MULTSEL[1:0] = 11, MULTOUT = 150 to 167 MHz)*	$J_{GEN(rms)}$	Clock Input (MHz) = 9.375 to 10.438	—	5.8	TBD	ps$_{RMS}$
		Clock Input (MHz) = 18.750 to 20.875	—	3.2	TBD	ps$_{RMS}$
		Clock Input (MHz) = 37.500 to 41.750	—	2.2	TBD	ps$_{RMS}$
		Clock Input (MHz) = 75.000 to 83.500	—	1.4	TBD	ps$_{RMS}$
		Clock Input (MHz) = 150.000 to 167.000	—	1.3	TBD	ps$_{RMS}$
Jitter Transfer Bandwidth (MULTSEL[1:0] = 00, MULTOUT = 2400 to 2672 MHz)*	J_{BW}	Clock Input (MHz) = 600.000 to 668.000	—	1360	TBD	kHz

*Note: See PLL Performance section of this document for test descriptions.

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Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD} = 2.5 V ± 5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Transfer Bandwidth (MULTSEL[1:0] = 01, MULTOUT = 1200 to 1336 MHz)*	J_{BW}	Clock Input (MHz) = 300.000 to 334.000	—	680	TBD	kHz
		Clock Input (MHz) = 600.000 to 668.000	—	1360	TBD	kHz
Jitter Transfer Bandwidth (MULTSEL[1:0] = 10, MULTOUT = 600 to 668 MHz)*	J_{BW}	Clock Input (MHz) = 37.500 to 41.750	—	85	TBD	kHz
		Clock Input (MHz) = 75.000 to 83.500	—	170	TBD	kHz
		Clock Input (MHz) = 150.000 to 167.000	—	340	TBD	kHz
		Clock Input (MHz) = 300.000 to 334.000	—	680	TBD	kHz
		Clock Input (MHz) = 600.000 to 668.000	—	1360	TBD	kHz
Jitter Transfer Bandwidth (MULTSEL[1:0] = 11, MULTOUT = 150 to 167 MHz)*	J_{BW}	Clock Input (MHz) = 9.375 to 10.438	—	21	TBD	kHz
		Clock Input (MHz) = 18.750 to 20.875	—	43	TBD	kHz
		Clock Input (MHz) = 37.500 to 41.750	—	85	TBD	kHz
		Clock Input (MHz) = 75.000 to 83.500	—	170	TBD	kHz
		Clock Input (MHz) = 150.000 to 167.000	—	340	TBD	kHz
Jitter Transfer Peaking (MULTSEL[1:0] = 00, MULTOUT = 2400 to 2672 MHz)*	J_P	Clock Input (MHz) = 600.000 to 668.000	—	0.03	TBD	dB
Jitter Transfer Peaking (MULTSEL[1:0] = 01, MULTOUT = 1200 to 1336 MHz)*	J_P	Clock Input (MHz) = 300.000 to 334.000	—	0.03	TBD	dB
		Clock Input (MHz) = 600.000 to 668.000	—	0.02	TBD	dB
Jitter Transfer Peaking (MULTSEL[1:0] = 10, MULTOUT = 600 to 668 MHz)*	J_P	Clock Input (MHz) = 37.500 to 41.750	—	0.12	TBD	dB
		Clock Input (MHz) = 75.000 to 83.500	—	0.06	TBD	dB
		Clock Input (MHz) = 150.000 to 167.000	—	0.03	TBD	dB
		Clock Input (MHz) = 300.000 to 334.000	—	0.02	TBD	dB
		Clock Input (MHz) = 600.000 to 668.000	—	0.01	TBD	dB
*Note: See PLL Performance section of this document for test descriptions.						

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Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V$_{DD}$ = 2.5 V ± 5%, T$_A$ = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Transfer Peaking (MULTSEL[1:0] = 11, MULTOUT = 150 to 167 MHz)*	J$_P$	Clock Input (MHz) = 9.375 to 10.438	—	0.12	TBD	dB
		Clock Input (MHz) = 18.750 to 20.875	—	0.06	TBD	dB
		Clock Input (MHz) = 37.500 to 41.750	—	0.03	TBD	dB
		Clock Input (MHz) = 75.000 to 83.500	—	0.02	TBD	dB
		Clock Input (MHz) = 150.000 to 167.000	—	0.01	TBD	dB
Acquisition Time	T$_{AQ}$	After falling edge of PWRDN/CAL	1.45	1.5	1.7	ms
		From the return of valid CLKIN	40	60	150	µs
Frequency Difference at which PLL goes out of Lock (REFCLK compared to the divided down VCO clock)	LOL		TBD	600	TBD	ppm
Frequency Difference at which PLL goes into Lock (REFCLK compared to the divided down VCO clock)	LOCK		TBD	300	TBD	ppm
*Note: See PLL Performance section of this document for test descriptions.						

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**Table 5. Minimum Jitter Tolerance in Nanoseconds* (MULTSEL[1:0] = 00,
MULTOUT = 2400 to 2672 MHz)**

Frequency (Hz)	600-668 MHz Clock Input
< TBD	TBD
TBD	TBD
TBD	TBD
> TBD	TBD
*Note: Measured using sinusoidal jitter at stated Test Condition frequency.	

**Table 6. Minimum Jitter Tolerance in Nanoseconds* (MULTSEL[1:0] = 01,
MULTOUT = 1200 to 1336 MHz)**

Frequency (Hz)	300-334 MHz Clock Input	600-668 MHz Clock Input
< TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
> TBD	TBD	TBD
*Note: Measured using sinusoidal jitter at stated Test Condition frequency.		

**Table 7. Minimum Jitter Tolerance in Nanoseconds* (MULTSEL[1:0] = 10,
MULTOUT = 600 to 668 MHz)**

Frequency (Hz)	37.5–41.75 MHz Clock Input	75–83.5 MHz Clock Input	150-167 MHz Clock Input	300–334 MHz Clock Input	600-668 MHz Clock Input
< 300	25.0	25.0	25.0	25.0	TBD
25K	2.33	4.67	9.33	16.7	TBD
250K	0.67	0.83	1.17	2.17	TBD
> 1M	0.50	0.58	0.67	0.67	TBD
*Note: Measured using sinusoidal jitter at stated Test Condition frequency.					

Table 8. Minimum Jitter Tolerance in Nanoseconds* (MULTSEL[1:0] = 11, MULTOUT = 150 to 167 MHz)

Frequency (Hz)	9.375–10.438 MHz Clock Input	18.75–20.875 MHz Clock Input	37.5–41.75 MHz Clock Input	75–83.5 MHz Clock Input	150-167 MHz Clock Input
< 300	TBD	66.7	66.7	100	TBD
6.5K	TBD	18.0	36.7	66.7	TBD
65K	TBD	3.33	4.67	8.00	TBD
325K	TBD	2.67	2.67	3.33	TBD
> 1M	TBD	2.00	2.33	2.67	TBD
*Note: Measured using sinusoidal jitter at stated Test Condition frequency.					

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.8	V
LVTTL Input Voltage	V_{DIG}	–0.3 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
Lead Temperature (soldering 10 seconds)		300	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ) CLKIN+, CLKIN–, REFCLK+, REFCLK–, All other pins	— —	1 1.5	kV kV
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

Table 10. Thermal Characteristics

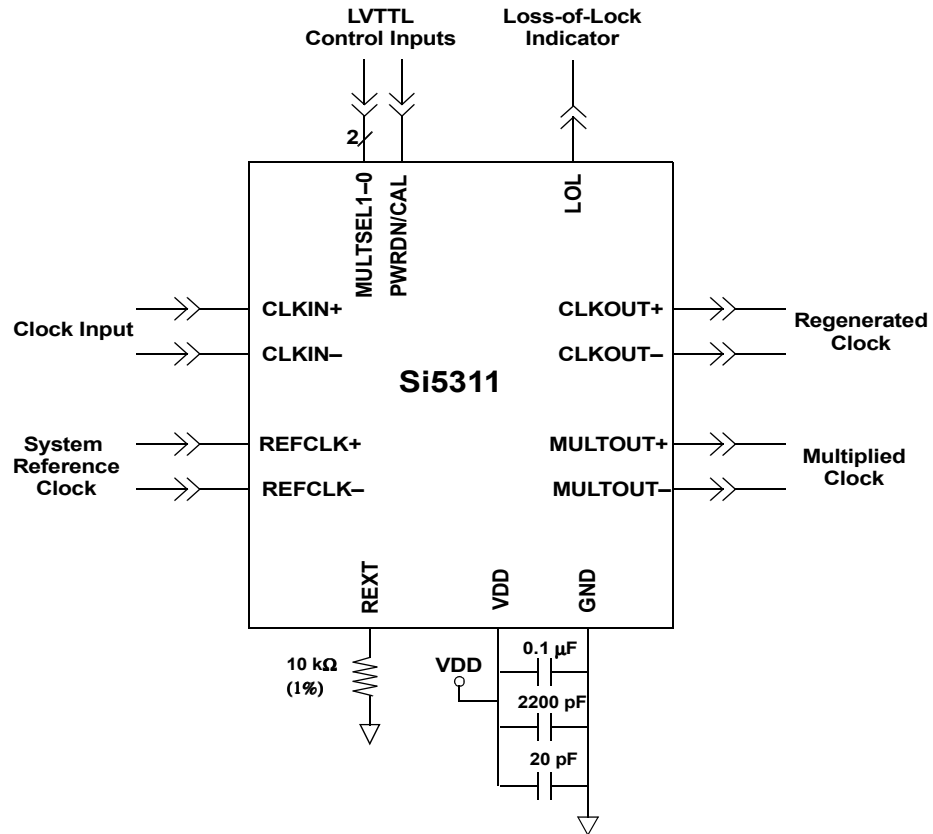| Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

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Figure 5. Si5311 Typical Application Circuit

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Functional Description

The Si5311 is an integrated high speed clock multiplier and clock regenerator device based on Silicon Laboratories DSPLL™ technology. The DSPLL phase locks to the clock input signal (CLKIN) and generates a phase-locked output clock (MULTOUT) at a multiple of the input clock frequency. The MULTOUT output is configured to operate in the 150–167 MHz, the 600–668 MHz, the 1.2–1.33 GHz, or the 2.4–2.67 GHz frequency range using the MULTSEL0 and MULTSEL1 control inputs.

When the device is configured for a MULTOUT output frequency range of 150–167 MHz or 600–668 MHz, the DSPLL is also employed to regenerate an output clock (CLKOUT) that is a jitter-attenuated version of the input clock with clean rising and falling edges. The CLKOUT

output is not characterized for the MULTOUT ranges of 1.2–1.33 GHz or 2.4–2.67 GHz.

A reference clock input signal (REFCLK) is used by the DSPLL as a reference for determination of the PLL lock status. For convenience, REFCLK can be provided at any one of five frequencies, each a multiple of the CLKIN frequency. The REFCLK rate is automatically detected, so no control inputs are needed for configuration. The REFCLK input can be synchronous or asynchronous with respect to the CLKIN input. The operating ranges for the CLKIN, CLKOUT, MULTOUT, and REFCLK signals are indicated in Table 11. Values for typical applications are given in Table 12.

Table 11. CLKIN, CLKOUT, MULTOUT, REFCLK Operating Ranges

MULTSEL [1:0]	CLKIN Range (MHz)	REFCLK = 2^n x CLKIN ±100 ppm (see Note 2)	CLKOUT	MULTOUT
00 (MULTOUT = 2.4–2.7 GHz)	600.00–668.00	n = –6, –5, –4, –3, or –2	See Note 1(a)	4xCLKIN
01 (MULTOUT = 1.2–1.33 GHz)	300.00–334.00	n = –5, –4, –3, –2, or –1	See Note 1(a)	4xCLKIN
	600.00–668.00	n = –6, –5, –4, –3, or –2	See Note 1(a)	2xCLKIN
10 (MULTOUT = 600–668 MHz)	37.500–41.750	n = –2, –1, 0, 1, or 2	1xCLKIN	16xCLKIN
	75.000–83.500	n = –3, –2, –1, 0, or 1	1xCLKIN	8xCLKIN
	150.000–167.000	n = –4, –3, –2, –1, or 0	1xCLKIN	4xCLKIN
	300.000–334.000	n = –5, –4, –3, –2, or –1	1xCLKIN	2xCLKIN
	600.000–668.000	n = –6, –5, –4, –3, or –2	See Note 1(b)	1xCLKIN
11 (MULTOUT = 150–167 MHz)	9.375–10.438	n = 0, 1, 2, 3, or 4	1xCLKIN	16xCLKIN
	18.750–20.875	n = –1, 0, 1, 2, or 3	1xCLKIN	8xCLKIN
	37.500–41.750	n = –2, –1, 0, 1, or 2	1xCLKIN	4xCLKIN
	75.000–83.500	n = –3, –2, –1, 0, or 1	1xCLKIN	2xCLKIN
	150.000–167.000	n = –4, –3, –2, –1, or 0	See Note 1(b)	1xCLKIN

Note:
1. The CLKOUT output is not valid for (a) MULTSEL[1:0] = 00 or MULTOUT[1:0] = 01
  (b) MULTOUT:CLKIN ratios of 1:1 (MULTOUT = 1 x CLKIN.)
2. The REFCLK input can be set to any one of the five CLKIN multiples indicated. The REFCLK input can be asynchronous to the CLKIN input, but must be within ±100 ppm of the stated CLKIN multiple.

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Table 12. Clock Values for Typical Applications

	CLKIN (MHz)	REFCLK Input (MHz)	MULTSEL [1:0]	CLKOUT (MHz)	MULTOUT output (MHz)
SONET/SDH	9.72	9.72	11	9.72	155.52
	19.44	19.44	11	19.44	155.52
	38.88	38.88	10	38.88	622.08
			11	38.88	155.52
	77.76	77.76	10	77.76	622.08
			11	77.76	155.52
	155.52	155.52	10	155.52	622.08
			11	—	155.52
	311.04	9.72, 19.44, 38.88, 77.76, or 155.52	01	—	1244.16
			10	311.04	622.08
	622.08	9.72, 19.44, 38.88, 77.76, or 155.52	00	—	2488.32
			01	—	1244.16
			10	—	622.08
Gigabit Ethernet	9.77	9.77	11	9.77	156.25
	19.53	19.53	11	19.53	156.25
	39.06	39.06	10	39.06	625
			11	39.06	156.25
	78.125	78.125	10	78.125	625
			11	78.125	156.25
	156.25	156.25	10	156.25	625
			11	—	156.25
	312.5	9.77, 19.53, 39.06, 78.125, or 156.25	01	—	1250
			10	312.5	625
	625	9.77, 19.53, 39.06, 78.125, or 156.25	00	—	2500
			01	—	1250
			10	—	625
SONET/SDH FEC (15/14)	10.41	10.41	11	10.41	166.63
	20.83	20.83	11	20.83	166.63
	41.66	41.66	10	41.66	666.51
			11	41.66	166.63
	83.31	83.31	10	83.31	666.51
			11	83.31	166.63
	166.63	166.63	10	166.63	666.51
			11	—	166.63
	333.26	10.41, 20.83, 41.66, 83.31, or 166.63	01	—	1333.03
			10	333.26	666.51
	666.51	10.41, 20.83, 41.66, 83.31, or 166.63	00	—	2666.06
			01	—	1333.03
			10	—	666.51

Si5311

DSPLL™

The PLL structure (shown in Figure 1 on page 4) utilizes Silicon Laboratories' DSPLL technology to produce superior jitter performance while eliminating the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage controlled oscillator (VCO). The technology produces clocks with less jitter than is generated using traditional methods. In addition, because external loop filter components are not required, sensitive noise entry points are eliminated, thus making the DSPLL less susceptible to board-level noise sources.

Clock Multiplier

The DSPLL phase locks to the clock input signal (CLKIN) and generates an output clock (MULTOUT) at a multiple of the input clock frequency. The MULTOUT output is configured to operate in the 150–167 MHz, the 600–668 MHz, the 1.2–1.33 GHz, or the 2.4–2.67 GHz frequency range using the MULTSEL0 and MULTSEL1 control inputs as indicated in Table 11. Values for typical applications are given in Table 12.

The amount of jitter present in the MULTOUT output is a function of the DSPLL jitter transfer function and jitter generation characteristic. Details are provided in the PLL Performance section of this document. (See Figures 6, 7, 8, and 9.) The amount of jitter that the DSPLL can tolerate on the CLKIN input is specified in Tables 5, 6, 7, and 8.

The DSPLL implementation in the Si5311 is insensitive to the duty cycle of the CLKIN input. The MULTOUT output will continue to exhibit a very good duty cycle characteristic even when the CLKIN input duty cycle is degraded.

1x Multiplication

The Si5311 Clock Multiplier function may also be utilized as a 1x multiplier in order to provide jitter attenuation and duty cycle correction without multiplication of the input clock frequency.

Note: When the Si5311 is configured as a 1:1 multiplier, the CLKOUT output is not valid.

Clock Regeneration

When the MULTOUT output is configured to operate in either the 150–167 MHz or the 600–667 MHz range, the Si5311 clock regeneration (CLKOUT output) is also provided. In this case, the DSPLL is used to regenerate

a jitter-attenuated version of the CLKIN input, resulting in a "clean" CLKOUT output with sharp rising and falling edges. The CLKOUT output is a resampled version of the CLKIN input with all CLKOUT transitions occurring synchronously with the rising edges of the MULTOUT output. The rising edges of CLKOUT are insensitive to the location of the falling edges of the CLKIN input. Thus the period of CLKOUT, measured rising edge to rising edge, is not affected by the CLKIN duty cycle or by jitter on the falling edge of CLKIN.

The falling edges of CLKOUT may be affected by the location of the CLKIN falling edges as follows: If the duty cycle error of CLKIN is significant relative to the period of MULTOUT, then

1. The CLKOUT duty cycle may deviate from 50% (the falling edge of CLKOUT will be time quantized to the nearest rising edge of MULTOUT.)

2. Jitter on the falling edges of CLKIN may result in a CLKOUT duty cycle that alternates between two discrete values.

Note: When the Si5310 is configured as a 1:1 multiplier, the CLKOUT output is not valid.

Reference Clock

The reference clock input (REFCLK) is used to center the DSPLL and also to act as a reference for determination of the PLL lock status. REFCLK is a multiple of the CLKIN frequency, and can be provided in any one of five frequency ranges (9.375–10.438 MHz, 18.78–20.875 MHz, 37.500–41.750 MHz, 75.00–83.50 MHz, or 150–167.00 MHz). The REFCLK rate is automatically detected by the Si5311, so no control inputs are needed for REFCLK frequency selection. The REFCLK input may be synchronous or asynchronous with respect to the CLKIN input. The frequency relationship between REFCLK and CLKIN is indicated in Table 11. In many applications, it may be desirable to tie REFCLK and CLKIN together and drive them from the same clock source. The Si5311 is insensitive to the phase relationship between CLKIN and REFCLK, so these differential inputs may be driven in phase or 180° out of phase if this simplifies board layout. Values for typical applications are given in Table 12.

DSPLL Lock Detection (Loss-of-Lock)

The Si5311 provides lock-detect circuitry that indicates whether the DSPLL has frequency locked with the incoming CLKIN signal. The circuit compares the frequency of a divided down version of the multiplier output with the frequency of the supplied reference clock. If the divided multiplier output frequency deviates from that of the reference clock by the amount specified in Table 4 on page 8, the PLL is declared out of lock, and the loss-of-lock (LOL) pin is asserted.

While out of lock, the DSPLL will try to reacquire lock

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with the input clock. During reacquisition, the multiplier output (MULTOUT) will drift over a range of approximately 1% relative to the supplied reference clock. The LOL output will remain asserted until the divided multiplier output frequency differs from the REFCLK frequency by less than the amount specified in Table 4.

Note: LOL is not asserted during PWRDN/CAL.

PLL Performance

The Si5311 DSPLL circuitry is designed to provide low jitter generation, high jitter tolerance, and a well-controlled jitter transfer function with low peaking. Each of these key performance parameters is described more fully in the following sections.

Jitter Tolerance

Jitter tolerance for the Si5311 is defined as the maximum peak-to-peak sinusoidal jitter that can be added to the incoming clock before the PLL exceeds its allowable operating range and loses lock. The tolerance is a function of the jitter frequency, the incoming clock rate, and the MULTSEL0/1 settings.

The jitter tolerance for specified jitter frequencies and input clock rates is given in Tables 5, 6, 7, and 8.

Jitter Transfer

Jitter transfer is defined as the ratio of output signal jitter to input signal jitter for a specified jitter frequency. The jitter transfer characteristic determines the amount of input clock jitter that will be passed on to the Si5311 CLKOUT and MULTOUT outputs. The DSPLL technology used in the Si5311 provides a tightly controlled jitter transfer curve because many of the PLL gain parameters are determined by digital signal processing algorithms which do not vary over supply voltage, process, and temperature. In a system application, a well-controlled transfer curve minimizes the output clock jitter variation from board to board, providing more consistent system level jitter performance.

The jitter transfer characteristic is a function of the MULTSEL0/1 settings and the input clock rate. Higher input clock rates produce higher bandwidth transfer functions with lower jitter peaking. Table 4 gives the 3 dB bandwidth and peaking values for specified input clock rates and MULTSEL0/1 settings. Figures 6, 7, 8, and 9 show a family of jitter transfer curves for different input clock rates.

Jitter Generation

Jitter generation is defined as the amount of jitter produced at the output of the device with a jitter free input clock. Generated jitter arises from sources within the VCO and other PLL components. Jitter generation is a function of MULTSEL0/1 settings and input clock frequency. For clock multiplier applications, the higher

the multiplier ratio desired, the larger the jitter generation. Table 4 gives the jitter generation values for specified MULTSEL0/1 settings and input clock rates.
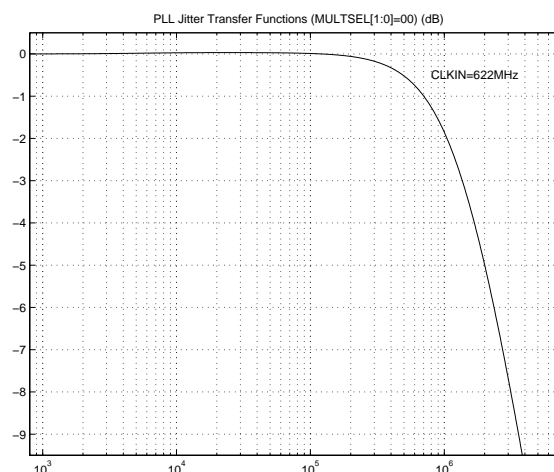

Figure 6. PLL Jitter Transfer Functions, MULTSEL[1:0] = 00 (MULTOUT = 2400–2672 MHz)
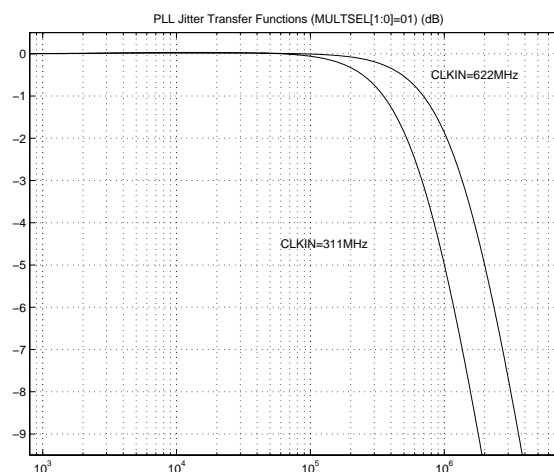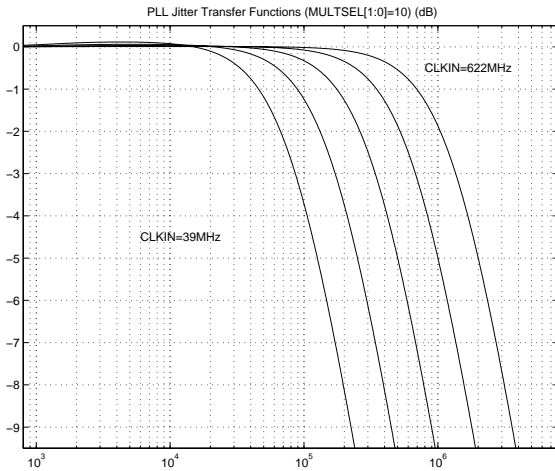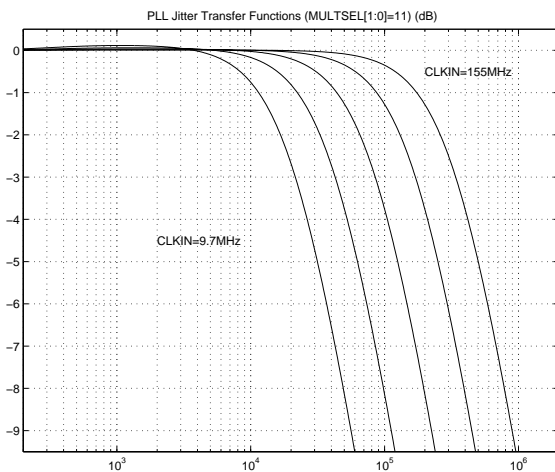

Figure 7. PLL Jitter Transfer Functions, MULTSEL[1:0] = 01 (MULTOUT = 1200–1336 MHz)

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**Figure 8. PLL Jitter Transfer Functions,
MULTSEL[1:0] = 10
(MULTOUT = 600–668 MHz)**

**Figure 9. PLL Jitter Transfer Functions,
MULTSEL[1:0] = 11
(MULTOUT = 150–167 MHz)**

Device Power-Down

The Si5311 PWRDN/CAL input can be used to hold the device in a power-down state when not in use. When the PWRDN/CAL input is asserted (set high), the CLKOUT and MULTOUT output drivers are disabled and the positive and negative terminals of the CLKOUT and MULTOUT outputs are each tied to VDD through 100 Ω on-chip resistors. This feature is useful in reducing power consumption in applications that employ redundant clock sources. When PWRDN/CAL is released (set to low) the digital logic is reset to a known initial condition and the DSPLL circuitry is recalibrated

and will begin to lock to the incoming clock.

PLL Self-Calibration

Si5311 device provides an internal self-calibration function that optimizes the loop gain parameters within the internal DSPLL. Self-calibration is initiated by a high-to-low transition of the PWRDN/CAL signal while a valid reference clock is supplied to the REFCLK input.

For optimal jitter performance, the supply voltage should be stable at 2.5 V ±10% when calibration is initiated. The PWRDN/CAL signal should be held high for at least 1 µS after the supply has stabilized before transitioning low to initiate self-calibration. See Silicon Laboratories application note AN42 for suggested methods of generating the PWRDN/CAL signal for initiation of self-calibration.

Device Grounding

The Si5311 uses the GND pad on the bottom of the 20-pin micro leaded package (MLP) for device ground. This pad should be connected directly to the analog supply ground. See Figures 12 and 13 for the ground (GND) pad location.

Bias Generation Circuitry

The Si5311 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption compared with traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

Differential Input Circuitry

The Si5311 provides differential inputs for both the input clock (CLKIN) and the reference clock (REFCLK) inputs. An example termination for these inputs is shown in Figure 10. In applications where direct dc coupling is possible, the 0.1 µF capacitors may be omitted. The CLKIN and REFCLK input amplifiers require input signals with minimum differential peak-to-peak voltages as specified in Table 2 on page 6.

Differential Output Circuitry

The Si5311 utilizes a current mode logic (CML) architecture to output both the regenerated clock (CLKOUT) and the multiplied clock (MULTOUT). An example of output termination with ac coupling is shown in Figure 11. For applications in which direct dc coupling is possible, the 0.1 µF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML is listed in Table 2 on page 6.
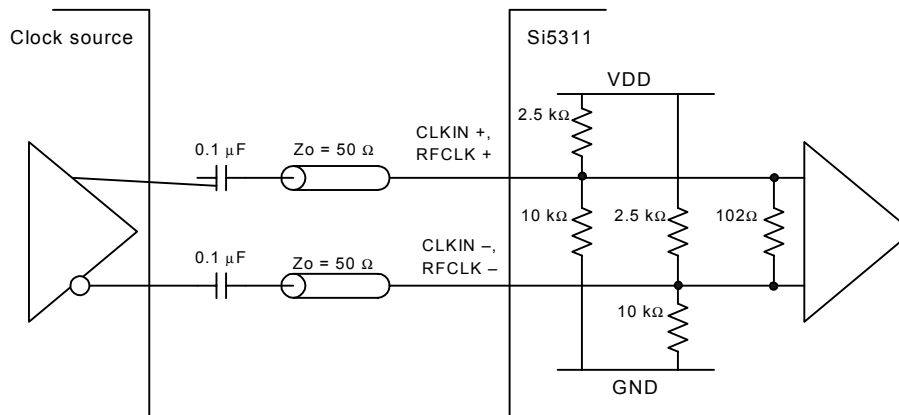
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Figure 10. Input Termination for CLKIN and REFCLK (AC Coupled)
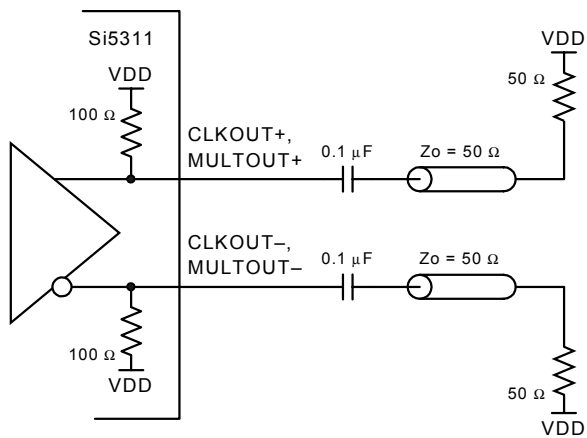
Figure 11. Output Termination for CLKOUT and MULTOUT (AC Coupled)

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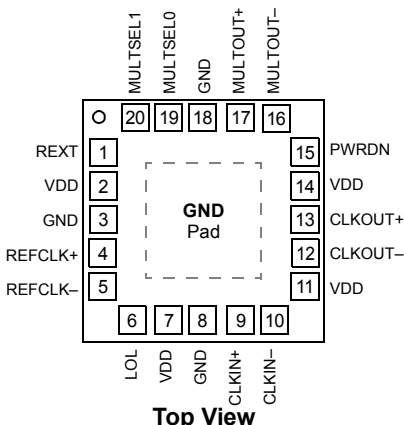
Si5311

Pin Descriptions: Si5311

Figure 12. Si5311 Pin Configuration

Table 13. Si5311 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	REXT			**External Bias Resistor.** This resistor is used by onboard circuitry to establish bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.
2, 7, 11, 14	VDD		2.5 V	**Supply Voltage.** Nominally 2.5 V.
3, 8, 18, and GND Pad	GND		GND	**Supply Ground.** Nominally 0.0 V. The GND pad found on the bottom of the 20-pin micro leaded package (see Figure 13) must be connected directly to supply ground.
4, 5	REFCLK+, REFCLK–	I	See Table 2	**Differential Reference Clock.** The reference clock sets the initial operating frequency used by the onboard PLL for clock regeneration and multiplication. Additionally, the reference clock is used as a reference in generation of the LOL output and to bound the frequency drift of MULTOUT when CLKIN is not present.
6	LOL	O	LVTTL	**Loss of Lock.** This output is driven high when a divided version of the clock multiplier output deviates from the reference clock frequency by the amount specified in Table 4 on page 8.
9, 10	CLKIN+, CLKIN–	I	See Table 2	**Differential Clock Input.** Differential input clock from which MULTOUT is derived.

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Table 13. Si5311 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
12, 13	CLKOUT–, CLKOUT+	O	CML	**Differential Clock Output.** The clock output signal is a regenerated version of the input clock signal present on CLKIN. It is phase aligned with MULTOUT and is updated on the rising edge of MULTOUT. Notes:The CLKOUT output is not valid for MULTSEL[1:0] = 00 or MULTSEL[1:0] = 01. The CLKOUT output is also not valid for MULTOUT:CLKIN ratios of 1:1 (MULTOUT = 1x CLKIN). Connection of an improperly terminated transmission line to the CLKOUT output can cause reflections that may adversely affect the performance of the MULTOUT output. If the CLKOUT output is not used, these pins should be either tied to V_{DD} (recommended), left unconnected, or connected to a properly terminated transmission line.
15	PWRDN/CAL	I	LVTTL	**Power Down.** To shut down the high-speed outputs and reduce power consumption, hold this pin high. For normal operation, hold this pin low. **Calibration.** To initiate an internal self-calibration, force a high-to-low transition on this pin. (See "PLL Self-Calibration," on page 18.) **Note:** This input has a weak internal pulldown.
16, 17	MULTOUT–, MULTOUT+	O	CML	**Differential Multiplier Output.** The multiplier output is generated from the signal present on CLKIN. In the absence of CLKIN, the REFCLK is used to bound the frequency of MULTOUT according to Table 4 on page 8. **Note:** Connection of an improperly terminated transmission line to the MULTOUT output can cause reflections that may adversely affect the CLKOUT output. If the MULTOUT output is not used, these pins should be either tied to V_{DD} (recommended), left unconnected, or connected to a properly terminated transmission line.
19	MULTSEL1, MULTSEL0	I	LVTTL	**Multiplier Rate Select.** These pins configure the onboard PLL-based clock multiplier for clock generation at one of four user selectable clock rates. **Note:** These inputs have weak internal pulldowns.
20	NC			**No Connect.** This pin should be tied to ground.

Ordering Guide

Table 14. Ordering Guide

Part Number	Package	Temperature
Si5311-BM	20-pin MLP	–40°C to 85°C

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Package Outline

Figure 13 illustrates the package details for the Si5311. Table 15 lists the values for the dimensions shown in the illustration.
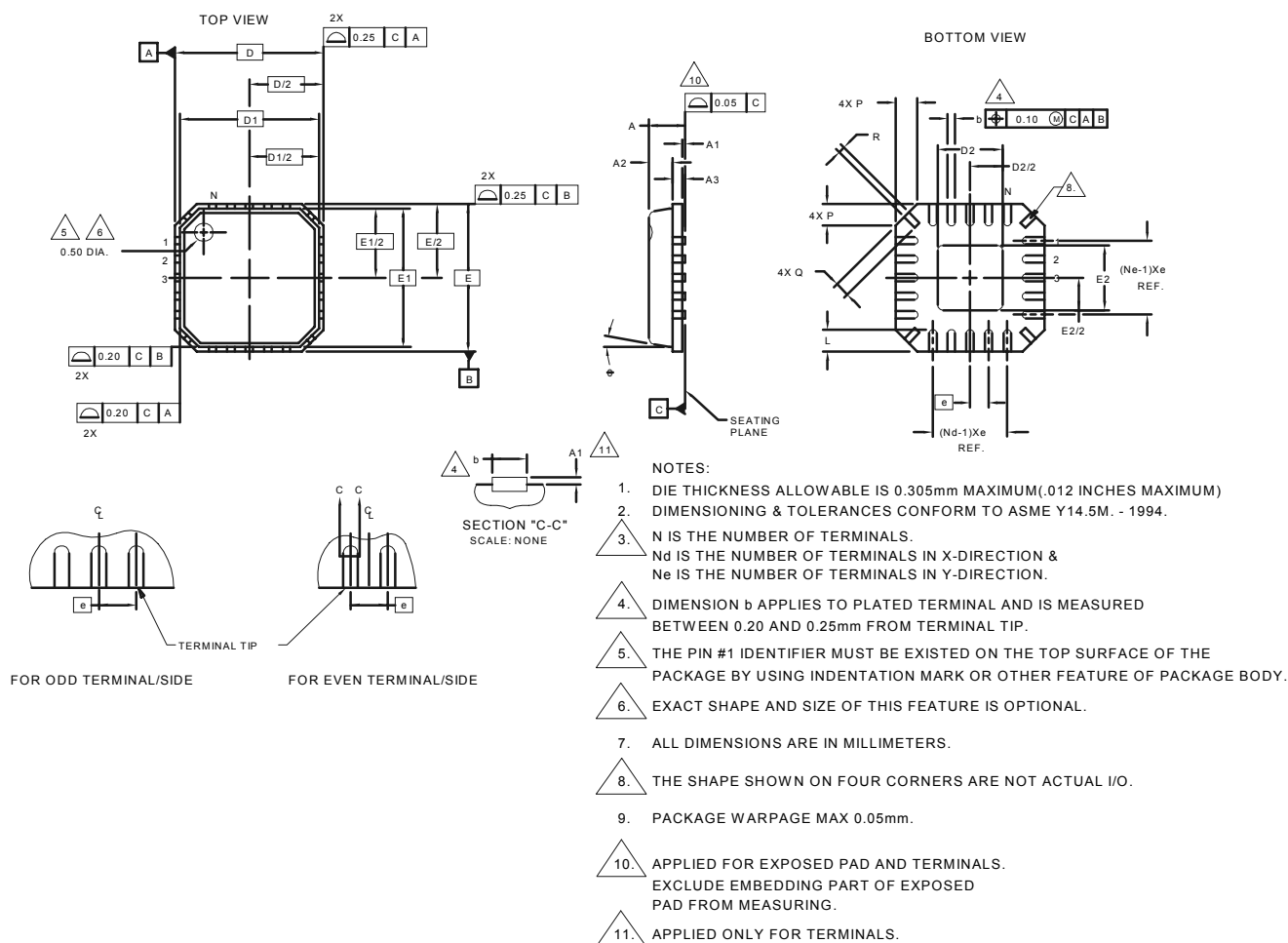

Figure 13. 20-pin Micro Leaded Package (MLP)

Table 15. Package Diagram Dimensions

Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	—	0.85	1.00	E1	3.75 BSC		
A1	0.00	0.01	0.05	E2	1.95	2.10	2.25
A2	—	0.65	0.80	N	20		
A3	0.20 REF			Nd	5		
b	0.18	—	0.30	Ne	5		
D	4.00 BSC			L	0.50	0.60	0.75
D1	3.75 BSC			P	0.24	0.42	0.60
D2	1.95	2.10	2.25	Q	0.30	0.40	0.65
e	0.50 BSC			R	0.13	0.17	0.23
E	4.00 BSC			θ	—	—	12°

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