Si5600

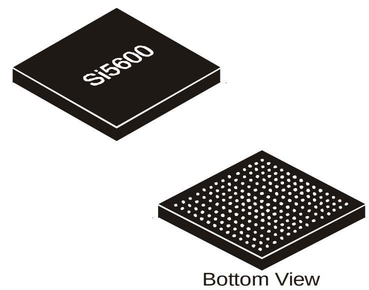
PRELIMINARY DATA SHEET

SiPHY™ OC-192/STM-64 SONET/SDH TRANSCEIVER

Features

Complete low power, high speed, SONET/SDH transceiver with integrated limiting amp, CDR, CMU, and MUX/DEMUX

- Data Rates Supported: OC-192/ STM-64, 10GbE, and 10.7 Gbps FEC
- Low Power Operation 1.2 W (typ)
- DSPLL™ Based Clock Multiplier Unit w/ Selectable Loop Filter Bandwidths
- Integrated Limiting Amplifier
- Loss-of-Signal (LOS) Alarm
- Diagnostic and Line Loopbacks
- SONET Compliant Loop Timed Operation
- Programmable Slicing Level and Sample Phase Adjustment
- SFI-4 Compliant Low Speed Interface
- Single Supply 1.8 V Operation
- 15 x 15 mm BGA Package



Ordering Information:

See page 25.

Applications

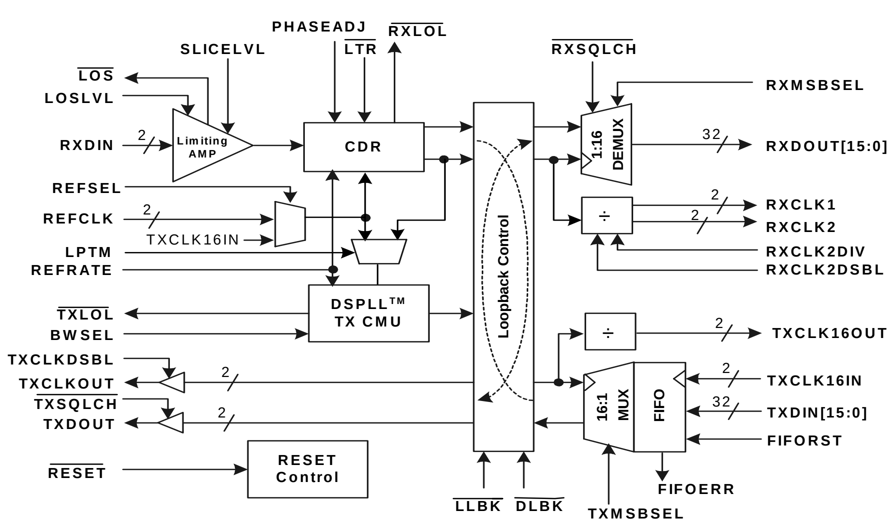
- Sonet/SDH Transmission Systems
- Optical Transceiver Modules
- Sonet/SDH Test Equipment

Description

The Si5600 is a complete low-power transceiver for high-speed serial communication systems operating between 9.9 Gbps and 10.7 Gbps. The receive path consists of a fully integrated limiting amplifier, clock and data recovery unit (CDR), and 1:16 deserializer. The transmit path combines a low jitter clock multiplier unit (CMU) with a 16:1 serializer. The CMU uses Silicon Laboratories' DSPLL™ technology to provide superior jitter performance while reducing design complexity by eliminating external loop filter components. To simplify BER optimization in long haul applications, programmable slicing, and sample phase adjustment are supported.

The Si5600 operates from a single 1.8 V supply over the industrial temperature range (–40°C to 85°C).

Functional Block Diagram



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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A		–40	25	85	°C
LVTTL Output Supply Voltage	V_{DD33}		1.71	—	3.47	V
Si5600 Supply Voltage	V_{DD}		1.71	1.8	1.89	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.

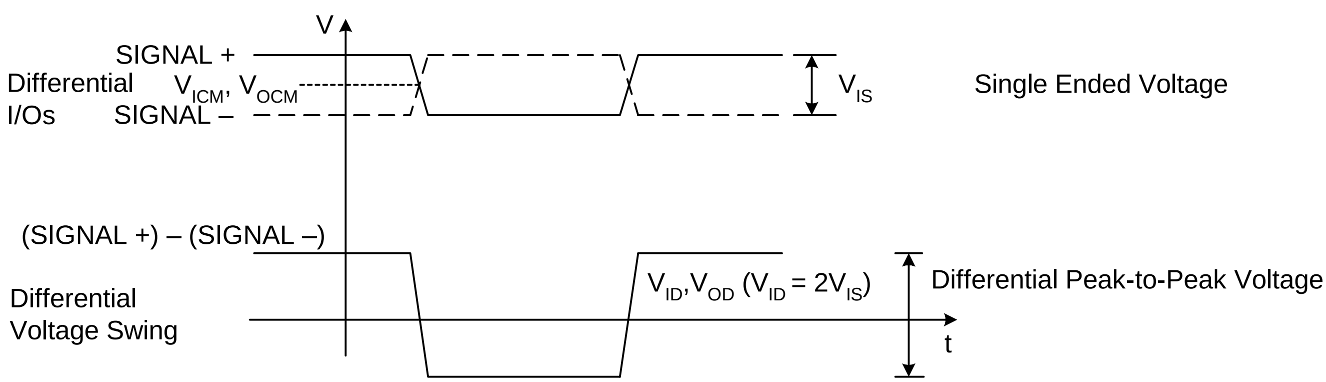

Figure 1. Differential Voltage Measurement (RXDIN, RXDOUT, RXCLK1, RXCLK2, TXDIN, TXDOUT, TXCLKOUT, TXCLK16OUT, TXCLK16IN)

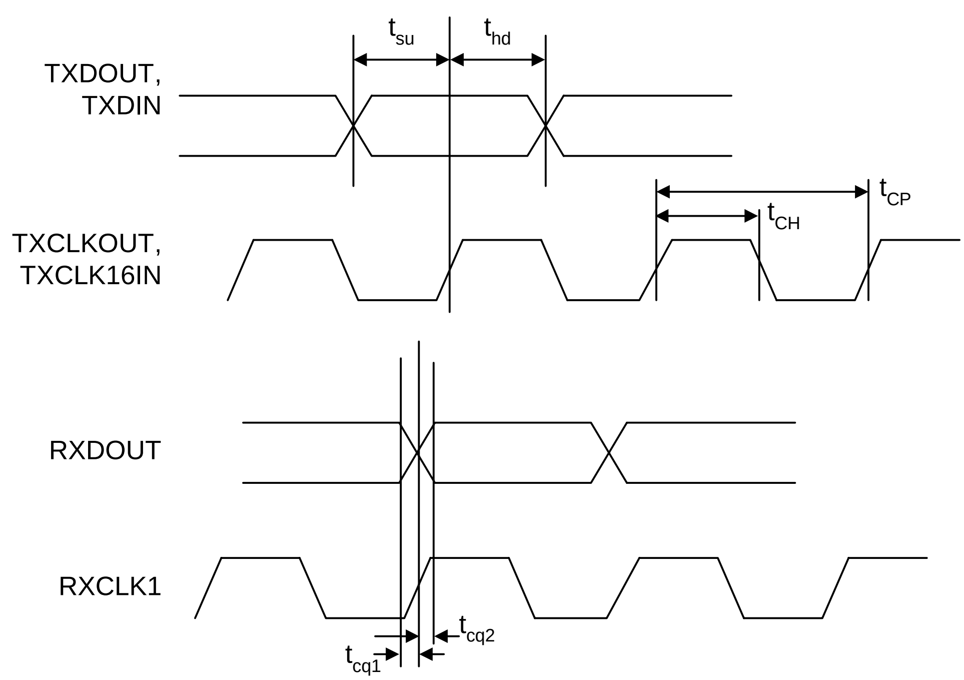

Figure 2. Data to Clock Delay

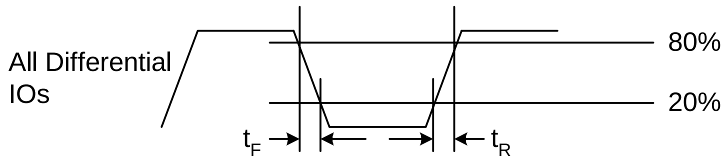

Figure 3. Rise/Fall Time Measurement

Table 2. DC Characteristics

(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	611	TBD	mA
Power Dissipation	P_D		—	1.2	TBD	W
Voltage Reference (VREF)	V_{REF}	VREF driving 10 kΩ load	1.21	1.25	1.29	V
Common Mode Input Voltage (RXDIN)	V_{ICM}		TBD	0.1	TBD	V
Differential Input Voltage Swing (RXDIN)	V_{ID}	See Figure 1	20	—	1.0	mV (pk-pk)
Common Mode Output Voltage (TXDOUT, TXCLKOUT)	V_{OCM}		.8	0.9	1.0	V
Differential Output Voltage Swing (TXDOUT, TXCLKOUT), Differential pk-pk	V_{OD}	See Figure 1	800	1000	1200	mV (pk-pk)
LVPECL Input Voltage HIGH (REFCLK)	V_{IH}		1.975	2.3	2.59	V
LVPECL Input Voltage LOW (REFCLK)	V_{IL}		1.32	1.6	1.99	V
LVPECL Input Voltage Swing, Differential pk-pk (REFCLK)	V_{ID}	Figure 1	250	—	2400	mV (pk-pk)
LVPECL Internally Generated Input Bias (REFCLK)	V_{IB}		1.6	1.95	2.3	V
LVDS Input High Voltage (TXDIN, TXCLK16IN)	V_{IH}		—	—	2.4	V
LVDS Input Low Voltage (TXDIN, TXCLK16IN)	V_{IL}		0.0	—	—	V
LVDS Input Voltage, Single Ended pk-pk (TXDIN, TXCLK16IN)	V_{ISE}		100	—	600	mV (pk-pk)
LVDS Output High Voltage (RXDOUT, RXCLK1, RXCLK2, TXCLK16OUT)	V_{OH1}	100 Ω Load Line-to-Line	TBD	—	1.475	mV
LVDS Output Low Voltage (RXDOUT, RXCLK1, RXCLK2, TXCLK16OUT)	V_{OL1}	100 Ω Load Line-to-Line	0.925	—	TBD	V
LVDS Output Voltage, Differential pk-pk (RXDOUT, RXCLK1, RXCLK2, TXCLK16OUT)	V_{OSE}	100 Ω Load Line-to-Line, Figure 1	500	—	800	mV (pk-pk)

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVDS Common Mode Voltage (RXDOUT, RXCLK1, RXCLK2, TXCLK16OUT)	V_{CM}		1.125	—	1.275	V
Input Impedance (TXDIN, TXCLK16IN, REFCLK, RXDIN)	R_{IN}	Each input to common mode	42	50	58	Ω
Output Short to GND (RXDOUT, RXCLK1, RXCLK2, TXCLK16OUT, TXDOUT, TXCLKOUT)	$I_{SC(–)}$		—	25	TBD	mA
Output Short to V_{DD} (RXDOUT, RXCLK1, RXCLK2, TXCLK16OUT, TXDOUT, TXCLKOUT)	$I_{SC(+)}$		TBD	–100	—	µA
LVTTL Input Voltage Low (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET, TXCLKDSBL, FIFORST, TXSQLCH, BWSEL, TXMSBSEL, DLBK, LLBK, LPTM)	V_{IL2}	VDD33 = 3.3 V	—	—	0.8	V
		VDD33 = 1.8 V	—	—	0.7	
LVTTL Input Voltage High (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET, TXCLKDSBL, FIFORST, TXSQLCH, BWSEL, TXMSBSEL, DLBK, LLBK, LPTM)	V_{IH2}	VDD33 = 3.3 V	2.0	—	—	V
		VDD33 = 1.8 V	1.7			
LVTTL Input Low Current (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET, TXCLKDSBL, FIFORST, TXSQLCH, BWSEL, TXMSBSEL, DLBK, LLBK, LPTM)	I_{IL}		—	—	10	µA
LVTTL Input High Current (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET, TXCLKDSBL, FIFORST, TXSQLCH, BWSEL, TXMSBSEL, DLBK, LLBK, LPTM)	I_{IH}		—	—	10	µA
LVTTL Input Impedance (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET, TXCLKDSBL, FIFORST, TXSQLCH, BWSEL, TXMSBSEL, DLBK, LLBK, LPTM)	R_{IN}		10	—	—	kΩ
LVTTL Output Voltage Low (LOS, RXLOL, FIFOERR, TXLOL)	V_{OL2}	VDD33 = 1.8 V	—	—	0.4	V
		VDD33 = 3.3 V	—	—	0.4	
LVTTL Output Voltage High (LOS, RXLOL, FIFOERR, TXLOL)	V_{OH2}	VDD33 = 1.8 V	1.4	—	—	V
		VDD33 = 3.3 V	2.4	—	—	

Table 3. AC Characteristics (RXDIN, RXDOUT, RXCLK1, RXCLK2)

(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clock Frequency (RXCLK1)	f_{clkout}		—	622	667	MHz
Duty Cycle (RXCLK1, RXCLK2)		tch/tcp, Figure 2	45	—	55	%
Output Rise and Fall Times (RXCLK1, RXCLK2,RXDOUT)	t_R,t_F	Figure 3	—	50	—	ps
Data Invalid Prior to RXCLK1	t_{cq1}	Figure 2	—	—	200	ps
Data Invalid After RXCLK1	t_{cq2}	Figure 2	—	—	200	ps
Input Return Loss (RXIN)		400 kHz–10.0 GHz 10.0 GHz–16.0 GHz	18.7 TBD	— —	— —	dB dB
Slicing Adjust Dynamic Range		SLICELVL = 200–800 mV	–20	—	20	mV
Slicing Level Offset[1] (referred to RXDIN)		SLICELVL = 200–800 mV	–500	—	500	µV
Slicing Level Accuracy		VSLICE	–5	—	5	%
Sampling Phase Adjustment[2]		PHASEADJ = 200–800 mV	–45°	—	45°	
LOS Threshold Dynamic Range		LOSLVL = 200–800 mV	10	—	50	mV pk-pk
LOS Threshold Offset[3] (referred to RXDIN)		LOSLVL = 200–800 mV	–500	—	500	µV
LOS Threshold Accuracy		VLOS	–5	—	5	%

Note:
1. Slice level (referred to RXDIN) is calculated as follows: VSLICE = (SLICE_LVL – 0.4 • VREF)/15.
2. Sample Phase Offset is calculated as follows: PHASE OFFSET = 45° (PHASEADJ – 0.4 • VREF)/0.3
3. LOS Threshold voltage (referred to RXDIN) is calculated as follows: VLOS = 30 mV + (LOS_LVL – 0.4 • VREF)/15.

Table 4. AC Characteristics (TXCLK16OUT, TXCLK16IN, TXCLKOUT, TXDIN, TXDOUT)
(V_{DD} = 1.8 V ± 5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TXCLKOUT Frequency	f_{clkout}		—	9.95	10.7	GHz
TXCLKOUT Duty Cycle		tch/tcp, Figure 2	45	—	55	%
Output Rise Time (TXCLKOUT, TXDOUT)	t_R	Figure 3	—	25	—	ps
Output Fall Time (TXCLKOUT, TXDOUT)	t_F	Figure 3	—	25	—	ps
TXCLKOUT Setup to TXDOUT	t_{su}	Figure 2	25	—	—	ps
TXCLKOUT Hold From TXDOUT	t_{hd}	Figure 2	25	—	—	ps
Output Return Loss		400 kHz–10 GHz 10 GHz–16 GHz	TBD TBD	— —	— —	dB dB
TXCLK16OUT Frequency	f_{CLKIN}		—	622	667	MHz
TXCLK16OUT Duty Cycle		tch/tcp, Figure 2	40	—	60	%
TXCLK16OUT Rise & Fall Times	t_R,t_F		100	—	300	ps
TXDIN Setup to TXCLK16IN	t_{DSIN}		—	—	300	ps
TXDIN Hold from TXCLK16IN	t_{DHIN}		—	—	300	ps
TXCLK16IN Frequency	f_{CLKIN}		—	622	667	MHz
TXCLK16IN Duty Cycle		tch/tcp, Figure 2	40	—	60	%
TXCLK16IN Rise & Fall Times	t_R,t_F		100	—	300	ps

Table 5. AC Characteristics (Receiver PLL)
(V_{DD} = 1.8 V ± 5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance	$J_{TOL(PP)}$	f = 2.4 kHz	15	30	—	UIpp
		f = 24 kHz	1.5	3.0	—	UIpp
		f = 400 kHz	1.5	3.0	—	UIpp
		f = 4 MHz	0.15	0.3	—	UIpp
Acquisition Time	T_{AQ}		—	—	20	µs
Input Reference Clock Frequency	RC_{FREQ}	REFRATE = 1	—	622	667	MHz
		REFRATE = 0	—	155	167	MHz
Reference Clock Duty Cycle	RC_{DUTY}		40	50	60	%
Reference Clock Frequency Tolerance	RC_{TOL}		–100	—	100	ppm
Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock)	LOL		TBD	600	1000	ppm
Frequency Difference at which Receive PLL goes into Lock (REFCLK compared to the divided down VCO clock)	LOCK		TBD	300	TBD	ppm
Note: Bellcore specifications: GR-1377-CORE, Issue 5, December 1998.						

Table 6. AC Characteristics (Transmitter Clock Multiplier Characteristics)

(V_{DD} = 1.8 V ± 5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Generation—Deterministic	$J_{DET(PP)}$	PRBS 23	—	0.020	TBD	UI_{PP}
Jitter Generation—Random	$J_{GEN(RMS)}$		—	0.005	TBD	UI_{RMS}
Jitter Transfer Bandwidth	J_{BW}	BWSEL = 0	—	—	12	kHz
		BWSEL = 1	—	—	50	kHz
Jitter Transfer Peaking			—	0.05	0.1	dB
Acquisition Time	T_{AQ}	Valid REFCLK	—	15	20	mS
Input Reference Clock Frequency	RC_{FREQ}	REFRATE = 1	—	622	667	MHz
		REFRATE = 0	—	155	167	MHz
Input Reference Clock Duty Cycle	RC_{DUTY}		40	—	60	%
Input Reference Clock Frequency Tolerance	RC_{TOL}		–100	—	100	ppm

Note: Bellcore specifications: GR-1377-CORE, Issue 5, December 1998.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to TBD	V
LVTTL Input Voltage	V_{DD33}	–0.5 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any Output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
Package Temperature (soldering 10 seconds)		275	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		TBD	V

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

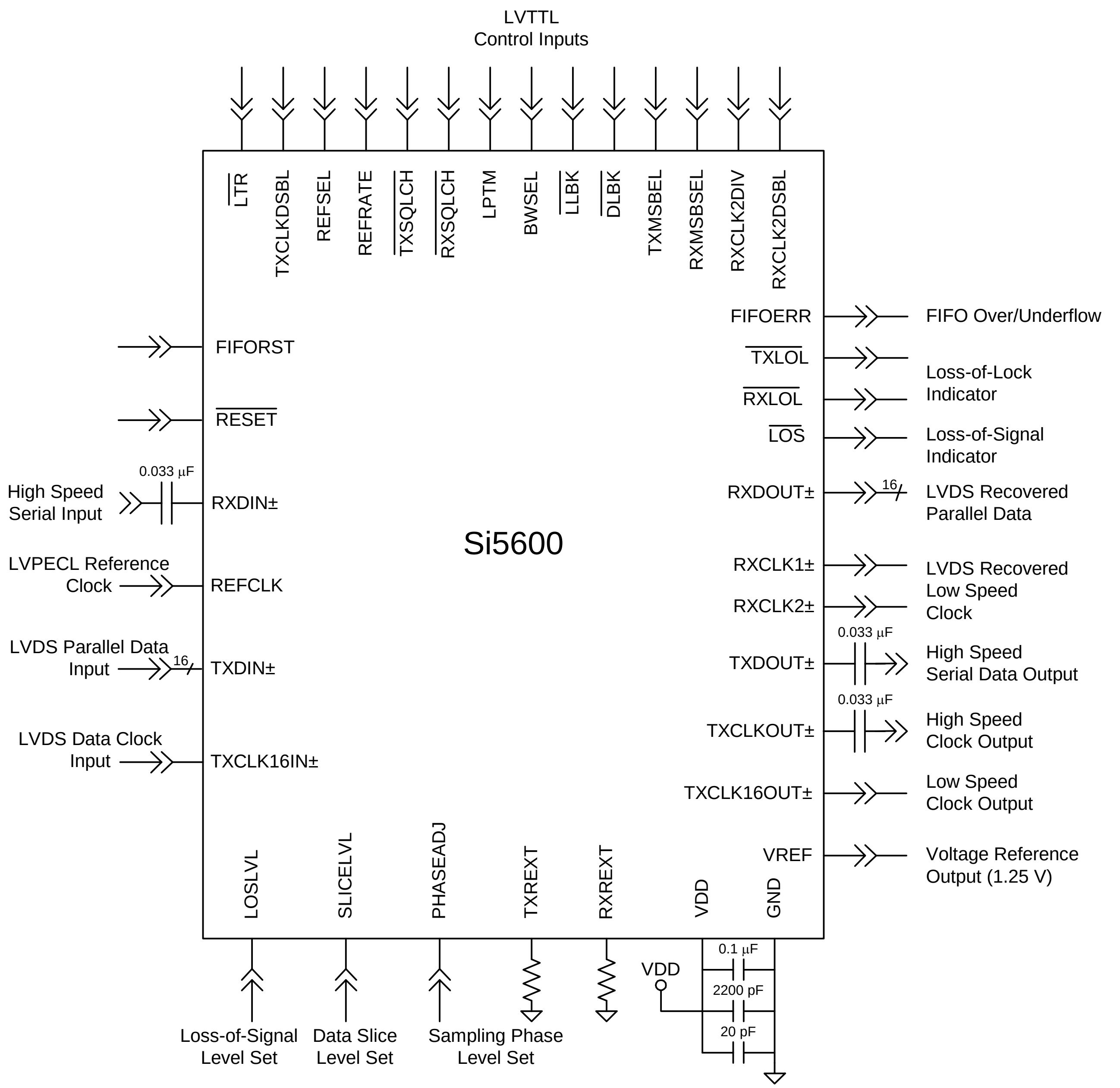

Figure 4. Si5600 Typical Application Circuit

Functional Description

The Si5600 transceiver is a low power, fully integrated serializer/deserializer that provides significant margin to all SONET/SDH jitter specifications. The device operates from 9.9–10.7 Gbps making it suitable for OC-192/STM-64, 10GbE, and OC-192/STM-64 applications that use 15/14 forward error correction (FEC) coding. The low speed receive/transmit interface uses LVDS I/Os that are compliant to the Optical Interface Forum's SFI-4 standard.

Receiver

The receiver within the Si5600 includes a precision limiting amplifier, high jitter tolerance clock and data recovery unit (CDR), and 1:16 demultiplexer. In addition, programmable data slicing and sampling phase adjustment are provided to support bit-error-rate (BER) optimization for long haul applications.

Limiting Amplifier

The Si5600 incorporates a high sensitivity limiting amplifier with sufficient gain to directly accept the output of transimpedance amplifiers. High sensitivity is achieved by using a digital calibration algorithm to cancel out amplifier offsets. This algorithm achieves superior offset cancellation by using statistical averaging to remove noise that may degrade more traditional calibration routines.

The limiting amplifier provides sufficient gain to fully saturate with input signals that are less than 20 mV peak-to-peak differential. In addition, input signals that exceed 1 V peak-to-peak differential will not cause any performance degradation.

Loss-of-Signal (LOS) Detection

The limiting amplifier includes circuitry that generates a loss-of-signal (LOS) alarm when the input signal amplitude on RXDIN falls below an externally controlled threshold. The Si5600 can be configured to drive the $\overline{\text{LOS}}$ output low when the differential input amplitude drops below a threshold set between ~10 mV and 50 mV pk-pk differential. Approximately 3 dB of hysteresis prevents unnecessary switching on $\overline{\text{LOS}}$.

The LOS threshold is set by applying a voltage between 0.20 V and 0.80 V to the LOSLVL input. The voltage present on LOSLVL maps to an input signal threshold as follows:

$$V_{LOS} = \frac{(V_{LOSLVL} - 0.4\text{xVREF})}{15} + 30\text{ mV}$$

V_{LOS} is the differential pk-pk LOS threshold referred to the RXDIN input, V_{LOSLVL} is the voltage applied to the LOSLVL pin, and VREF is reference voltage output on the VREF pin.

The LOS detection circuitry is disabled by tieing the LOSLVL input to the supply (VDD). This forces the $\overline{\text{LOS}}$ output high.

Slicing Level Adjustment

To support applications that require BER optimization, the limiting amplifier provides circuitry that supports adjustment of the 0/1 decision threshold (slicing level) over a range of ±20 mV when referred to the internally biased RXDIN input. The slicing level is set by applying a voltage between 0.20 V and 0.80 V to the SLICELVL input. The voltage present on SLICELVL sets the slicing level as follows:

$$V_{LEVEL} = \frac{(V_{SLICE} - 0.4\text{xVREF})}{15}$$

V_{LEVEL} is the slicing level referred to the RXDIN input, V_{SLICE} is the voltage applied to the SLICE_LVL pin, and VREF is reference voltage output on the VREF pin.

The slicing level adjustment may be disabled by tieing the SLCLVL input to the supply (VDD). When slicing is disabled, the slicing offset is set to 0.0 V relative to internally biased input common mode voltage for RXDIN.

Clock and Data Recovery (CDR)

The Si5600 uses an integrated CDR to recover clock and data from a non-return to zero (NRZ) signal input on RXDIN. The recovered data clock is used to regenerate the incoming data by sampling the output of the limiting amplifier at the center of the NRZ bit period. The recovered clock and data is then deserialized by a 1:16 demultiplexer and output via a LVDS compatible low speed interface (RXDOUT[15:0], RXCLK1, and RXCLK2).

Sample Phase Adjustment

In applications where it is not desirable to recover data by sampling in the center of the data eye, the Si5600 supports adjustment of the CDR sampling phase across the NRZ data period. When sample phase adjustment is enabled, the sampling instant used for data recovery can be moved over a range of ±45° relative to the center of the incoming NRZ bit period. Adjustment of the sampling phase is desirable when data eye distortions are introduced by the transmission medium.

The sample phase is set by applying a voltage between 0.20 V and 0.80 V to the PHASEADJ input. The voltage present on PHASEADJ maps to sample phase offset as follows:

$$\text{Phase Offset} = \frac{45° x (V_{PHASE} - 0.4xVREF)}{0.30}$$

Phase Offset is the sampling offset in degrees from the center of the data eye, V_{PHASE} is the voltage applied to the PHASEADJ pin, and VREF is reference voltage output on the VREF pin. A positive phase offset will adjust the sampling point to lead the default sampling point in the center of the data eye, and a negative phase offset will adjust the sampling point to lag the default sampling point.

Data recovery using a sampling phase offset is disabled by tieing the PHASEADJ input to the supply (VDD). This forces a phase offset of 0° to be used for data recovery.

Lock Detect

The Si5600 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. This circuit compares the frequency of a divided down version of the recovered clock with the frequency of the supplied reference clock (REFCLK). If the recovered clock frequency deviates from that of the reference clock by the amount specified in Table 5 on page 9, the PLL is declared out of lock, and the loss-of-lock ($\overline{\text{RXLOL}}$) pin is asserted. In this state, the PLL will try to reacquire lock with the incoming data stream. During reacquisition, the recovered clock frequency (RXCLK1 and RXCLK2) will drift over a ±1000 ppm range relative to the supplied reference clock. The $\overline{\text{RXLOL}}$ output will remain asserted until the recovered clock frequency is within the REFCLK frequency by the amount specified in Table 5 on page 9.

Lock-to-Reference

In applications where it is desirable to maintain a stable output clock during an alarm condition like loss-of-signal, the lock-to-reference input ($\overline{\text{LTR}}$) can be used to force a stable output clock. When $\overline{\text{LTR}}$ is asserted, the CDR is prevented from acquiring the data signal and the CDR will lock the RXCLKOUT1 and RXCLKOUT2 outputs to the provided REFCLK. In typical applications, the $\overline{\text{LOS}}$ output would be tied to the $\overline{\text{LTR}}$ input to force a stable output clock.

Deserialization

The Si5600 uses a 1:16 demultiplexer to deserialize the high speed input. The deserialized data is output on a 16-bit parallel data bus RXDOUT[15:0] synchronous with the rising edge of RXCLK1. This clock output is derived by dividing down the recovered clock by a factor of 16.

Serial Input to Parallel Output Relationship

The Si5600 provides the capability to select the order in which the received serial data is mapped to the parallel output bus RXDOUT[15:0]. The mapping of the receive bits to the output data word is controlled by the RXMSBSEL input. If RXMSBSEL is tied low, the first bit received is output on RXDOUT0 and the following bits are output in order on RXDOUT1 through RXDOUT15. If RXMSBSEL is tied high, the first bit received is output on RXDOUT15, and the following bits are output in order on RXDOUT14 through RXDOUT0.

Auxiliary Clock Output

To support the widest range of system timing configurations, a second clock output is provided on RXCLK2. This output can be configured to provide a clock that is a 1/16th or 1/64th submultiple of the high speed recovered clock. The divide factor used to generate RXCLK2 is controlled via the RXCLKDIV2 input as described in "Pin Descriptions: Si5600," on page 19. In applications which do not use RXCLK2, this output can be powered down by forcing the RSCLK2DSBL input high.

Data Squelch

During some system error conditions, such as LOS, it may be desirable to force the receive data output to 0 in order to avoid propagation of erroneous data into the downstream electronics. In these applications, the Si5600 provides a data squelching control input, $\overline{\text{RXSQLCH}}$. When this input is active low, the data on RXDOUT will be forced to 0. Data squelch is disabled if the device is operating in diagnostic loopback mode ($\overline{\text{DLBK}}$ = 0).

Transmitter

The transmitter consists of a low jitter, clock multiplier unit (CMU) with a 16:1 serializer. The CMU uses a phase-locked loop (PLL) architecture based on Silicon Laboratories' proprietary DSPLL™ technology. This technology is used to generate ultra-low jitter clock and data outputs that provide significant margin to the SONET/SDH specifications. The DSPLL architecture also utilizes a digitally implemented loop filter that eliminates the need for external loop filter components. As a result, sensitive noise coupling nodes that typically cause degraded jitter performance in crowded PCB environments are removed.

The DSPLL™ also reduces the complexity and performance requirements of reference clock distribution strategies for OC-192/STM-64 optical port cards. This is possible because the DSPLL provides selectable wideband and narrowband loop filter settings that allow the user to set the jitter attenuation characteristics of the CMU to accommodate reference clock sources that have a high jitter content. Unlike traditional analog PLL implementations, the loop filter bandwidth is controlled by a digital filter inside the DSPLL and can be changed without any modification to external components.

DSPLL™ Clock Multiplier Unit

The Si5600's clock multiplier unit (CMU) uses Silicon Laboratories' proprietary DSPLL technology to generate a low jitter, high frequency clock source capable of producing a high speed serial clock and data output with significant margin to the SONET/SDH specifications. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage controlled oscillator (VCO). Because external loop filter components are not required, sensitive noise entry points are eliminated, thus making the DSPLL less susceptible to board-level noise sources. Therefore, SONET/SDH jitter compliance is easier to attain in the application.

Programmable Loop Filter Bandwidth

The digitally implemented loop filter allows for two bandwidth settings that provide either wideband or narrowband jitter transfer characteristics. The filter bandwidth is selected via the BWSEL control input. In traditional PLL implementations, changing the loop filter bandwidth would require changing the values of external loop filter components.

In narrowband mode, a loop filter cutoff of 12 kHz is provided. This setting makes the Si5600 more tolerant to jitter on the reference clock source. As a result, distribution circuitry used to generate the physical layer reference clocks can be simplified without compromising jitter margin to the SONET/SDH specification.

In wideband mode, the loop filter provides a cutoff of 50 kHz. This setting is desirable in applications where the reference clock is provided by a low jitter source like the Si5364 Clock Synchronization IC or Si5320 Precision Clock Multiplier/Jitter Attenuator IC. This allows the DSPLL to more closely track the precision reference source, resulting in the best possible jitter performance.

Serialization

The Si5600 includes serialization circuitry that combines a FIFO with a parallel to serial shift register. Low speed data on the parallel input bus, TXDIN[15:0], is latched into the FIFO on the rising edge of TXCLK16IN. The data in the FIFO is clocked into the shift register by an output clock, TXCLK16OUT, that is produced by dividing down the high speed transmit clock, TXCLKOUT, by a factor of 16. The TXCLK16OUT clock output is provided to support 16-bit word transfers between the Si5600 and upstream devices using a counter clocking scheme. The high-speed serial data stream is clocked out of the shift register using TXCLKOUT.

Input FIFO

The Si5600 integrates a FIFO to decouple data transferred into the FIFO via TXCLK16IN from data transferred into the shift register via TXCLK16OUT. The FIFO is eight parallel words deep and accommodates any static phase delay that may be introduced between TXCLK16OUT and TXCLK16IN in counter clocking schemes. Furthermore, the FIFO will accommodate a phase drift or wander between TXCLK16IN and TXCLK16OUT of up to three parallel data words.

The FIFO circuitry indicates an overflow or underflow condition by asserting FIFOERR high. This output can be used to recenter the FIFO read/write pointers by tieing it directly to the FIFORST input. The Si5600 will also recenter the read/write pointers after the device's power on reset, external reset via $\overline{\text{RESET}}$, and each time the DSPLL transitions from an out of lock state to a locked state ($\overline{\text{TXLOL}}$ transitions from low to high).

Parallel Input To Serial Output Relationship

The Si5600 provides the capability to select the order in which data on the parallel input bus is transmitted serially. Data on this bus can be transmitted MSB first or LSB first depending on the setting of TXMSBSEL. If TXMSBSEL is tied low, TXDIN0 is transmitted first followed in order by TXDIN1 through TXDIN15. If TXMSBSEL is tied high, TXDIN15 is transmitted first followed in order by TXDIN14 through TXDIN0. This feature simplifies board routing when ICs are mounted on both sides of the PCB.

Transmit Data Squelch

To prevent the transmission of corrupted data into the network, the Si5600 provides a control pin that can be used to force TXDOUT to 0. By driving $\overline{\text{TXSQLCH}}$ low, the high speed serial output, TXDOUT will be forced to 0. Transmit data squelching is disabled when the device is in line loopback mode ($\overline{\text{LLBK}}$ = 0).

Clock Disable

The Si5600 provides a clock disable pin, TXCLKDSBL, that is used to disable the high-speed serial data clock output, TXCLKOUT. When the TXCLKDSBL pin is asserted, the positive and negative terminals of CLKOUT are tied to 1.5 V through 50 Ω on-chip resistors. This feature is used to reduce power consumption in applications that do not use the high speed transmit data clock.

Loop Timed Operation

The Si5600 may be configured to provide SONET/SDH compliant loop timed operation. When LPTM is asserted high, the transmit clock and data timing is derived from the recovered clock output by the CDR. This is achieved by dividing down the recovered clock and using it as a reference source for the transmit CMU. This will produce a transmit clock and data that are locked to the timing recovered from the received data path. In this mode, a narrow band loop filter setting is recommended.

Diagnostic Loopback

The Si5600 supports diagnostic loopback which establishes a loopback path from the serializer output to the deserializer input. This provides a mechanism for looping back data input via the low speed transmit interface TXDIN to the low speed receive data interface RXDOUT. This mode is enabled by forcing DLBK low.

Line Loopback

The Si5600 supports line loopback which establishes a loopback path from the high speed receive input to the high speed transmit output. This provides a mechanism for looping back the high-speed clock and data recovered from RXDIN to the transmit data output TXDOUT and clock TXCLKOUT. This mode is enabled by forcing LLBK low.

Bias Generation Circuitry

The Si5600 makes use of two external resistors, RXREXT and TXREXT, to set internal bias currents for the receive and transmit sections of the Si5600. The external resistors allows precise generation of bias currents that significantly reduce power consumption. The bias generation circuitry requires 3.09 kΩ (1%) resistors connected between RXREXT/TXREXT and GND.

Reference Clock

The Si5600 is designed to operate with reference clock sources that are either 1/16th or 1/64th the desired transceiver data rate. The device will support operation with data rates between 9.9 Gbps and 10.7 Gbps and the reference clock should be scaled accordingly. For example, to support 10.66 Gbps operation the reference clock source would be approximately 167 MHz or 666 MHz. The REFRATE input pin is used to configure the device for operation with one of the two supported reference clock submultiples of the data rate.

The Si5600 supports operation with two selectable reference clock sources. The first configuration uses an externally provided reference clock that is input via REFCLK. The second configuration uses the parallel data clock, TXCLK16IN, as the reference clock source. When using TXCLK16IN as the reference source, the narrowband loop filter setting in the CMU may be preferable to remove jitter that may be present on the data clock. The selection of reference clock source is controlled via the REFSEL input.

The CMU in the Si5600's transmit section multiplies up the provided reference to the serial transmit data rate. When the CMU has achieved lock with the selected reference, the TXLOL output will be driven high.The CDR in the receive section of the Si5600 uses a reference clock to center the PLL frequency so that it is close enough to the data frequency to achieve lock with the incoming data. When the CDR has locked to the data, RXLOL is driven high.

Reset

The Si5600 is reset by holding the RESET pin low for at least 1 µs. When RESET is asserted low, the input FIFO pointers reset and the digital control circuitry initializes. When RESET transitions high to start normal operation, the CMU will be calibrated.

Voltage Reference Output

The Si5530 provides an output voltage reference that can be used by an external circuit to set the LOS threshold, slicing level, or sampling phase adjust. One possible implementation would use a resistor divider to set the control voltage for LOSLVL, SLICELVL, or PHASEADJ. A second alternative would use a DAC to set the control voltage. Using this approach, VREF would be used to establish the range of a DAC output. The reference voltage is nominally 1.25 V.

Transmit Differential Output Circuitry

The Si5600 utilizes a current-mode logic (CML) architecture to drive the high speed serial output clock and data on TXCLKOUT and TXDOUT. An example of output termination with ac coupling is shown in Figure 5. In applications where direct dc coupling is possible, the 250 nF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is listed in Table 2 on page 5.

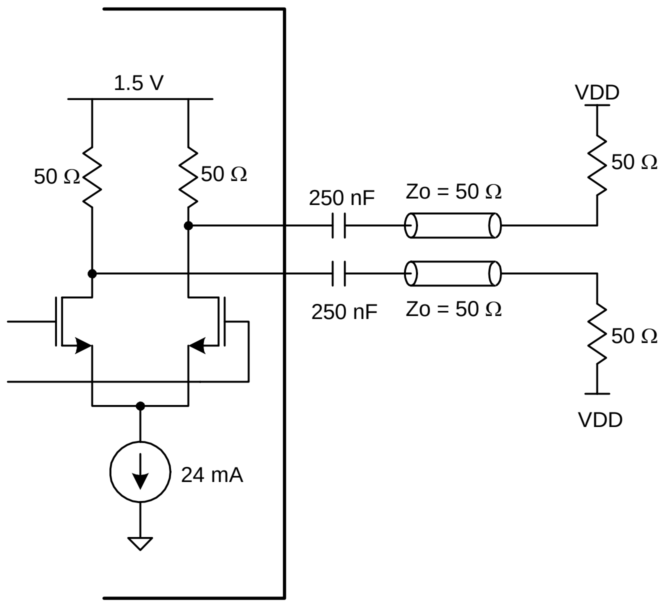

Figure 5. CML Output Driver Termination (TXCLKOUT, TXDOUT)

Si5600 Pinout: 195 BGA

	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	RXDOUT [10]+	RXDOUT [8]–	RXDOUT [8]+	RXDOUT [6]–	RXDOUT [6]+	RXDOUT [4]–	RXDOUT [4]+	RXDOUT [2]–	RXDOUT [2]+	RXDOUT [0]–	RXDOUT [0]+	RX CLK[1]–	RX CLK[1]+	
B	RXDOUT [10]–	RXDOUT [9]–	RXDOUT [9]+	RXDOUT [7]–	RXDOUT [7]+	RXDOUT [5]–	RXDOUT [5]+	RXDOUT [3]–	RXDOUT [3]+	RXDOUT [1]–	RXDOUT [1]+	RX CLK[2]–	RX CLK[2]+	GND
C	RXDOUT [12]+	RXDOUT [11]+	RXCLK2 DIV	RXREXT	NC	RXSQLCH	RXCLK2 DSBL	RSVD_ GND	RSVD_ GND	VREF	SLICELVL	LOSLVL	GND	GND
D	RXDOUT [12]–	RXDOUT [11]–	RXMSB SEL	GND	GND	GND	GND	GND	GND	GND	PHASEADJ	RSVD_ GND	GND	RXDIN+
E	RXDOUT [14]+	RXDOUT [13]+	RSVD_ GND	GND	VDD	VDD	VDD	VDD	VDD	VDD	RSVD_ VDD33	LTR	GND	RXDIN–
F	RXDOUT [14]–	RXDOUT [13]–	DLBK	GND	VDD	VDD	VDD	VDD	VDD	VDD	RSVD_ GND	RXLOL	GND	GND
G	REF CLK+	RXDOUT [15]+	RSVD_ VDD33	GND	VDD	VDD	VDD	VDD	VDD	VDD	RESET	LOS	GND	TXCLKOUT+
H	REF CLK–	RXDOUT [15]–	LLBK	GND	VDD	VDD	VDD	VDD	VDD	VDD	REFRATE	VDD33	GND	TXCLKOUT–
J	TXDIN [14]+	TXDIN [15]+	LPTM	GND	VDD	VDD	VDD	VDD	VDD	VDD	GND	GND	GND	GND
K	TXDIN [14]–	TXDIN [15]–	TXCLK DSBL	GND	VDD	VDD	VDD	VDD	VDD	VDD	RSVD_ GND	FIFOERR	GND	TXDOUT+
L	TXDIN [12]+	TXDIN [13]+	REFSEL	GND	GND	GND	GND	GND	GND	GND	NC	TXREXT	GND	TXDOUT–
M	TXDIN [12]–	TXDIN [13]–	TXSQLCH	RSVD_ GND	RSVD_ GND	TXMSB SEL	RSVD_ GND	BWSEL	FIFORST	TXLOL	GND	GND	GND	GND
N	TXDIN [11]+	TXDIN [11]–	TXDIN [9]+	TXDIN [9]–	TXDIN [7]+	TXDIN [7]–	TXDIN [5]+	TXDIN [5]–	TXDIN [3]+	TXDIN [3]–	TXDIN [1]+	TXDIN [1]–	TXCLK16 IN+	TXCLK16 IN–
P	TXDIN [10]+	TXDIN [10]–	TXDIN [8+]	TXDIN [8]–	TXDIN [6]+	TXDIN [6]–	TXDIN [4]+	TXDIN [4]–	TXDIN [2]+	TXDIN [2]–	TXDIN [0]+	TXDIN [0]–	TXCLK16 OUT+	TXCLK16 OUT–

Bottom View

Figure 6. Si5600 Pin Configuration (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		RX CLK1+	RX CLK1-	RXDOUT [0]+	RXDOUT [0]–	RXDOUT [2]+	RXDOUT [2]–	RXDOUT [4]+	RXDOUT [4]–	RXDOUT [6]+	RXDOUT [6]–	RXDOUT [8]+	RXDOUT [8]–	RXDOUT [10]+
B	GND	RX CLK[2]+	RX CLK[2]–	RXDOUT [1]+	RXDOUT [1]–	RXDOUT [3]+	RXDOUT [3]–	RXDOUT [5]+	RXDOUT [5]–	RXDOUT [7]+	RXDOUT [7]–	RXDOUT [9]+	RXDOUT [9]–	RXDOUT [10]–
C	GND	GND	LOSLVL	SLICELVL	VREF	RSVD_ GND	RSVD_ GND	RXCLK2 DSBL	$\overline{\text{RXSQLCH}}$	NC	RXREXT	RXCLK2 DIV	RXDOUT [11]+	RXDOUT [12]+
D	RXDIN+	GND	RSVD_ GND	PHASE ADJ	GND	GND	GND	GND	GND	GND	GND	RXMSB SEL	RXDOUT [11]–	RXDOUT [12]–
E	RXDIN–	GND	$\overline{\text{LTR}}$	RSVD_ VDD33	VDD	VDD	VDD	VDD	VDD	VDD	GND	RSVD_ GND	RXDOUT [13]+	RXDOUT [14]+
F	GND	GND	$\overline{\text{RXLOL}}$	RSVD_ GND	VDD	VDD	VDD	VDD	VDD	VDD	GND	$\overline{\text{DLBK}}$	RXDOUT [13]–	RXDOUT [14]–
G	TXCLKOUT+	GND	$\overline{\text{LOS}}$	$\overline{\text{RESET}}$	VDD	VDD	VDD	VDD	VDD	VDD	GND	RSVD_ VDD33	RXDOUT [15]+	REF CLK+
H	TXCLKOUT–	GND	VDD33	REFRATE	VDD	VDD	VDD	VDD	VDD	VDD	GND	$\overline{\text{LLBK}}$	RXDOUT [15]–	REF CLK–
J	GND	GND	GND	GND	VDD	VDD	VDD	VDD	VDD	VDD	GND	LPTM	TXDIN [15]+	TXDIN [14]+
K	TXDOUT+	GND	FIFOERR	RSVD_ GND	VDD	VDD	VDD	VDD	VDD	VDD	GND	TXCLK DSBL	TXDIN [15]–	TXDIN [14]–
L	TXDOUT–	GND	TXREXT	NC	GND	GND	GND	GND	GND	GND	GND	REFSEL	TXDIN [13]+	TXDIN [12]+
M	GND	GND	GND	GND	$\overline{\text{TXLOL}}$	FIFORST	BWSEL	RSVD_ GND	TXMSB SEL	RSVD_ GND	RSVD_ GND	$\overline{\text{TXSQLCH}}$	TXDIN [13]–	TXDIN [12]–
N	TXCLK16 IN–	TXCLK16 IN+	TXDIN [1]–	TXDIN [1]+	TXDIN [3]–	TXDIN [3]+	TXDIN [5]–	TXDIN [5]+	TXDIN [7]–	TXDIN [7]+	TXDIN [9]–	TXDIN [9]+	TXDIN [11]–	TXDIN [11]+
P	TXCLK16 OUT–	TXCLK16 OUT+	TXDIN [0]–	TXDIN [0]+	TXDIN [2]–	TXDIN [2]+	TXDIN [4]–	TXDIN [4]+	TXDIN [6]–	TXDIN [6]+	TXDIN [8]–	TXDIN [8]+	TXDIN [10]–	TXDIN [10]+

Top View

Figure 7. Si5600 Pin Configuration (Transparent Top View)

Pin Descriptions: Si5600

Pin Number(s)	Name	I/O	Signal Level	Description
M7	BWSEL	I	LVTTL	**Bandwidth Select DSPLL.** This input selects loop bandwidth of the DSPLL. BWSEL = 0: Loop bandwidth set to 12 kHz. BWSEL = 1: Loop bandwidth set to 50 kHz.
F12	$\overline{\text{DLBK}}$	I	LVTTL	**Diagnostic Loopback.** When this input is active low the transmit clock and data are looped back for output on RXDOUT, RXCLK1 and RXCLK2. This pin should be held high for normal operation.
K3	FIFOERR	O	LVTTL	**FIFO Error.** This output is driven high when a FIFO overflow/ underflow has occurred. This output will stick high until reset by asserting FIFORST.
M6	FIFORST	I	LVTTL	**FIFO RESET.** This input when asserted high resets the read/ write FIFO pointers to their initial state.
B1, C1–2, D5–11, D2, E11, E2, F11, F1–2, G11, G2, H11, H2, J11, J1–4, K2, K11, L5–11, L2, M1–4	GND	GND		**Supply Ground.**
H12	$\overline{\text{LLBK}}$	I	LVTTL	**Line Loopback.** When this input is active low the recovered clock and data are looped back for output on TXDOUT, and TXCLKOUT. This pin should be held high for normal operation.
G3	$\overline{\text{LOS}}$	O	LVTTL	**Loss-of-Signal.** This output is driven low when the peak-to-peak signal amplitude is below threshold set via LOSLVL.
C3	LOSLVL	I		**LOS Threshold Level.** Applying an analog voltage to this pin allows adjustment of the threshold used to declare LOS. Tieing this input high disables LOS detection and forces the $\overline{\text{LOS}}$ output high.

Pin Number(s)	Name	I/O	Signal Level	Description
J12	LPTM	I	LVTTL	**Loop Timed Operation.** When this input is forced high, the recovered clock from the receiver is divided down and used as the reference source for the transmit CMU. The narrowband setting for the DSPLL CMU will be sufficient to provide SONET compliant jitter generation and transfer on the transmit data and clock outputs (TXDOUT,TXCLKOUT). This pin should be held low for normal operation.
E3	$\overline{\text{LTR}}$	I	LVTTL	**Lock-to-Reference** This input forces a stable output clock by locking RXCLK1 and RXCLK2 to the provided reference. Driving $\overline{\text{LTR}}$ low activates this feature.
C10, L4	NC			**No Connect.** Reserved for device testing leave electrically unconnected.
D4	PHASEADJ	I		**Sampling Phase Adjust.** Applying an analog voltage to this pin allows adjustment of the sampling phase across the data eye. Tieing this input high nominally centers the sampling phase.
G14, H14	REFCLK+, REFCLK–	I	LVPECL	**Differential Reference Clock.** The reference clock sets the operating frequency of the PLL used to generate the high speed transmit clock. In addition, REFCLK sets the initial operating frequency used by the onboard PLL for clock and data recovery. The Si5600 will operate with reference clock frequencies that are either 1/16th or 1/64th the serial data rate (nominally 155 MHz or 622 MHz).
H4	REFRATE	I	LVTTL	**Reference Clock Select.** This input configures the Si5600 to operate with one of two reference clock frequencies. If REFRATE is held high, the device requires a reference clock that is 1/16 the serial data rate. If REFRATE is low, a reference clock at 1/64 the serial data rate is required.
L12	REFSEL	I	LVTTL	**Reference Clock Selection.** This inputs selects the reference clock source used by the CMU. When REFSEL = 0, the low speed data input clock, TXCLK16IN, is used as the CMU reference. When REFSEL = 1, the reference clock provided on REFCLK is used.

Pin Number(s)	Name	I/O	Signal Level	Description
G4	$\overline{\text{RESET}}$	I	LVTTL	**Device Reset.** Forcing this input low for a at least 1 µs will cause a device reset. For normal operation, this pin should be held high.
C6–7, D3, E12, F4, K4, M10–11, M8	RSVD_GND			**Reserved Tie to Ground.** Must tie directly to GND for proper operation.
E4, G12	RSVD_VDD33			**Reserved Tie to VDD33.** Must tie directly to VDD33 for proper operation.
A2–3	RXCLK1+, RXCLK1–	O	LVDS	**Differential Clock Output 1.** The clock recovered from the signal present on RXDIN is divided down by 16 and output on CLK-OUT. In the absence of data, a stable clock on RXCLK1 can be maintained by asserting $\overline{\text{LTR}}$.
B2–3	RXCLK2+, RXCLK2–	O	LVDS	**Differential Clock Output 2.** An auxiliary output clock is provided on this pin that may be a divided down version of the high speed clock recovered from the signal present on RXDIN. The divide factor used in generating RXCLK2 is set via RXCLK2DIV.
C12	RXCLK2DIV	I	LVTTL	**Clock Divider Select.** This input selects the divide factor used to generate the RXCLK2 output. When this input is driven low, RXCLK2 is 1/16th the recovered high speed clock. When driven high, RXCLK2 is 1/64th the recovered high speed clock rate.
C8	RXCLK2DSBL	I	LVTTL	**RXCLK2 Disable.** Driving this input high will disable the RXCLK2 output. This would be used to save power in applications that do not require an auxiliary clock.
D1, E1	RXDIN+, RXDIN–	I	High Speed Differential	**Differential Data Input.** Clock and data are recovered from the high speed data signal present on these pins.
A4–14, B4–14, C13–14, D13–14, E13–14, F13–14, G13, H13	RXDOUT[15:0]+, RXDOUT[15:0]–	O	LVDS	**Differential Parallel Data Output.** The data recovered from the signal present on RXDIN is demultiplexed and output as a 16-bit parallel word via RXDOUT[15:0]. These outputs are updated on the rising edge of RXCLK1.
F3	$\overline{\text{RXLOL}}$	O	LVTTL	**Loss-of-Lock.** This output is driven low when the recovered clock frequency deviates from the reference clock by the amount specified in Table 5.

Pin Number(s)	Name	I/O	Signal Level	Description
D12	RXMSBSEL	I	LVTTL	**Data Bus Receive Order.** This determines the order of the received data bits on the output bus. For RXMSBSEL = 0, the first data bit received is output on RXDOUT[0] and following data bits are output on RDOUT[1] through RXDOUT[15]. For RXMSBSEL = 1, the first data bit is output on RXDOUT[15] and following data bits are output on RXDOUT[14] through RXDOUT[0].
C11	RXREXT			**External Bias Resistor.** This resistor is used by the receiver circuitry to establish bias currents within the device. This pin must be connected to GND through a 3.09 kΩ (1%) resistor.
C9	$\overline{\text{RXSQLCH}}$	I	LVTTL	**Data Squelch.** When this input is low the data on RXDOUT is forced to 0. Set high for normal operation.
C4	SLICELVL	I		**Slicing Level Adjustment.** Applying an analog voltage to this pin allows adjustment of the slicing level applied to the input data eye. Tieing this input high nominally sets the slicing offset to 0.
N1–2	TXCLK16IN+, TXCLK16IN–	I	LVDS	**Differential Data Clock Input.** The rising edge of this input clocks data present on TXDIN into the device.
P1–2	TXCLK16OUT+, TXCLK16OUT–	O	LVDS	**Divided Down Output Clock.** This clock output is generated by dividing down the high speed output clock, TXCLKOUT, by a factor of 16. It is intended for use in counter clocking schemes that transfer data between the system ASIC and the Si5600.
K12	TXCLKDSBL	I	LVTTL	**High Speed Clock Disable** When this input is high, the output driver for TXCLKOUT is disabled. In applications that do not require the output data clock, the output clock driver should be disabled to save power.
G1, H1	TXCLKOUT+, TXCLKOUT–	O	CML	**High Speed Clock Output.** The high speed output clock, TXCLKOUT, is generated by the PLL in the clock multiplier unit. Its frequency is nominally 16 or 64 times the selected reference source.

Pin Number(s)	Name	I/O	Signal Level	Description
J13–14, K13–14, L13–14, M13–14, N3–14, P3–14	TXDIN[15:0]+, TXDIN[15:0]–	I	LVDS	**Differential Parallel Data Input.** The 16-bit data word present on these pins is multiplexed into a high speed serial stream and output on TXDOUT. The data on these inputs is clocked into the device by the rising edge of TXCLK16IN.
K1, L1	TXDOUT+, TXDOUT–	O	CML	**Differential High Speed Data Output.** The 16-bit word input on TXDIN[15:0] is multiplexed into a high speed serial stream that is output on these pins. Input data is multiplexed in sequence from TXDIN0 to TXDIN15 with TXDIN0 transmitted first. This output is updated by the rising edge of TXCLKOUT.
M5	$\overline{\text{TXLOL}}$	O	LVTTL	**CMU Loss-of-Lock.** The output is asserted low when the CMU is not phase locked to the selected reference source.
M9	TXMSBSEL	I	LVTTL	**Data Bus Transmit Order.** For TXMSBSEL = 0, data on TXDIN[0] is transmitted first followed by TXDIN[1] through TXDIN[15]. For TXMSBSEL = 1, TXDIN[15] is transmitted first followed by TXDIN[14] through TXDIN[0].
L3	TXREXT			**External Bias Resistor.** This resistor is used by the transmitter circuitry to establish bias currents within the device. This pin must be connected to GND through a 3.09 kΩ (1%) resistor.
M12	$\overline{\text{TXSQLCH}}$	I	LVTTL	**Transmit Data Squelch.** If $\overline{\text{TXSQLCH}}$ is asserted low, the output data stream on TXDOUT will be forced to 0s. If $\overline{\text{TXSQLCH}}$ = 1, TX squelching is turned off.
E5–10, F5–10, G5–10, H5–10, J5–10, K5–10	VDD	VDD	1.8 V	**Supply Voltage.** Nominally 1.8 V.

Pin Number(s)	Name	I/O	Signal Level	Description
H3	VDD33	VDD33	1.8 V or 3.3 V	**Digital Output Supply.** Must be tied to either 1.8 V or 3.3 V. When tied to 3.3 V, LVTTL compatible output voltage swings on RXLOL and LOS, TXLOL, FIFOERR are supported.
C5	VREF	O	Voltage Ref	**Voltage Reference.** The Si5600 provides an output voltage reference that can be used by an external circuit to set the LOS threshold, slicing level, or sampling phase adjustment. The equivalent resistance between this pin and GND should not be less than 10 kΩ. The reference voltage is nominally 1.25 V.

Ordering Guide

Table 9. Ordering Guide

Part Number	Package	Temperature
Si5600-BC	195 BGA	–40°C to 85°C

Package Outline

Figure 8 illustrates the package details for the Si5600. Table 10 lists the values for the dimensions shown in the illustration.

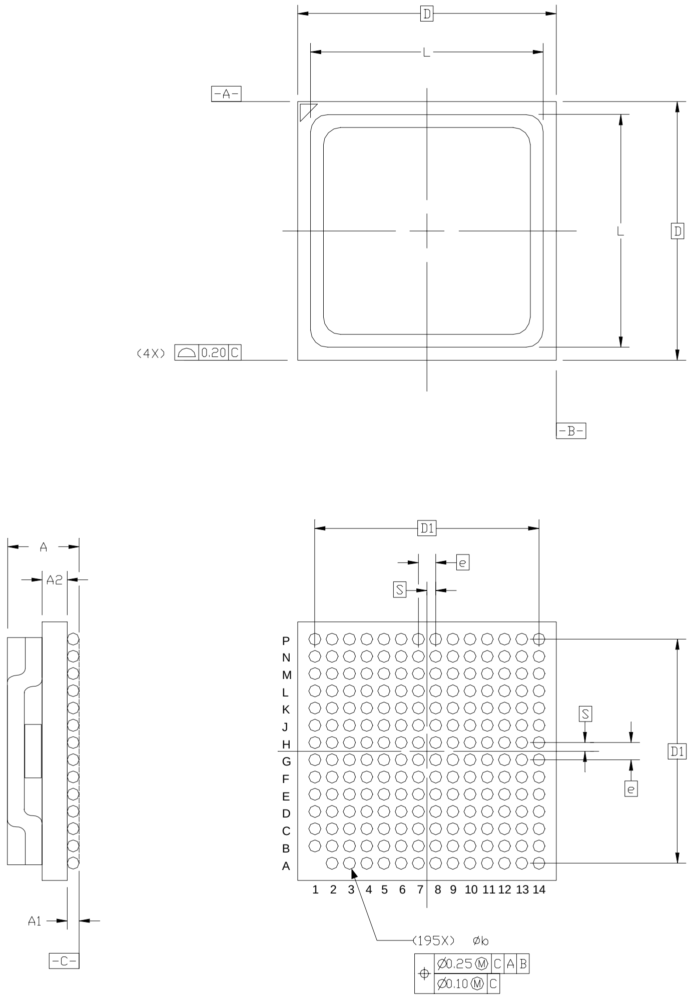

Figure 8. 195-Ball Grid Array (BGA)

Table 10. Package Diagram Dimensions (mm)

Symbol	Min	Nom	Max
A	3.50	3.65	3.80
A1	0.65	0.70	0.75
A2	1.35	1.45	1.55
b	0.65	0.70	0.75
D	14.90	15.00	15.10
D1	—	13.00	—
e	—	1.00	—
L	12.95	13.00	13.05
S	—	0.50	—

NOTES:

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