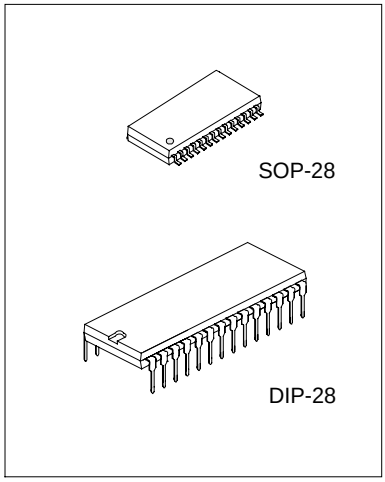
SC3010

INFRARED REMOTE CONTROL TRANSMITTER



DESCRIPTION

SC3010 is a remote control transmitter utilizing CMOS Technology specially designed for use on general purpose (RC-5) infrared applications with low voltage supply and large debounce time. SC3010 supports 32 systems. Each system has a maximum of 64 commands; thus, SC3010 can provide up to a total of 2,048 commands.

FEATURES

* CMOS Technology
* Low Voltage Supply
* Supports up to 32 systems
* Single Pin Oscillator
* Bi-phase Transmission Technique
* Provides 2,048 Commands

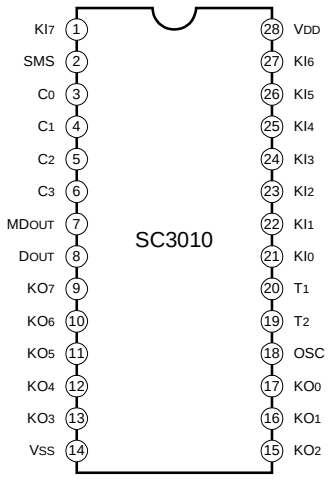
APPLICATIONS

* Television
* VCR
* Audio Equipment
* Multi-Media System
* Personal Computer

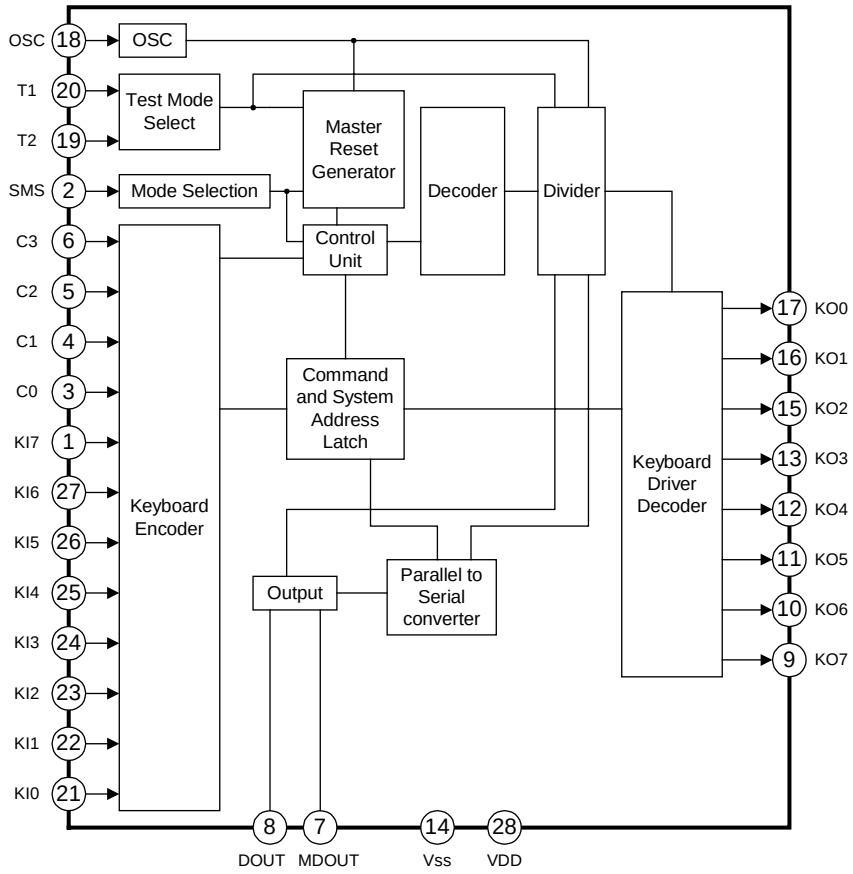
ORDERING INFORMATION

SC3010	DIP-28 Package
SC3010S	SOP-28 Package

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Tamb=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Value	Unit
Supply Voltage*	V_{DD}		V_{SS} -0.3 ~ 5.5	V
Input Voltage*	V_{IN}	V_{DD}=3 V	-0.5 ~ V_{DD}+0.5	V
Output Voltage*	V_{OUT}	V_{DD}=3 V	-0.5 ~ V_{DD}+0.5	V
Operating Temperature	T_{OPR}	V_{DD}=3 V	-20~85	°C

NOTE: * = with reference to Vss

ELECTRICAL CHARACTERISTICS (Tamb=25°C, unless otherwise specified)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	Freq=455KHz	2.0	3.0	5.5	V
Stand-By Current	I_{DD}	V_{DD} =3V (Output no load)		0	10	μA
Input Current(KI0~KI7,C0~C3)	I_{IN}	VI=0V T1=0 T2=0 SMS=0		15	600	μA
High Level Input Voltage (KI0~KI7,C0~C3,SMS,T1,T2)	V_{IH}	V_{DD} =3V,(KI0~KI7 And C0~C3 Connected To V_{DD})	0.7 V_{DD}			V
Low Level Input Voltage (KI0~KI7,C0~C3,SMS,T1,T2)	V_{IL}	V_{DD} =3V ,(T1,T2,OSC,SMS Connected To V_{SS})			0.3 V_{DD}	V
Input Current Leakage (KI0~KI7,C0~C3)	I_{LEAK1}	VI=3V V_{DD}=3V T1=T2=High		0	1.0	μA
		VI=0V V_{DD}=3V T1=T2=High		0	1.0	
Input Current Leakage (OSC)	I_{LEAK2}	VI=0V V_{DD}=3V T1=T2=High		0	1.0	μA
	I_{LEAK3}	VI=3V V_{DD}=3V T1=T2=High	4.5	15	30	
Input Leakage Current (SMS,T1,T2)	I_{LEAK4}	VI=3V V_{DD}=3V T=25°C		0	1.0	μA
		VI=0V V_{DD}=3V T=25°C		0	1.0	
High Level Output Voltage (Dout, MD_{OUT})	V_{OH}	V_{DD}=3V I_{OH}=0.4mA	V_{DD}-0.3			V
Low Level Output Voltage (Dout, MD_{OUT})	V_{OL}	V_{DD}=3V I_{OH}=0.6mA			0.35	
Output Current Leakage (Dout, MD_{OUT})	I_{LEAK5}	Vo=3V V_{DD}=3V T=25°C			10	μA
		Vo=0V V_{DD}=3V T=25°C			1	
Low Level Output Voltage (KO0~KO7)	V_{OL}	V_{DD}=3V I_{OL}=0.3mA			0.8	V
Output Current Leakage (KO0~KO7)	I_{LEAK6}	Vo=3V V_{DD}=3V T=25°C		0	1	μA
		Vo=3V V_{DD}=3V T=-25~85°C		3	10	
Drive Current (Dout, MDout)	ID	V_{DD}=3V Vo=1.5V	1.5		2	mA
Operational Frequency	Fosc1	V_{DD}=3V	400		600	KHz
Free-Running Frequency	Fosc2	V_{DD}=3V	50		100	KHz

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description	NOTE
1	KI7	IP	Key Sense Input Pin	IP= Input with p-channel pull-up transistor; OD = Output with open drain n-channel transistor
2	SMS	I	System Mode Selection Input Pin	
3~6	C0~C3	IP	Key Sense Input Pins	
7	MD_{OUT}	O	Generated Output Data Pin modulated with 1/12 oscillator frequency at a 25% duty factor	
8	D_{OUT}	O	Generated Output Data Pin	
9~13	KO7~KO3	OD	Scan Driver Pins	
14	V_{SS}	Power	Negative Power Supply	
15~17	KO2~KO0	OD	Scan Driver Pins	
18	OSC	I	Oscillator Input Pin	
19	T2	I	Test Pin 2	
20	T1	I	Test Pin 1	
21~27	KI0~KI6	IP	Key Sense Input Pins	
28	V_{DD}	Power	Positive Power Supply	

FUNCTIONAL DESCRIPTION

1. KEY INPUT OPERATION

A Key Input Operation may be considered legal or illegal depending on the keys pressed. For key interconnection refer to the application circuit diagram in APPLICATION CIRCUIT SECTION. The maximum value of the switched key contact series resistance is 7kΩ.

a). Legal Key Input

A legal key input operation enables the device to activate the corresponding codes. A key input operation is considered as legal if it is 1). a connection of one K-Input (KI0~KI7) to one K-Output (KO0~KO7), or 2).a connection of one C-Input(C0~C3) to one K-Output (KO0~KO7) when the System Mode Selection (SMS) Pin is in a LOW state. If the SMS is in a HIGH state, then a wired connection must be made between a C-Input to a K-Output in order to generate the system number. For connections consisting of one K-Input or C-Input to more than one K-Output Pins, the last scan signal is recognized as LEGAL.

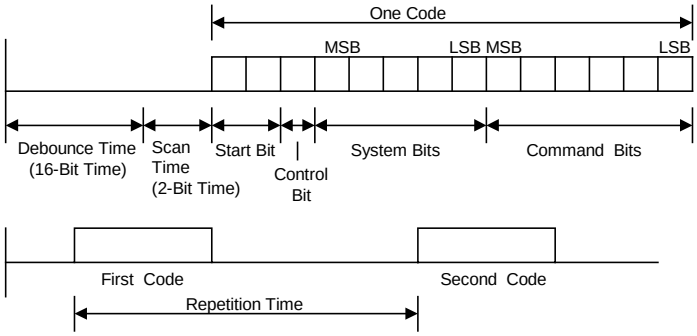
b). Illegal Key Input

An illegal key input operation does not produce any activity. No activity will be generated if 1) two or more K-Input/C-Input Pins or 2) C-Input and K-Input Pins are activated simultaneously. The oscillator will not start. Thus, this operation is considered as ILLEGAL.

2. INPUTS: KI0~KI7 & C0~C3

In the quiescent state, the command inputs KI0~KI7 are pulled HIGH by an internal pull-up transistor. Also if the system is quiescent and the System Mode Selection Input (SMS) is in High state so that current flow may be prevented. A wired connection in the C-KO Matrix provides 32 systems.

3. DATA OUTPUT



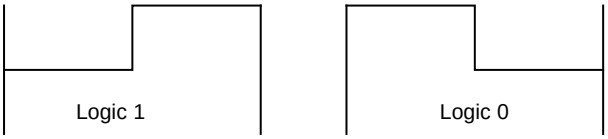
Where: debounce time+ scan time=18 bit-times, Repetition time=4x16 bit-times

Figure 1: Data Output Format

The generated information is transmitted through the output signal DOUT. The Data Output Code consists of 1.5 Start Bits (2xLogic 1), 1 Control Bit, 5 System Bits, and 6 Command Bits. Please refer to the diagram above for the data output format. (See also Command and System Matrixes).

After a legal key operation is performed, the KO outputs are switched off and a 16-bit debounce time period is experienced followed by a 2-bit scan cycle time. During the scanning cycle the outputs are switched to the conductive state one at a time.

Code is transmitted using a biphase technique. Please refer to the diagram below. The MDOUT Output Signal transmits the generated data modulated by 1/12 of the oscillator frequency with a 25% duty factor.



where: 1 bit-time=3x2^8xTosc=1.688ms (typ. Tosc=1/455KHz)

Figure 2: Biphase Code Transmission Technique

Both the DOUT and the MDOUT are non-conducting (3-state outputs) when in the quiescent state. The Scan Driver Outputs (KO0~KO7) are open drain n-channel and conduct when the circuit is in the quiescent state.

4. SYSTEM MODES

a). Combined System Mode (SMS=Low)

The KI and the C Sense Inputs have p-channel pull-up transistors (meaning they are normally in HIGH state). They are pulled to LOW state when an output is connected, to them as a result of a legal key operation. A legal key operation in the KI-KO or C-KO Matrix will initiate a debounce cycle. Once key contact has been established for 18-bit time without any interruption, the Oscillator Enable Signal is latched and the key may be released. The device is reset when there is an interruption during the 18-bit time period. At the end of the debounce cycle, KO Outputs are switched off and two scan cycles begins.

When KI or C Input senses a low level output, a Latch-Enable Signal is fed to the System (C-Input) or Command (KI-Input) Latches. After latching a system number, the device will generate the last command (i.e. all command bits logic 1) in the selected system for as long as the key is pressed. Latching of a command number causes the chip to generate this command together with the system number stored in the system latch. By releasing the key, the device will be reset if no data is to be transmitted at the time. The complete code frame is transmitted even if the key is released during code transmission.

b). Single System Mode (SMS=High)

In the Single System Mode, the KI-Sense Inputs are also pulled High by the p-channel pull-up transistors, as in the Combined System Mode. The C-Sense Inputs, however, are disabled by switching off their pull-high transistors. A system code is provided by a wired connection between the C-KO Matrix. The debounce cycle can ONLY be started by any legal key operation in the KI-KO Matrix. Once the key contact has been established for 18-bit time without any interruption, the Oscillator-Enable Signal is latched and the key may be released. Any interruption during the 18-bit time period resets the internal action.

At the end of the debounce cycle, the pull-up transistors in the KI-Lines are then switched off and the pull-up transistors in the C-lines are turned ON for the first scan cycle. The wired connection in the C-matrix matrix is then translated into a system number and stored in the system latch. At the end of the first scan cycle, 1) the C-Input pull-up transistors are switched off and the inputs are again disabled, 2) KI-Sense Input pull-up transistors are turned on. The command number is generated by the second scan cycle. This command number is then latched and transmitted together with the system number.

5.KEY RELEASE DETECTION

An additional control bit is complemented after key release. This additional control bit tells the decoder that the next code is a new command. This feature is important in cases where more digits are needed to be inputted (i.e. Teletext channel numbers or Viewdata pages). The extra control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission; thus, even with the Take Over of key operation during the code transmission, the correct system and command numbers are generated.

6.RESETTING THE DEVICE

The device will immediately reset under the following conditions:

1). A key is released during the debounce time

2). A key is released between two codes

3). During Matrix Scanning

a). A key is released while one of the drivers outputs is in the low ohmic state (Logic 0)

b). A key is released before that key has been detected.

c). There is no wired connection in the C-KO Matrix when SMS is in High State.

7.OSCILLATOR

The OSC is a 1-pin oscillator input/output terminal. The oscillator is constructed by connecting in series a ceramic resonator like TOKO CRK429.

8. TEST MODE

When T1,T2 and OSC Pins are in HIGH State, the circuit initializes. All internal nodes except for the LATCH are defined. The latch is defined when a scan cycle starts by pulling down a KI or a C Input while the oscillator is active.

If the debounce cycle has been completed, then the scan cycle can be accomplished $3x2^3$ times faster by setting the T1 to HIGH. If the scan cycle has been completed, the Latch contents can be read $3x2^7$ times faster by setting the T2 to HIGH.

SC3010 COMMAND MATRIX DATA CODE

The Command Matrix Data Code is given in the table below:

No.	KI-Line								KO-Line								Command Bits					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	•								•								0	0	0	0	0	0
1	•									•							0	0	0	0	0	1
2	•										•						0	0	0	0	1	0
3	•											•					0	0	0	0	1	1
4	•												•				0	0	0	1	0	0
5	•													•			0	0	0	1	0	1
6	•														•		0	0	0	1	1	0
7	•															•	0	0	0	1	1	1
8		•							•								0	0	1	0	0	0
9		•								•							0	0	1	0	0	1
10		•									•						0	0	1	0	1	0
11		•										•					0	0	1	0	1	1
12		•											•				0	0	1	1	0	0
13		•												•			0	0	1	1	0	1
14		•													•		0	0	1	1	1	0
15		•														•	0	0	1	1	1	1
16			•						•								0	1	0	0	0	0
17			•							•							0	1	0	0	0	1
18			•								•						0	1	0	0	1	0
19			•									•					0	1	0	0	1	1
20			•										•				0	1	0	1	0	0
21			•											•			0	1	0	1	0	1
22			•												•		0	1	0	1	1	0
23			•													•	0	1	0	1	1	1
24				•					•								0	1	1	0	0	0
25				•						•							0	1	1	0	0	1
26				•							•						0	1	1	0	1	0
27				•								•					0	1	1	0	1	1
28				•									•				0	1	1	1	0	0
29				•										•			0	1	1	1	0	1
30				•											•		0	1	1	1	1	0
31				•												•	0	1	1	1	1	1

(to be continued)

(continued)

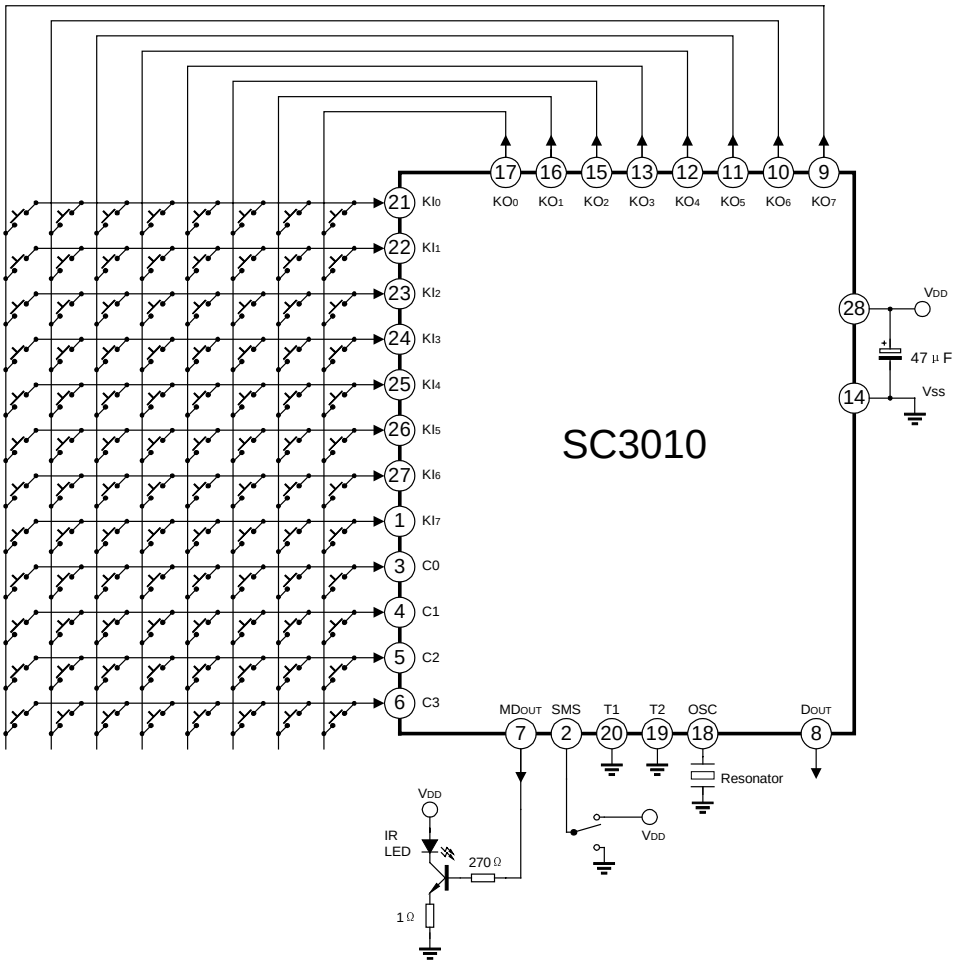
No.	KI-Line								KO-Line								Command Bits					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					•				•								1	0	0	0	0	0
33					•					•							1	0	0	0	0	1
34					•						•						1	0	0	0	1	0
35					•							•					1	0	0	0	1	1
36					•								•				1	0	0	1	0	0
37					•									•			1	0	0	1	0	1
38					•										•		1	0	0	1	1	0
39					•											•	1	0	0	1	1	1
40						•			•								1	0	1	0	0	0
41						•				•							1	0	1	0	0	1
42						•					•						1	0	1	0	1	0
43						•						•					1	0	1	0	1	1
44						•							•				1	0	1	1	0	0
45						•								•			1	0	1	1	0	1
46						•									•		1	0	1	1	1	0
47						•										•	1	0	1	1	1	1
48							•		•								1	1	0	0	0	0
49							•			•							1	1	0	0	0	1
50							•				•						1	1	0	0	1	0
51							•					•					1	1	0	0	1	1
52							•						•				1	1	0	1	0	0
53							•							•			1	1	0	1	0	1
54							•								•		1	1	0	1	1	0
55							•									•	1	1	0	1	1	1
56								•	•								1	1	1	0	0	0
57								•		•							1	1	1	0	0	1
58								•			•						1	1	1	0	1	0
59								•				•					1	1	1	0	1	1
60								•					•				1	1	1	1	0	0
61								•						•			1	1	1	1	0	1
62								•							•		1	1	1	1	1	0
63								•								•	1	1	1	1	1	1

SC3010 SYSTEM MATRIX DATA CODE

The System Matrix Data Code for K-KO Lines are given in the table below:

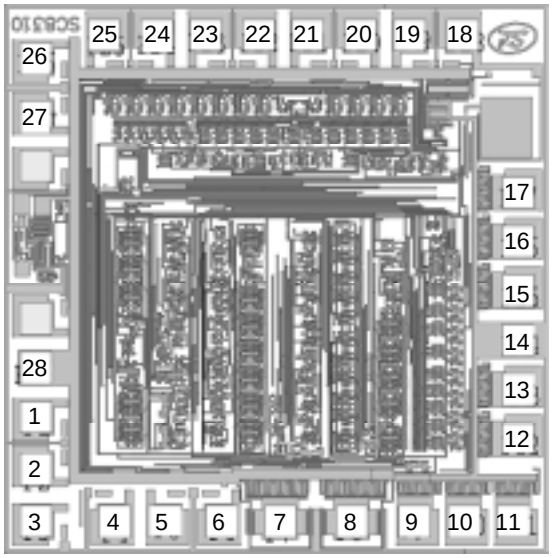
System No.	C-Line				KO-Line								System Bits				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	•				•								0	0	0	0	0
1	•					•							0	0	0	0	1
2	•						•						0	0	0	1	0
3	•							•					0	0	0	1	1
4	•								•				0	0	1	0	0
5	•									•			0	0	1	0	1
6	•										•		0	0	1	1	0
7	•											•	0	0	1	1	1
8		•			•								0	1	0	0	0
9		•				•							0	1	0	0	1
10		•					•						0	1	0	1	0
11		•						•					0	1	0	1	1
12		•							•				0	1	1	0	0
13		•								•			0	1	1	0	1
14		•									•		0	1	1	1	0
15		•										•	0	1	1	1	1
16			•		•								1	0	0	0	0
17			•			•							1	0	0	0	1
18			•				•						1	0	0	1	0
19			•					•					1	0	0	1	1
20			•						•				1	0	1	0	0
21			•							•			1	0	1	0	1
22			•								•		1	0	1	1	0
23			•									•	1	0	1	1	1
24				•	•								1	1	0	0	0
25				•		•							1	1	0	0	1
26				•			•						1	1	0	1	0
27				•				•					1	1	0	1	1
28				•					•				1	1	1	0	0
29				•						•			1	1	1	0	1
30				•							•		1	1	1	1	0
31				•								•	1	1	1	1	1

APPLICATION CIRCUIT



NOTE: There is a connection between the C0~C3 Lines and KO0~KO7 Lines if SMS is tied to VDD.

CHIP TOPOGRAPHY



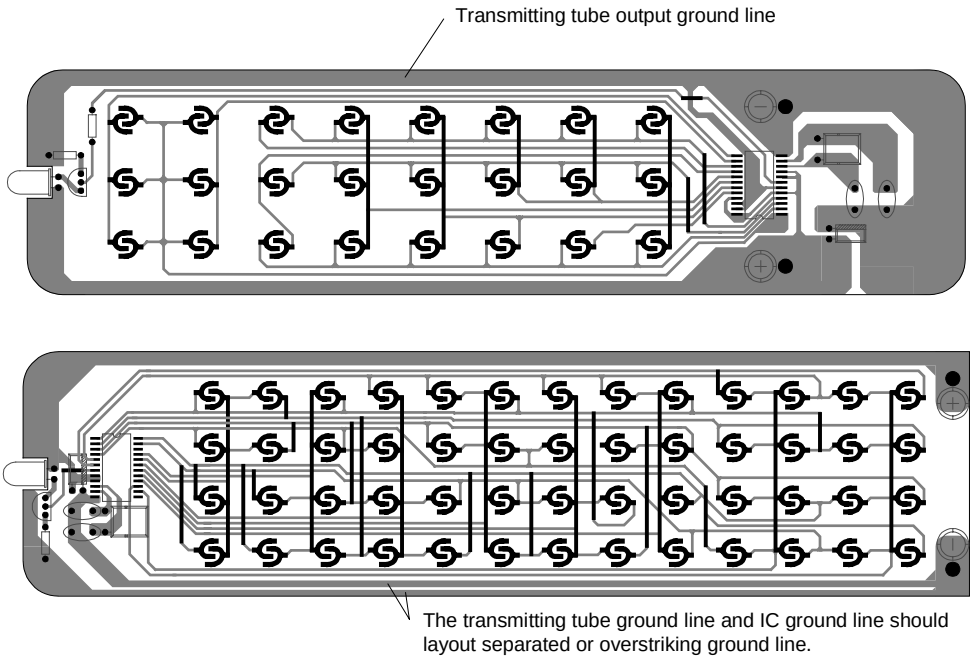
size: 1.71 x 1.69 mm^2

PAD COORDINATES (Unit: μm)

No.	Symbol	X	Y	No.	Symbol	X	Y
1	P1	-674.50	-407.50	15	P15	693.50	-49.00
2	P2	-674.50	-554.00	16	P16	693.50	91.00
3	P3	-674.50	-704.00	17	P17	693.50	231.00
4	P4	-450.50	-704.00	18	P18	537.00	680.50
5	P5	-309.75	-704.25	19	P19	386.75	680.50
6	P6	-146.50	-704.25	20	P20	246.75	680.50
7	P7	-18.75	-704.25	21	P21	97.25	680.50
8	P8	221.75	-704.25	22	P22	-42.75	680.50
9	P9	400.25	-704.25	23	P23	-192.25	680.50
10	P10	539.25	-704.25	24	P24	-332.00	680.50
11	P11	679.00	-704.25	25	P25	-481.50	680.50
12	P12	693.50	-468.75	26	P26	-674.50	614.50
13	P13	693.50	-329.00	27	P27	-674.50	449.00
14	P14	693.50	-189.00	28	P28	-674.50	267.375

Note: The original point of the coordinate is the die center.

PCB WIRE LAYOUT SCHEMATIC:



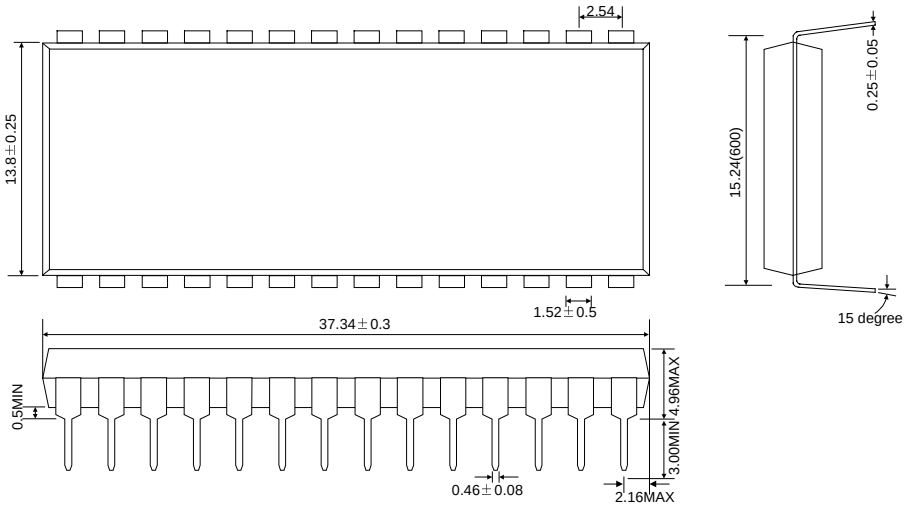
The above IC only use to hint, not to specified.

Note:

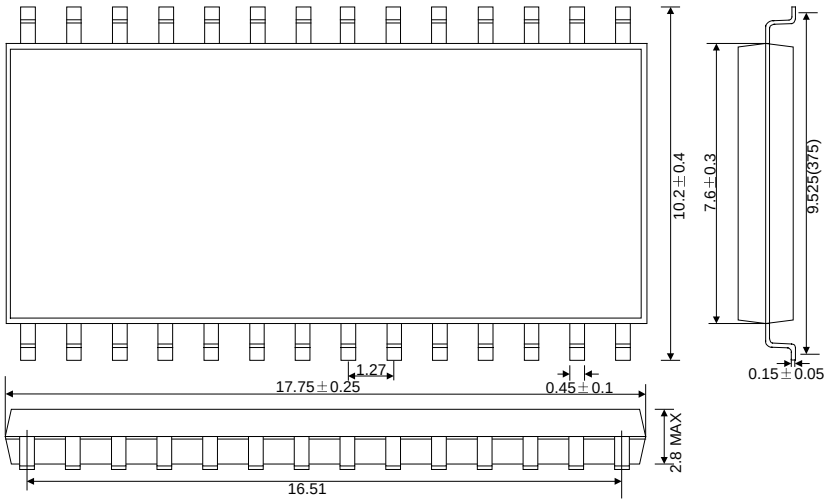
* In wire layout, the power filter capacitor should near to IC.
* In wire layout, should avoid power line and ground line too long.
* Recommended infrared transmit unit and IC ground line should layout separated, or overstriking lines.
* The emitter of triode connect 1Ω resistor at least.
* Recommended triode use 9014.

PACKAGE OUTLINE

DIP-28-600-2.54 UNIT: mm



SOP-28-375-1.27 UNIT: mm



Attach

Revision History

Data	REV	Description	Page
2001.11.07	2.0		
2002.02.28	2.1	Modify the “Absolute maximum rating “	2
		Modify the “Application circuit “	11
		Add the “PCB wire layout schematic”	13
		Modify the “package outline”	14