STK12C68

8K x 8 *AutoStore*™ nvSRAM
QuantumTrap™ CMOS
Nonvolatile Static RAM

SIMTEK

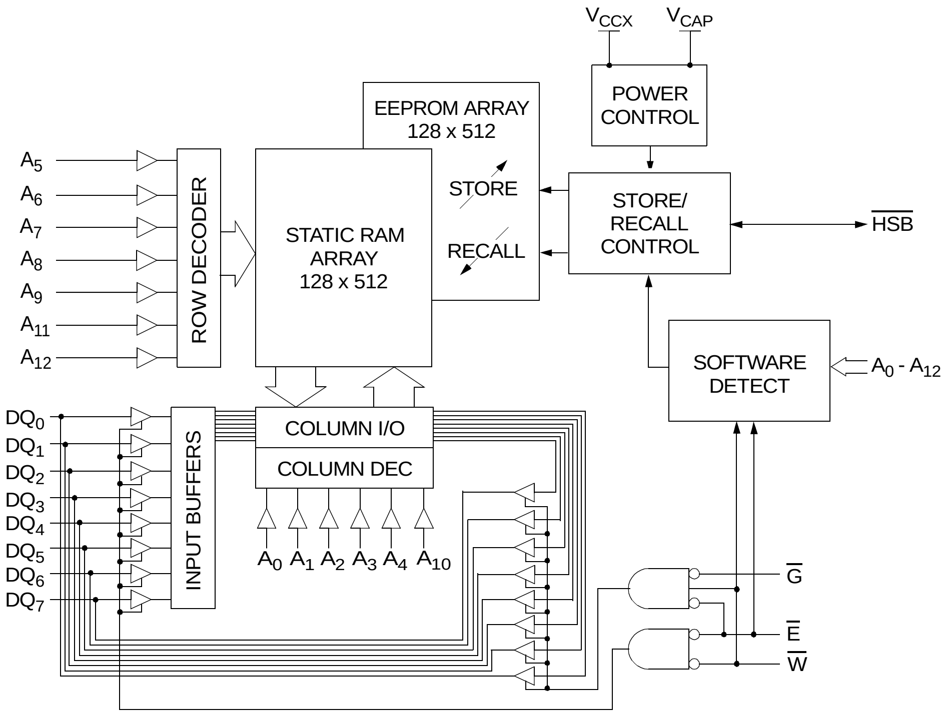
FEATURES

- **20ns, 25ns, 35ns and 45ns Access Times**
- **“Hands-off” Automatic *STORE* with External 68µF Capacitor on Power Down**
- ***STORE* to EEPROM Initiated by Hardware, Software or *AutoStore*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **10mA Typical I_{cc} at 200ns Cycle Time**
- **Unlimited READ, WRITE and *RECALL* Cycles**
- **1,000,000 *STORE* Cycles to EEPROM**
- **100-Year Data Retention in EEPROM**
- **Single 5V ± 10% Operation**
- **Not Sensitive to Power On/Off Ramp Rates**
- **No Data Loss from Undershoot**
- **Commercial and Industrial Temperatures**
- **28-Pin SOIC and DIP Packages**

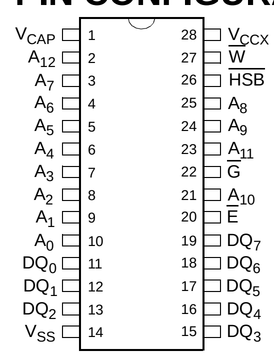
DESCRIPTION

The Simtek STK12C68 is a fast static RAM with a nonvolatile, electrically erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down. A 68µF or larger capacitor tied from V_{CAP} to ground guarantees the *STORE* operation, regardless of power-down slew rate or loss of power from “hot swapping”. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of *STORE* and *RECALL* cycles can also be software controlled by entering specific read sequences. A hardware *STORE* may be initiated with the $\overline{HSB}$ pin.

BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 300 PDIP
28 - 600 PDIP
28 - 350 SOIC
28 - 300 CDIP

PIN NAMES

A_0 - A_{12}	Address Inputs
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{HSB}$	Hardware Store Busy (I/O)
V_{CCX}	Power (+ 5V)
V_{CAP}	Capacitor
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to V_{SS} . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias. . . . . –55°C to 125°C
Storage Temperature . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)[b, f]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[c]	Average V_{CC} Current		100 90 75 65		N/A 90 75 65	mA mA mA mA	t_{AVAV} = 20ns t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[d]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC_3}[c]	Average V_{CC} Current at t_{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\overline{W}$ ≥ (V_{CC} – 0.2V) All Others Cycling, CMOS Levels
I_{CC_4}[d]	Average V_{CAP} Current during *AutoStore*™ Cycle		2		2	mA	All Inputs Don't Care
I_{SB_1}[e]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		32 27 23 20		N/A 28 24 21	mA mA mA mA	t_{AVAV} = 20ns, $\overline{E}$ ≥ V_{IH} t_{AVAV} = 25ns, $\overline{E}$ ≥ V_{IH} t_{AVAV} = 35ns, $\overline{E}$ ≥ V_{IH} t_{AVAV} = 45ns, $\overline{E}$ ≥ V_{IH}
I_{SB_2}[e]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\overline{E}$ ≥ (V_{CC} – 0.2V) All Others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V)
I_{ILK}	Input Leakage Current		±1		±1	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}, $\overline{E}$ or $\overline{G}$ ≥ V_{IH}
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = – 4mA except $\overline{HSB}$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA except $\overline{HSB}$
V_{BL}	Logic "0" Voltage on $\overline{HSB}$ Output		0.4		0.4	V	I_{OUT} = 3mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: The STK12C68-20 requires V_{CC} = 5.0V ± 5% supply to operate at specified speed.
Note c: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note d: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note e: $\overline{E}$ ≥ V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out.
Note f: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels . . . . 0V to 3V
Input Rise and Fall Times. . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . See Figure 1

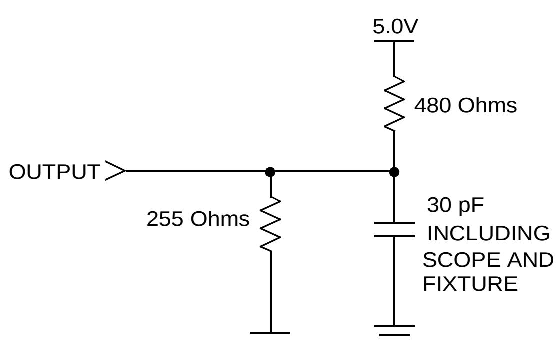


Figure 1: AC Output Loading

CAPACITANCE[g]

(T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note g: These parameters are guaranteed but not tested.

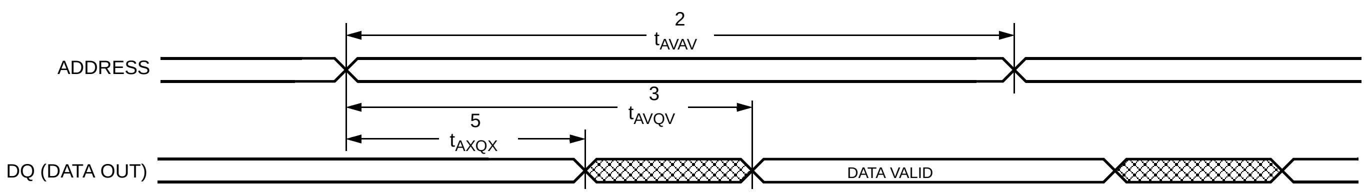
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[b, f]

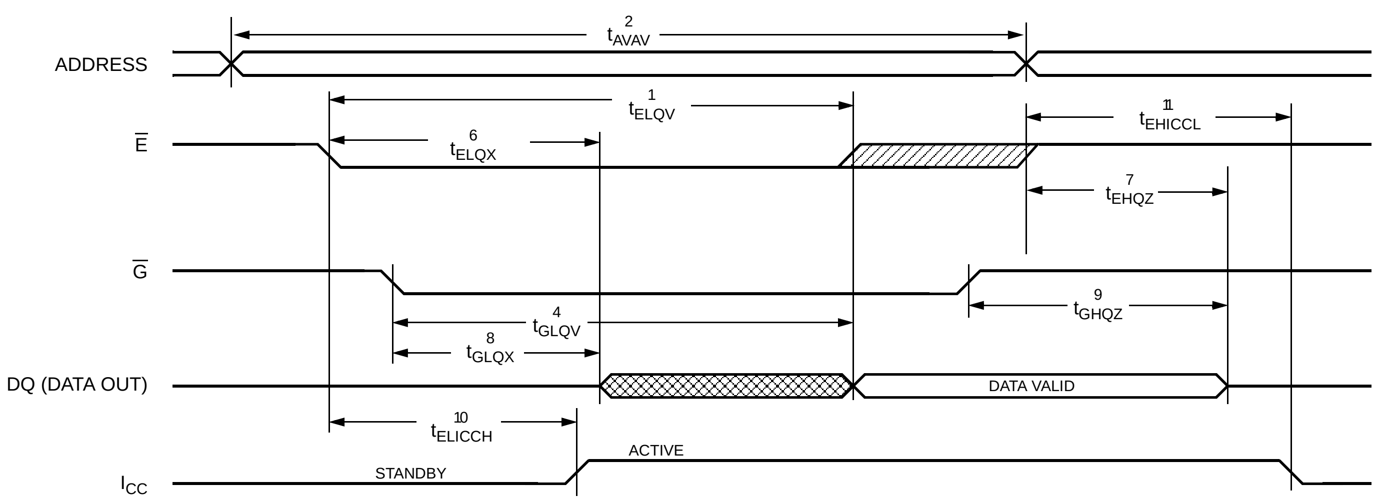
NO.	SYMBOLS #1, #2	SYMBOLS Alt.	PARAMETER	STK12C68-20 MIN	STK12C68-20 MAX	STK12C68-25 MIN	STK12C68-25 MAX	STK12C68-35 MIN	STK12C68-35 MAX	STK12C68-45 MIN	STK12C68-45 MAX	UNITS
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		20		25		35		45	ns
2	t_{AVAV}[h]	t_{RC}	Read Cycle Time	20		25		35		45		ns
3	t_{AVQV}[i]	t_{AA}	Address Access Time		22		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		8		10		15		20	ns
5	t_{AXQX}[i]	t_{OH}	Output Hold after Address Change	5		5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	t_{EHQZ}[j]	t_{HZ}	Chip Disable to Output Inactive		7		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t_{GHQZ}[j]	t_{OHZ}	Output Disable to Output Inactive		7		10		13		15	ns
10	t_{ELICCH}[g]	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t_{EHICCL}[g]	t_{PS}	Chip Disable to Power Standby		25		25		35		45	ns

Note h: $\overline{W}$ and $\overline{HSB}$ must be high during SRAM READ cycles.
Note i: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low.
Note j: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[h, i]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[h]



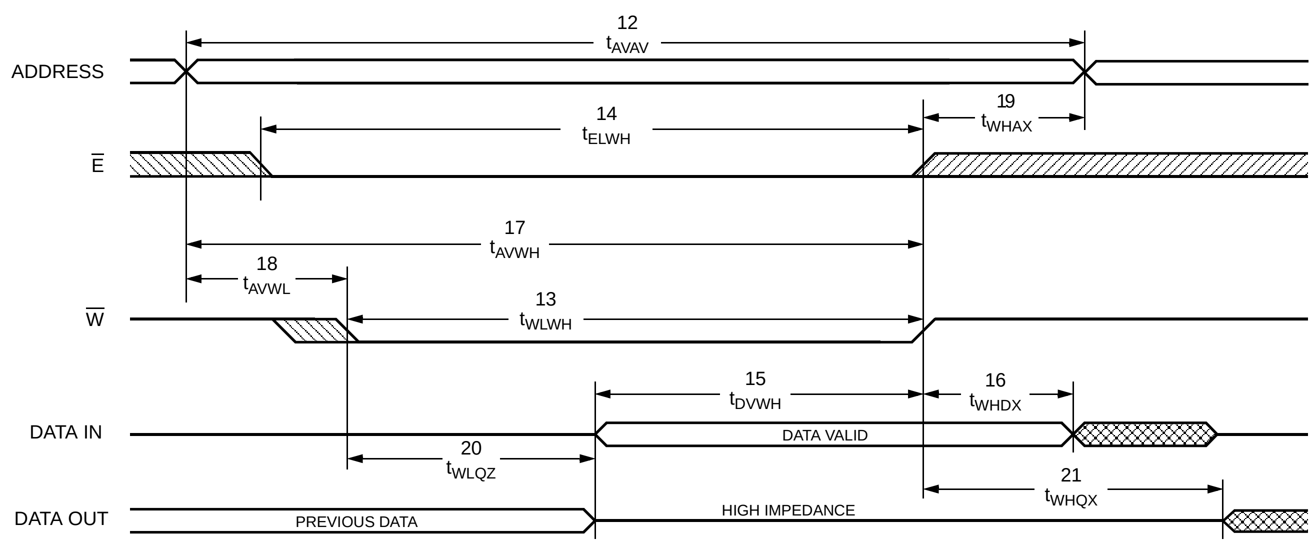
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[b, f]

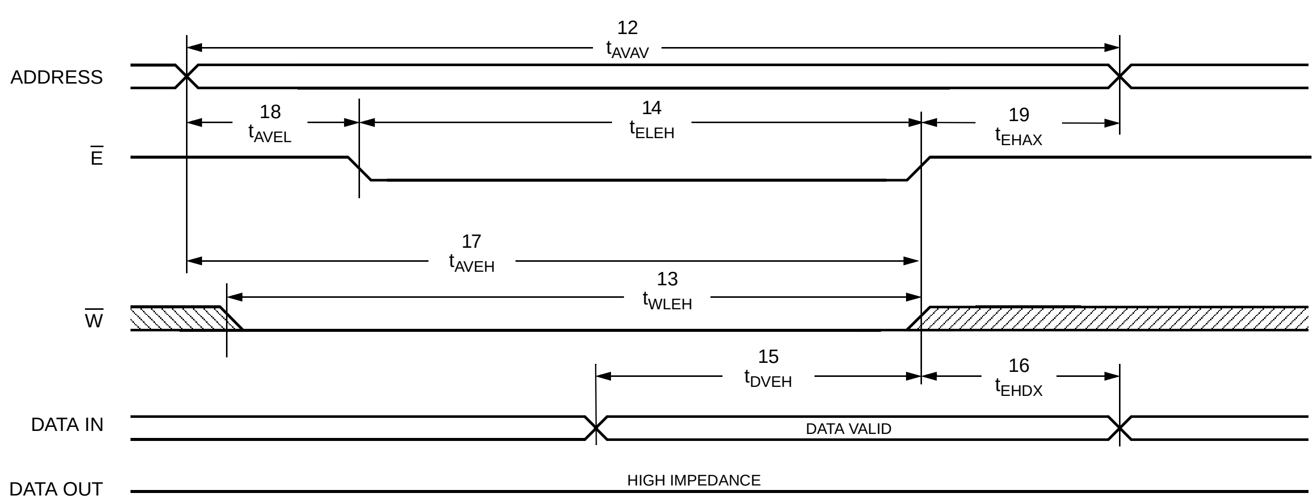
NO.	SYMBOLS #1	SYMBOLS #2	SYMBOLS Alt.	PARAMETER	STK12C68-20 MIN	STK12C68-20 MAX	STK12C68-25 MIN	STK12C68-25 MAX	STK12C68-35 MIN	STK12C68-35 MAX	STK12C68-45 MIN	STK12C68-45 MAX	UNITS
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	20		25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	15		20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	8		10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	15		20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		0		ns
20	t_{WLQZ} [j, k]		t_{WZ}	Write Enable to Output Disable		7		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		5		ns

Note k: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note l: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note m: $\overline{HSB}$ must be high during SRAM WRITE cycles.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[l, m]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[l, m]



HARDWARE MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A_{12} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	p
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile *STORE*	Output High Z	I_{CC_2}	n
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *STORE*	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC_2}	o, p
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *RECALL*	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	o, p

Note n: $\overline{HSB}$ *STORE* operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the *STORE* (if any) completes, the part will go into standby mode, inhibiting all operations until $\overline{HSB}$ rises.
Note o: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note p: I/O state assumes $\overline{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{G}$.

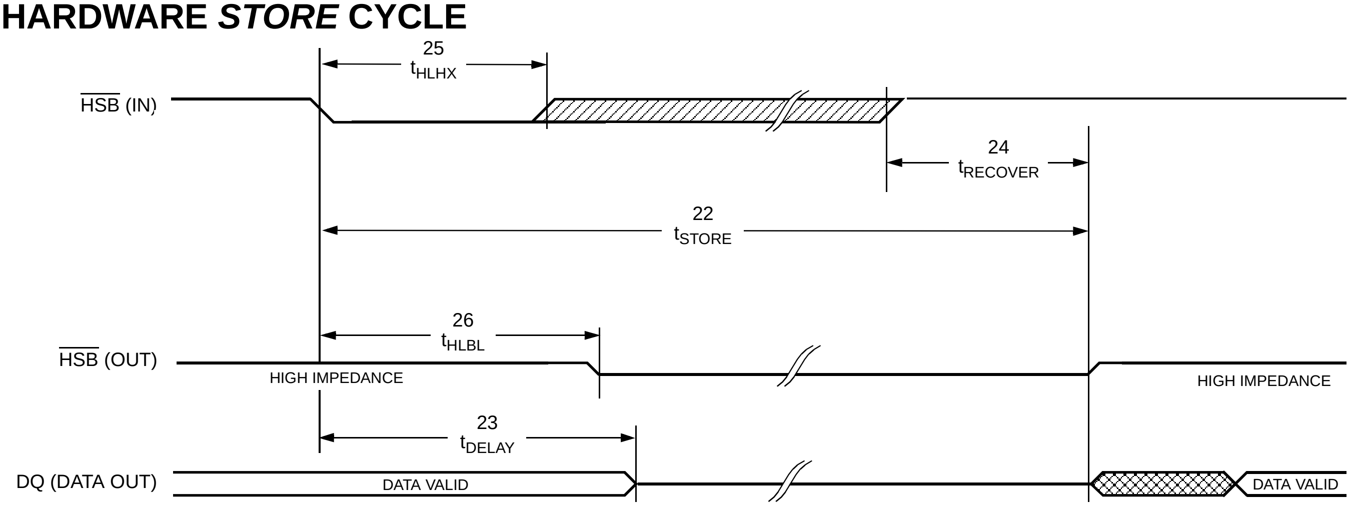
HARDWARE *STORE* CYCLE

$(V_{CC} = 5.0V \pm 10\%)^{b,\ f}$

NO.	SYMBOLS		PARAMETER	STK12C68		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	j, q
23	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	j, r
24	$t_{RECOVER}$	t_{HHQX}	Hardware *STORE* High to Inhibit Off		700	ns	q, s
25	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
26	t_{HLBL}		Hardware *STORE* Low to Store Busy		300	ns	

Note q: $\overline{E}$ and $\overline{G}$ low for output behavior.
Note r: $\overline{E}$ and $\overline{G}$ low and $\overline{W}$ high for output behavior.
Note s: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE *STORE* CYCLE

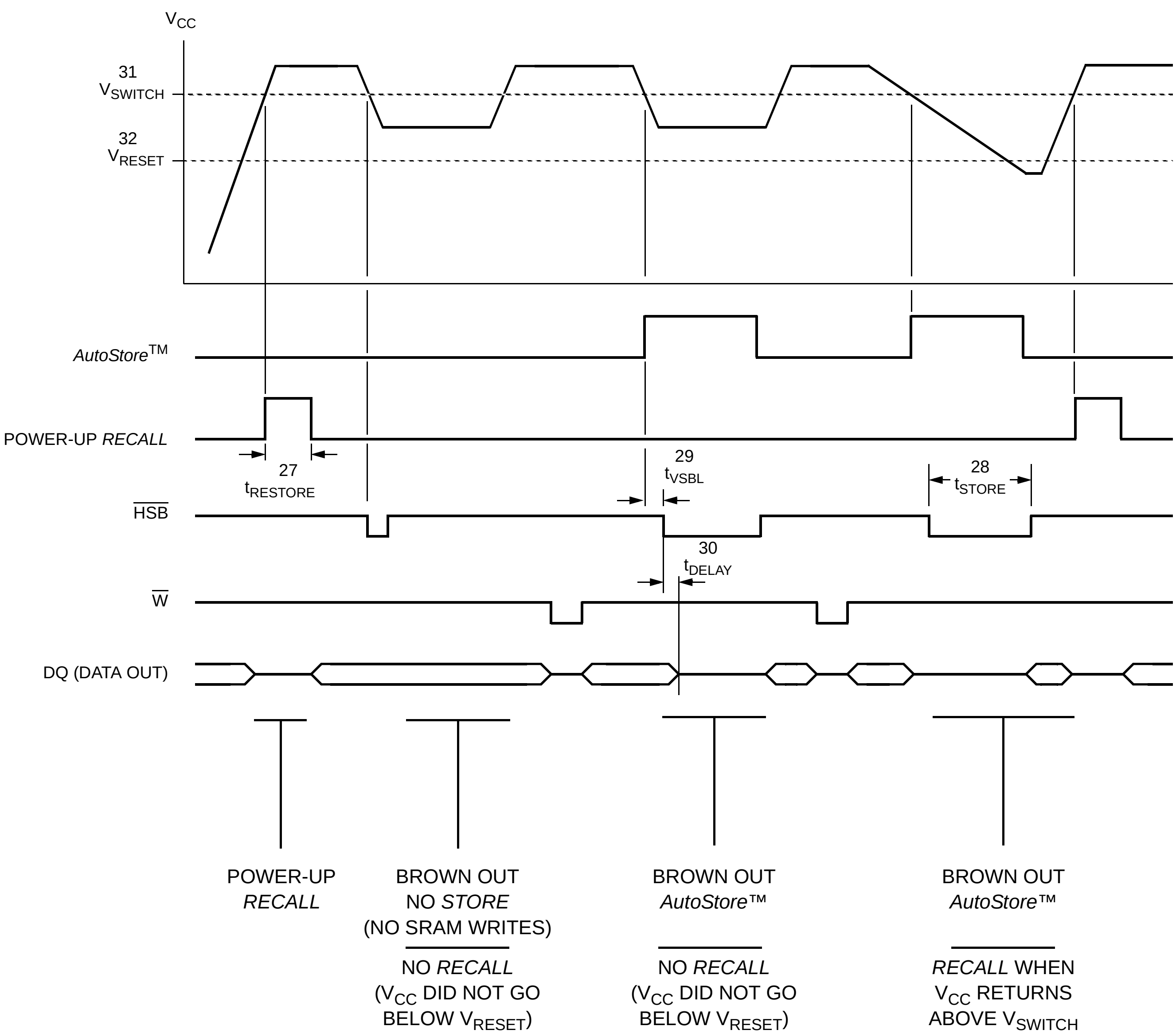


AutoStore™ /POWER-UP *RECALL* (V_{CC} = 5.0V ± 10%)[b, f]

NO.	SYMBOLS		PARAMETER	STK12C68		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	$t_{RESTORE}$		Power-up *RECALL* Duration		550	µs	t
28	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	q, r, u
29	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ Low		300	ns	m
30	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	q
31	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
32	V_{RESET}		Low Voltage Reset Level		3.9	V	

Note t: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note u: $\overline{HSB}$ is asserted low for 1µs when V_{CAP} drops through V_{SWITCH}. If an SRAM WRITE has not taken place since the last nonvolatile cycle, $\overline{HSB}$ will be released and no *STORE* will take place.

AutoStore™ /POWER-UP *RECALL*

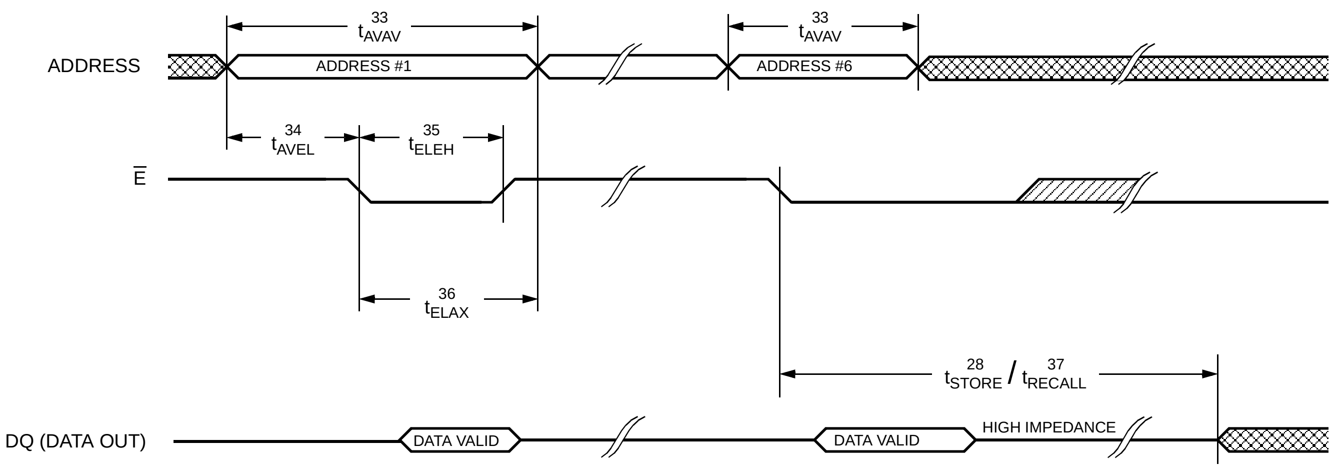


SOFTWARE-CONTROLLED *STORE*/*RECALL* CYCLE[w] ($V_{CC} = 5.0V \pm 10\%$)[b, f]

NO.	SYMBOLS		PARAMETER	STK12C68-20		STK12C68-25		STK12C68-35		STK12C68-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
33	t_{AVAV}	t_{RC}	*STORE*/*RECALL* Initiation Cycle Time	20		25		35		45		ns	q
34	t_{AVEL}	t_{AS}	Address Set-up Time	0		0		0		0		ns	v
35	t_{ELEH}	t_{CW}	Clock Pulse Width	15		20		25		30		ns	v
36	t_{ELAX}		Address Hold Time	15		20		20		20		ns	v
37	t_{RECALL}		*RECALL* Duration		20		20		20		20	µs	

Note v: The software sequence is clocked with $\overline{E}$ controlled READs.
Note w: The six consecutive addresses must be in the order listed in the Hardware Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{E}$ Controlled[w]



DEVICE OPERATION

The STK12C68 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

NOISE CONSIDERATIONS

The STK12C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK12C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-12} determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

POWER-UP *RECALL*

During power up, or after any low-power condition ($V_{CAP} < V_{RESET}$), an internal *RECALL* request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK12C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

SOFTWARE NONVOLATILE *STORE*

The STK12C68 software *STORE* cycle is initiated by executing sequential $\overline{E}$ controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate *STORE* cycle

The software sequence must be clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of $\overline{E}$ controlled READ operations must be performed:

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0E (hex) Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

The STK12C68 can be powered in one of three modes.

During normal *AutoStore*™ operation, the STK12C68 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 68µF and 220µF (± 20%) rated at 6V should be provided.

In system power mode (Figure 3), both V_{CCX} and V_{CAP} are connected to the + 5V power supply without the 68µF capacitor. In this mode the *AutoStore*™ function of the STK12C68 will operate on the stored system charge as power goes down. The user must, however, guarantee that V_{CCX} does not drop below 3.6V during the 10ms *STORE* cycle.

If an automatic *STORE* on power loss is not required, then V_{CCX} can be tied to ground and + 5V applied to V_{CAP} (Figure 4). This is the *AutoStore*™ Inhibit mode, in which the *AutoStore*™ function is disabled. If the STK12C68 is operated in this configuration, references to V_{CCX} should be changed to V_{CAP} throughout this data sheet. In this mode, *STORE* operations may be triggered through software control or the $\overline{HSB}$ pin. It is not permissable to change between these three options "on the fly".

In order to prevent unneeded *STORE* operations, automatic *STORE*s as well as those initiated by externally driving $\overline{HSB}$ low will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to $\overline{HSB}$. This can be used to signal the system that the *AutoStore*™ cycle is in progress.

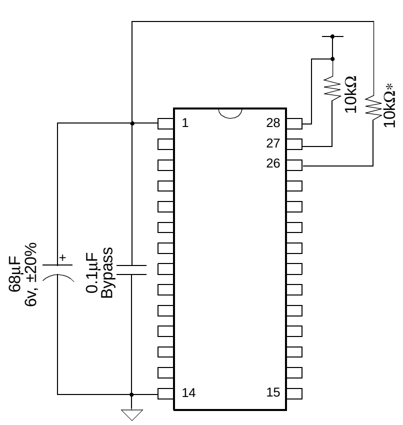


Figure 2: *AutoStore*™ Mode

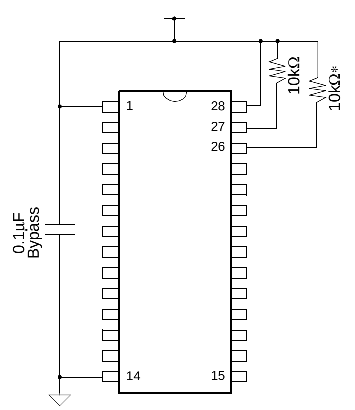


Figure 3: System Power Mode

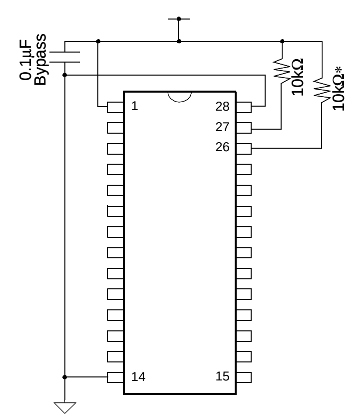


Figure 4: *AutoStore*™ Inhibit Mode

*If $\overline{HSB}$ is not used, it should be left unconnected.

HSB OPERATION

The STK12C68 provides the HSB pin for controlling and acknowledging the *STORE* operations. The HSB pin is used to request a hardware *STORE* cycle. When the HSB pin is driven low, the STK12C68 will conditionally initiate a *STORE* operation after t_{DELAY}; an actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The HSB pin acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when HSB is driven low by any means are given time to complete before the *STORE* operation is initiated. After HSB goes low, the STK12C68 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when HSB is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after HSB goes low will be inhibited until HSB returns high.

The HSB pin can be used to synchronize multiple STK12C68s while using a single larger capacitor. To operate in this mode the HSB pin should be connected together to the HSB pins from the other STK12C68s. An external pull-up resistor to + 5V is required since HSB acts as an open drain pull down. The V_{CAP} pins from the other STK12C68 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK12C68s detects a power loss and asserts HSB, the common HSB pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK12C68s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK12C68 will continue to drive the HSB pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK12C68 will remain disabled until the HSB pin returns high.

If HSB is not used, it should be left unconnected.

PREVENTING STORES

The *STORE* function can be disabled on the fly by holding HSB high with a driver capable of sourcing 30mA at a V_{OH} of at least 2.2V, as it will have to overpower the internal pull-down device that drives HSB low for 20µs at the onset of a *STORE*. When the STK12C68 is connected for *AutoStore*™ operation (system V_{CC} connected to V_{CCX} and a 68µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68 will attempt to pull HSB low; if HSB doesn't actually get below V_{IL}, the part will stop trying to pull HSB low and abort the *STORE* attempt.

HARDWARE PROTECT

The STK12C68 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CAP} < V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs are inhibited.

AutoStore™ can be completely disabled by tying V_{CCX} to ground and applying + 5V to V_{CAP}. This is the *AutoStore*™ Inhibit mode; in this mode, *STORE*s are only initiated by explicit request using either the software sequence or the HSB pin.

LOW AVERAGE ACTIVE POWER

The STK12C68 draws significantly less current when it is cycled at times longer than 50ns. Figure 5 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 6 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK12C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{cc} level; and 7) I/O loading.

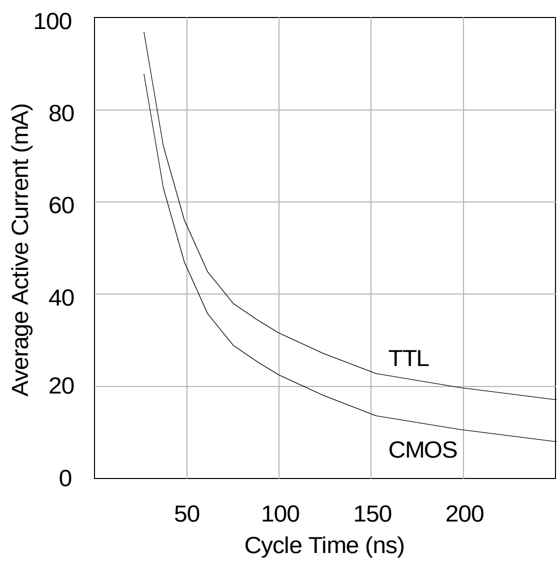


Figure 5: I_{cc} (max) Reads

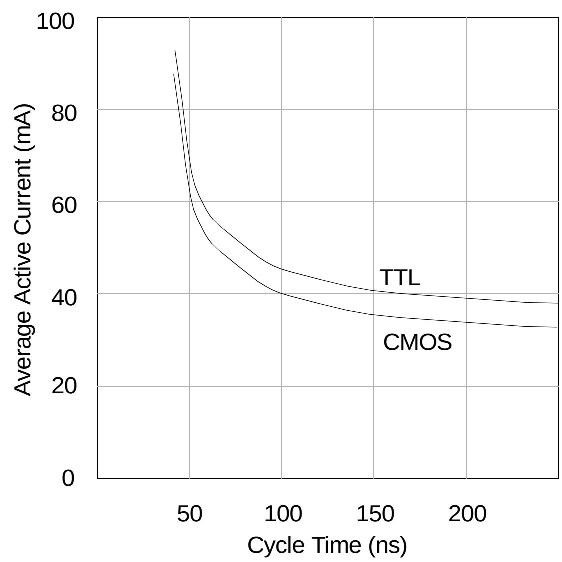


Figure 6: I_{cc} (max) Writes

ORDERING INFORMATION

STK12C68 - P 45 I

Temperature Range
- Blank = Commercial (0 to 70°C)
- I = Industrial (-40 to 85°C)

Access Time
- 20 = 20ns (Commercial only)
- 25 = 25ns
- 35 = 35ns
- 45 = 45ns

Package
- P = Plastic 28-pin 300 mil DIP
- W = Plastic 28-pin 600 mil DIP
- S = Plastic 28-pin 350 mil SOIC
- C = Ceramic 28-pin 300 mil DIP