STK15C68

8K x 8 *AutoStore*™ nvSRAM High Performance CMOS Nonvolatile Static RAM

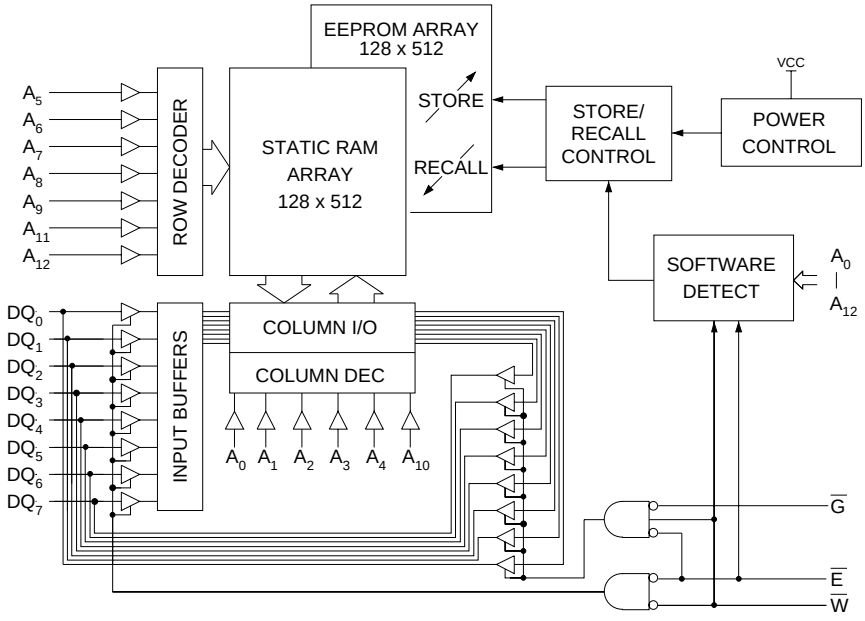
FEATURES

- **Nonvolatile Storage Without Battery Problems**
- **Directly Replaces 8K x 8 static RAM, Battery Backed RAM or EEPROM**
- **25ns, 35ns and 45ns Access Times**
- **Store to EEPROM Initiated by Software or *AutoStore*™ on Power Down**
- **Recall to SRAM by Software or Power Restore**
- **15mA I_{CC} at 200ns Cycle Time**
- **Unlimited Read, Write and Recall Cycles**
- **1,000,000 Store Cycles to EEPROM**
- **100 Year Data Retention Over Full Industrial Temperature Range**
- **Commercial and Industrial Temp. Ranges**
- **28 Pin 600 or 300 mil PDIP and 350 mil SOIC**

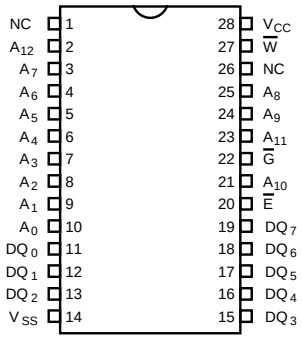
DESCRIPTION

The STK15C68 is a fast SRAM with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to EEPROM (the *STORE* operation) can take place automatically on power down using charge stored in system capacitance. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of STORE and RECALL cycles can also be controlled by entering control sequences on the SRAM inputs. The nvSRAM can be used in place of existing 8K x 8 SRAMs and also matches the pinout of 8k x 8 Battery Backed SRAMs, EPROMs, and EEPROMs, allowing direct substitution while enhancing performance. There is no limit on the number of read or write cycles that can be executed and no support circuitry is required for microprocessor interface.

BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 300 PDIP
28 - 600 PDIP
28 - 350 SOIC

PIN NAMES

A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on input relative to V_{SS} . . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under bias . . . . . –55°C to 125°C
Storage temperature . . . . . –65°C to 150°C
Power dissipation 1W
DC output current 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{cc} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}[b]	Average Current		85 80 75		95 85 80	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC2}[c]	Average Current During STORE		6		7	mA	All inputs Don't Care
I_{CC3}[b]	Average VCC Current at t_{AVAV} = 200ns		15		15	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All others cycling, CMOS levels
I_{CC4}[c]	Average Current During *AutoStore*™ Cycle		4		4	mA	All inputs Don't Care
I_{SB1}[d]	Average Current (Standby, Cycling TTL Input Levels)		35 32 28		39 35 32	mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB2}[d]	Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input pulse levels . . . . . 0V to 3V
Input rise and fall times . . . . . ≤ 5ns
Input and output timing reference levels 1.5V
Output load . . . . . See Figure 1

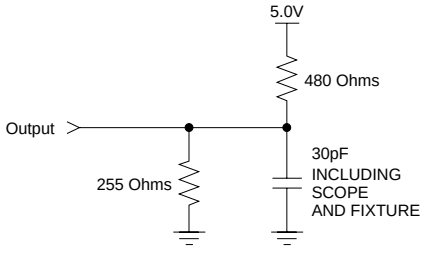


Figure 1: AC Output Loading

CAPACITANCE[e] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

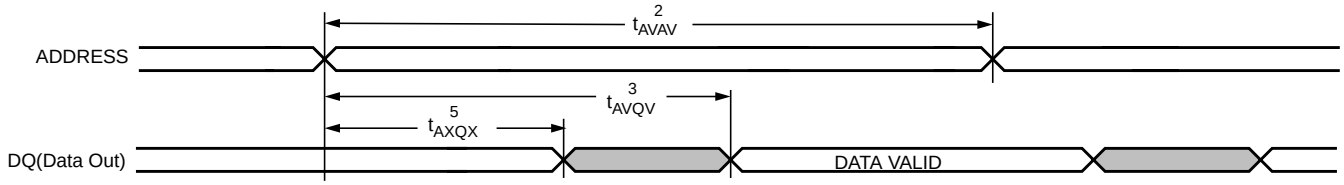
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

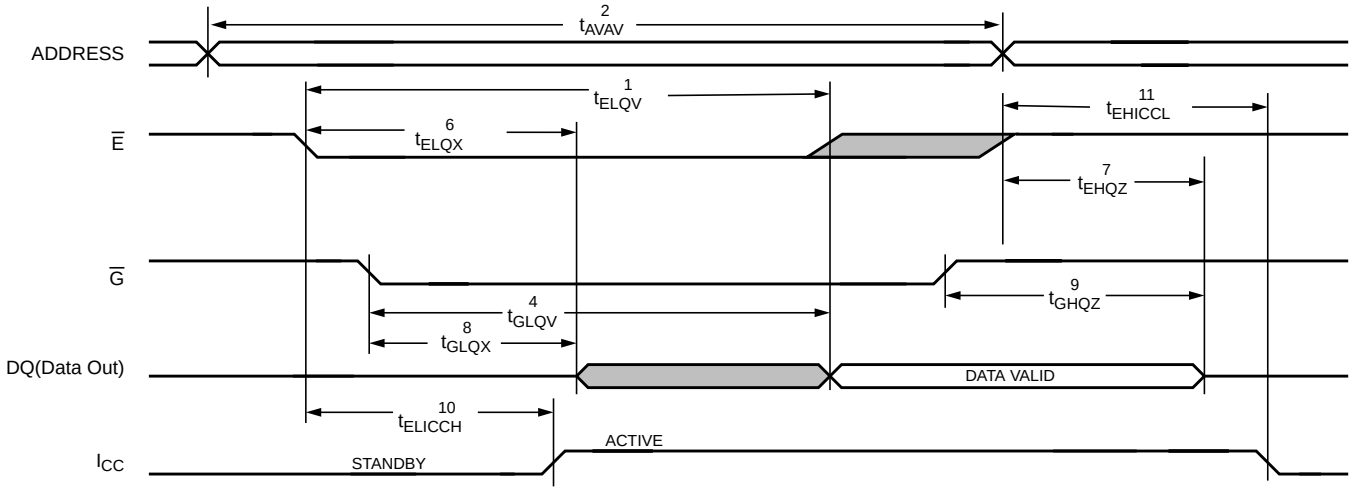
NO.	SYMBOLS		PARAMETER	STK15C68-25		STK15C68-35		STK15C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[f]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		20		25	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold After Address Change	3		3		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		10		17		20	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		10		17		20	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[d, e]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note f: $\overline{W}$ must be high during SRAM read cycles and low during SRAM write cycles.
Note g: I/O state assumes $\overline{E}$, $\overline{G}$, ≤ V_{IL} and $\overline{W}$ ≥ V_{IH}; device is continuously selected
Note h: Measured ± 200mV from steady state output voltage

SRAM READ CYCLE #1 (Address Controlled)[f, g]



SRAM READ CYCLE #2 ($\overline{E}$ Controlled)[f]



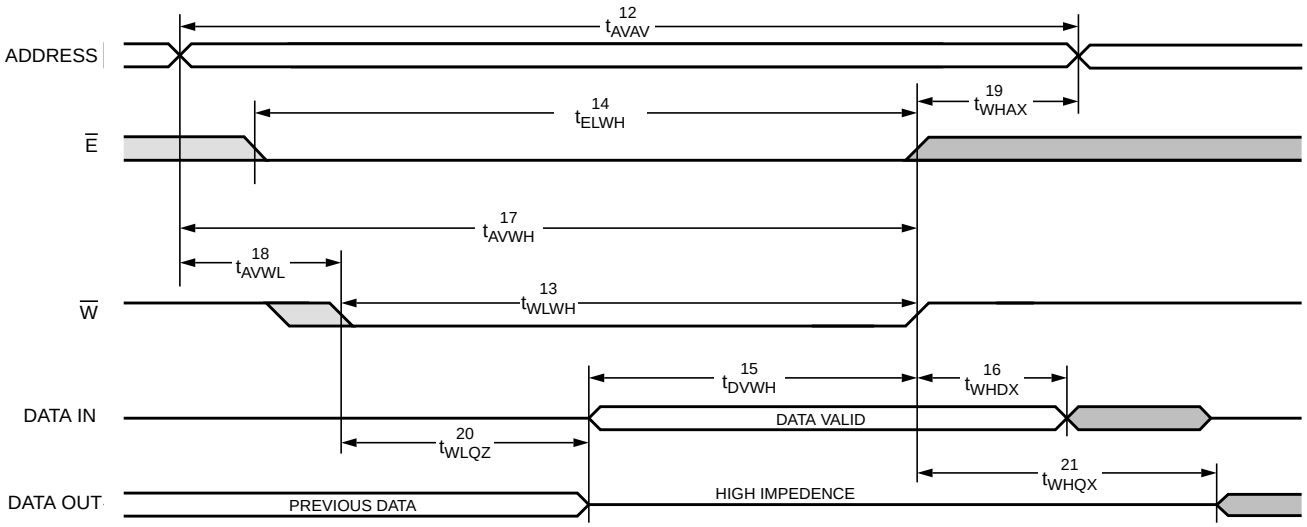
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

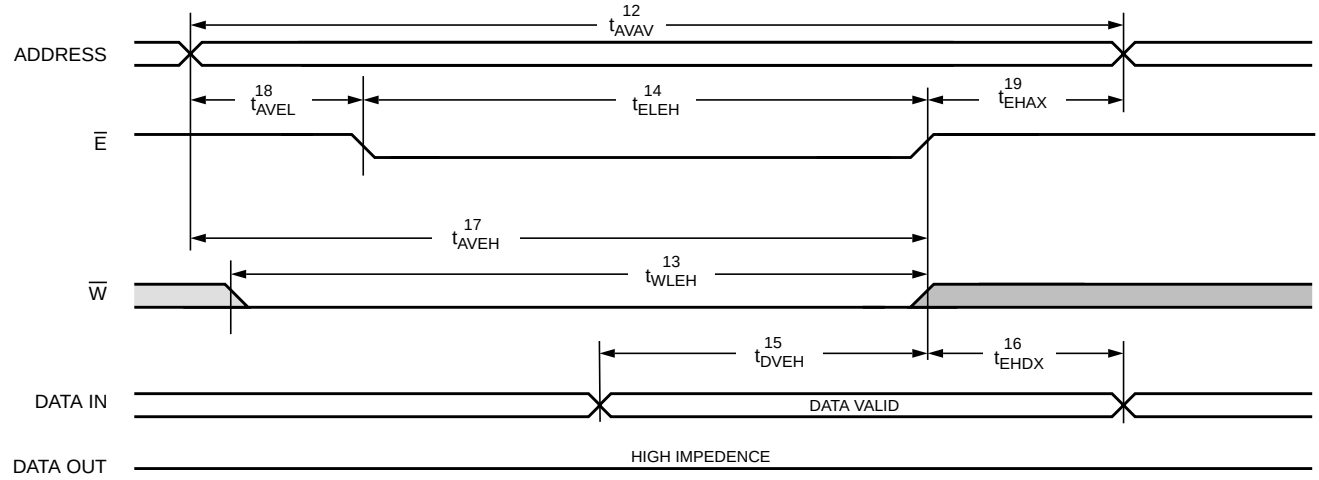
NO.	SYMBOLS			PARAMETER	STK15C68-25		STK15C68-35		STK15C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	t_{WLQZ}[h, i]		t_{WZ}	Write Enable to Output Disable		10		17		20	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low the outputs remain in the high impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ CONTROLLED[j]



SRAM WRITE CYCLE #2: $\overline{E}$ CONTROLLED[j]



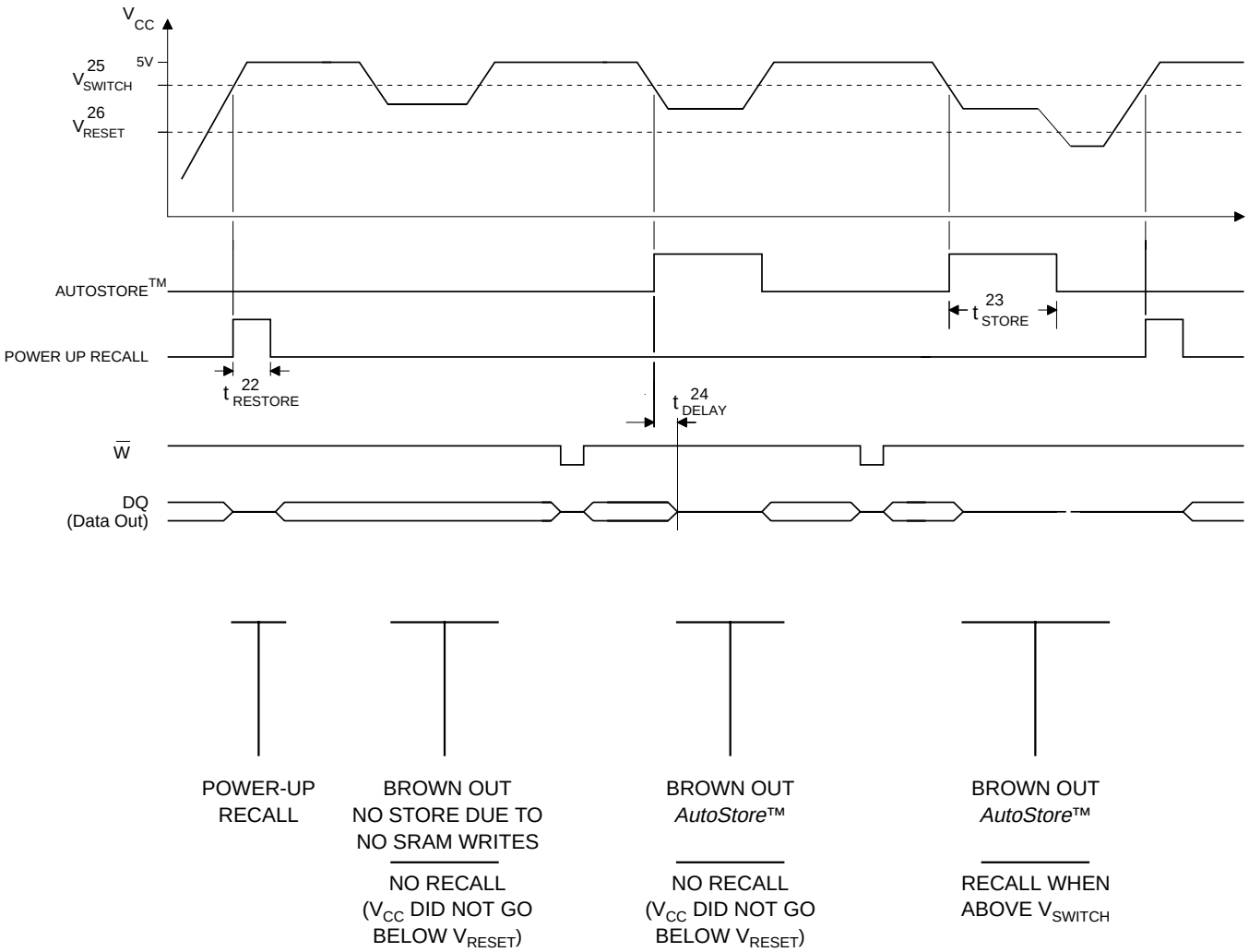
AutoStore™ / POWER-UP RECALL

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK15C68		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power Up RECALL Duration		550	µs	k
23	t_{STORE}	STORE Cycle Duration		10	ms	g
24	t_{DELAY}	Time Allowed to Complete SRAM Cycle	1		µs	g
25	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
26	V_{RESET} [e]	Low Voltage Reset Level		3.6	V	

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

AutoStore™ / POWER UP RECALL



SOFTWARE MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{12} - A_0 (hex)	MODE	I/O with $\overline{G}$ Low	I/O with $\overline{G}$ High	NOTES
L	H	X	0000	Read SRAM	Output data	Output High Z	I
			1555	Read SRAM	Output data	Output High Z	
			0AAA	Read SRAM	Output data	Output High Z	
			1FFF	Read SRAM	Output data	Output High Z	
			10F0	Read SRAM	Output data	Output High Z	
			0F0F	Nonvolatile *STORE*	Output high Z	Output High Z	
L	H	X	0000	Read SRAM	Output data	Output High Z	I
			1555	Read SRAM	Output data	Output High Z	
			0AAA	Read SRAM	Output data	Output High Z	
			1FFF	Read SRAM	Output data	Output High Z	
			10F0	Read SRAM	Output data	Output High Z	
			0F0E	Nonvolatile*RECALL*	Output high Z	Output High Z	

Note l: The six consecutive addresses must be in order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

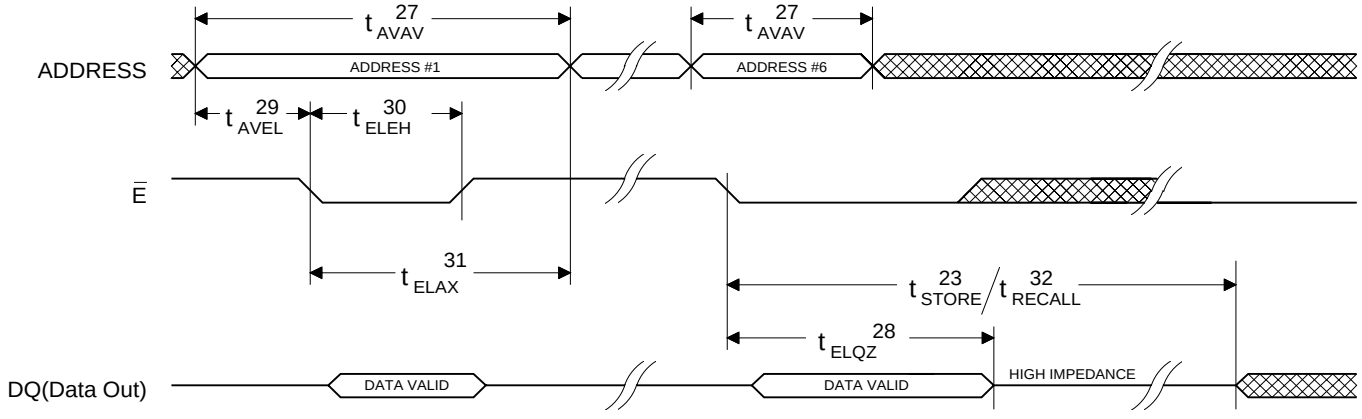
SOFTWARE CYCLES #1 & #2[m,n]

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK15C68-25		STK15C68-35		STK15C68-45		UNITS
	#1		MIN	MAX	MIN	MAX	MIN	MAX	
27	t_{AVAV}	*STORE*/*RECALL* Initiation Cycle Time	25		35		45		ns
28	t_{ELQZ}[g,m]	End of Sequence to Outputs Inactive		650		650		650	ns
29	t_{AVEL}[m]	Address Set-up Time	0		0		0		ns
30	t_{ELEH}[m]	Clock Pulse Width	20		25		30		ns
31	t_{ELAX}[g,m]	Address Hold Time	20		20		20		ns
32	t_{RECALL}	Recall Cycle Duration		20		20		20	µs

Note m: The software sequence is clocked with $\overline{E}$ controlled reads.
Note n: The six consecutive addresses must be in the order listed in the SOFTWARE MODE SELECTION Table - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE: $\overline{E}$ CONTROLLED



DEVICE OPERATION

The STK15C68 is a versatile memory chip that provides several modes of operation. The STK15C68 can operate as a standard 8K x 8 SRAM. It has a 8K x 8 EEPROM shadow to which the SRAM information can be copied, or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK15C68 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK15C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-12} determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high or $\overline{W}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

SOFTWARE NONVOLATILE STORE

The STK15C68 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate STORE cycle

The software sequence is clocked with $\overline{E}$ controlled reads.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

The STK15C68 uses the intrinsic system capacitance to perform an automatic store on power down. As long as the system power supply takes at least t_{STORE} to decay from V_{SWITCH} down to 3.6V the STK15C68 will safely and automatically store the SRAM data in EEPROM on power-down.

In order to prevent unneeded STORE operations, automatic STORE will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place.

POWER UP RECALL

During power up, or after any low power condition (V_{CC} < V_{RESET}) an internal recall request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

HARDWARE PROTECT

The STK15C68 offers hardware protection against inadvertent STORE operation during low voltage conditions. When V_{CC} < V_{SWITCH} Software STORE operations will be inhibited.

LOW AVERAGE ACTIVE POWER

The STK15C68 draws significantly less current when it is cycled at times longer than 55ns. *Figure 2*, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). *Figure 3* shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK15C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CC} level and; 7) I/O loading.

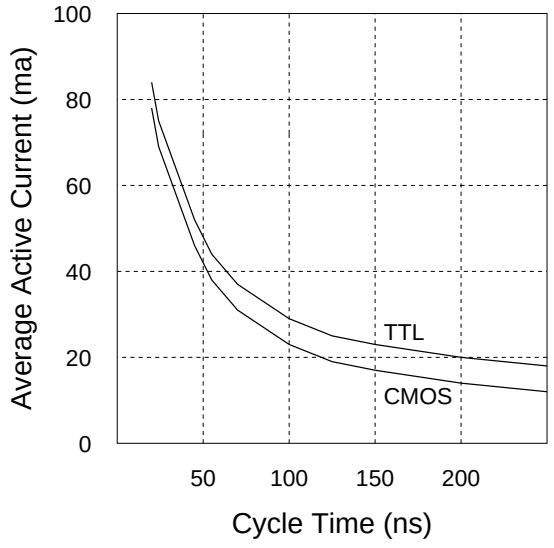


Fig. 2 - Icc (max) Reads

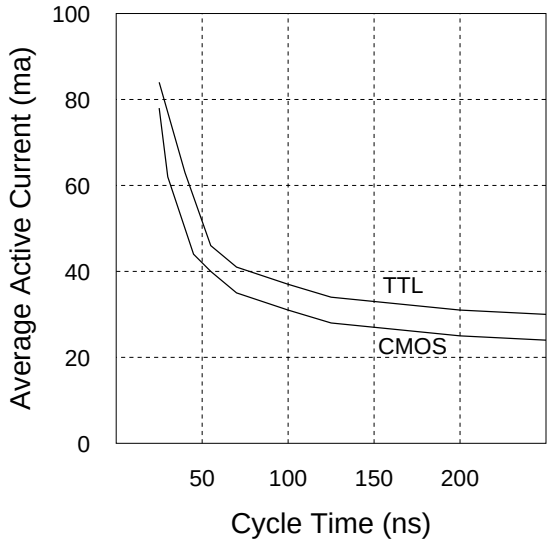
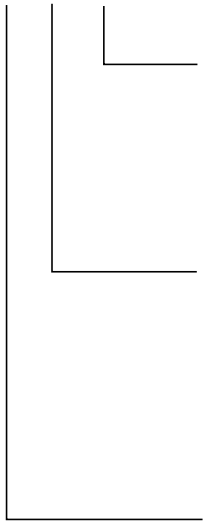


Fig. 3 - Icc (Max) Writes

ORDERING INFORMATION

STK15C68 - W 25 I



Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (–40 to 85 degrees C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

W = Plastic 28 pin 600 mil DIP

P = Plastic 28 pin 300 mil DIP

S = Plastic 28 pin 350 mil SOIC