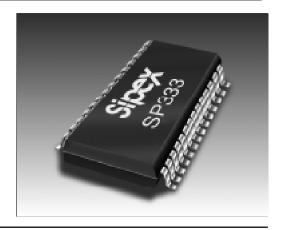


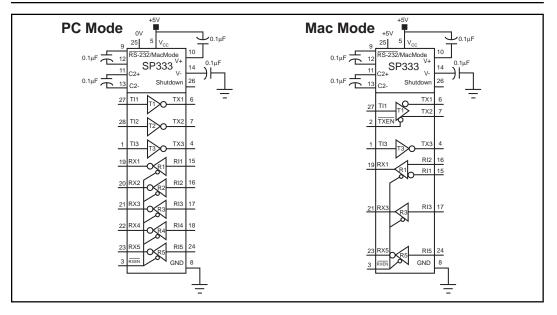
+5V Only RS-232/AppleTalk[™] Programmable Transceiver

- +5V Only, Single Supply Operation
- Low Power Shutdown
- 28-Pin SOIC Packaging
- 3 Drivers, 5 Receivers RS-232
- Complete AppleTalk[™] Interface
- High Data Rates
 10Mbps Differential Transceivers
 460kbps Single-Ended Transceivers



DESCRIPTION...

The **SP333** is a monolithic device that supports both Macintosh[™] and PC serial interfaces. RS-232 mode offers three (3) RS-232 drivers and five (5) RS-232 receivers. Mac mode includes a differential driver and a single-ended inverting driver. Receivers in Mac mode include one differential receiver, one non-inverting single-ended receiver and one inverting single-ended receiver. An on-chip charge pump allows +5V-only operation, and a low power Shutdown mode makes the **SP333** ideal for battery powered applications. The interface mode can be changed at any time by a mode select pin.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V _{cc}	+12V
Input Voltages	
Logic	0.3V to (V _{cc} +0.5V)
Drivers	0.3V to (V _{cc} +0.5V)
Receivers	±15V
Driver Outputs	±14V
Storage Temperature	65°C to +150°C
Power Dissipation	1000mW

SPECIFICATIONS

 $\rm T_{_{MIN}}$ to $\rm T_{_{MAX}}$ and $\rm V_{_{CC}}$ = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX. UNITS CONDITIONS		CONDITIONS
MAC Mode (pin 25 = +5V) Differential Driver High Level Output Voltage Low Level Output Voltage Differential Output, Load Differential Output, No Load Driver Short Circuit Current Output Leakage Current Input High Voltage Input Low Voltage Input Current		±5V ±40	-3.6 ±10 500 ±100 0.8 ±20	Volts Volts Volts Volts mA μA Volts Volts μA	$I_{OH} = 8mA$ $I_{OH} = -8mA$ $R_{L} = 450\Omega \text{ (TX outputs to GND)}$ $R_{L} = \infty$ $-7V \le V_{O} \le +7V; V_{IN \ LOW} \le 0.8V \text{ or}$ $V_{IN \ HIGH} \ge 2.0V$ $-7V \le V_{O} \le +7V; \ \overline{TxEN} = V_{CC}$ Applies to differential driver inputs Applies to differential driver inputs $V_{IN} = 0V \text{ to } V_{CC}$
Transition Time Propagation Delay t _{PHL} Data Rate	10	30 100 100		ns ns ns Mbps	$\begin{aligned} & R_{L}^{L} = 450\Omega, \ C_{L}^{C} = 50pF; \ Rise/Fall \\ & 10\% - 90\% \end{aligned}$ $\begin{aligned} & R_{L} = 450\Omega, \ C_{L} = 50pF \\ & R_{L} = 450\Omega, \ C_{L} = 50pF \\ & R_{L} = 450\Omega, \ C_{L} = 50pF \end{aligned}$
Single-Ended Inverting Drive High Level Output Voltage Low Level Output Voltage	+3.6 -6.0		+6.0 -3.6	Volts Volts	R_L = 450Ω to GND; $V_{IN LOW}$ ≤0.8V or $V_{IN HIGH}$ ≥2.0V R_L = 450Ω to GND; $V_{IN LOW}$ ≤0.8V or $V_{IN HIGH}$ ≥2.0V
Driver Open Circuit Voltage Driver Short Circuit Current Input High Voltage Input Low Voltage Input Current Transition Time	2.0	±40 30	±10 0.8 ±20	Volts mA Volts Volts μA ns	$ \begin{array}{l} R_{L}^{INOFIN} = \infty \\ -7V{\leq}V_{O}{\leq}{+}7V; \mbox{ Infinite duration} \\ Applies to single-ended driver inputs \\ Applies to single-ended driver inputs \\ V_{IN} = 0V \mbox{ to } V_{CC} \\ R_{L} = 450\Omega, \mbox{ C}_{L} = 50pF; \mbox{ Rise/Fall} \\ 10\% - 90\% \end{array} $
Propagation Delay t _{PHL} t _{PLH} Data Rate	10	100 100		ns ns Mbps	$\begin{array}{l} {\sf R}_{\sf L} = 450\Omega, \ {\sf C}_{\sf L} = 50 {\sf p} {\sf F} \\ {\sf R}_{\sf L} = 450\Omega, \ {\sf C}_{\sf L} = 50 {\sf p} {\sf F} \\ {\sf R}_{\sf L} = 450\Omega, \ {\sf C}_{\sf L} = 50 {\sf p} {\sf F} \end{array}$
Differential Receiver Differential Input Threshold Input Hysteresis Input Resistance Output Voltage High Output Voltage Low Short Circuit Current	-0.2 12 3.5	70	+0.2 0.4 85	Volts mV kΩ Volts Volts mA	$\begin{array}{c} -7V \leq V_{CM} \leq +7V \\ V_{CM} = 0V \\ -7V \leq V_{CM} \leq +7V \\ I_{SOURCE} = -4mA \\ I_{SINK} = +4mA \\ 0V \leq V_{OUT} \leq V_{CC} \end{array}$

SPECIFICATIONS (CONTINUED)

 T_{MN} to T_{MAX} and $V_{CC} = 5V\pm5\%$ unless otherwise noted.

T_{MIN} to T_{MAX} and $V_{CC} = 5V\pm5\%$ unless otherwise noted.						
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
Differential Receiver Propagation Delay t _{PHL} Data Rate	10	100 100		ns ns Mbps	$R_L = 450\Omega, C_L = 50pF$ $R_L = 450\Omega, C_L = 50pF$ $R_1 = 450\Omega, C_1 = 50pF$	
Single-Ended Inverting Rece Input Voltage Range Input Threshold Low Input Threshold High Hysteresis Input Impedance Output Voltage High Output Voltage Low Propagation Delay t_{PHL} t_{PLH} Data Rate	2000 2000 3 3.5 10	1.2 1.7 500 5	+15 3.0 1000 7 0.4	Volts Volts mV kΩ Volts Volts Ns ns Mbps	I _{SOURCE} = -4mA I _{SINK} = +4mA	
$\begin{array}{c} \textbf{Single-Ended Non-Inverting} \\ Input Voltage Range \\ Input Threshold Low \\ Input Threshold High \\ Hysteresis \\ Input Impedance \\ Output Voltage High \\ Output Voltage Low \\ Propagation Delay \\ t_{\text{PHL}} \\ t_{\text{PLH}} \\ t_{\text{PLH}} \\ \text{Data Rate} \end{array}$	Receiver -7 -0.2 12 3.5	70 15 100 100	+7 +0.2 0.4	Volts Volts WV kΩ Volts Volts ns ns Mbps	I _{SOURCE} = -4mA I _{SINK} = +4mA	
PC Mode (pin 25 = GND)RS-232 DriverTTL Input Levels V_{IL} V_{H} High Level Voltage OutputLow Level Voltage OutputOpen Circuit OutputShort Circuit CurrentPower Off ImpedanceSlew RateTransition TimePropagation Delay t_{PLH} Data Rate	2.0 +5.0 -15.0 300	60 1.5 1.3 600	0.8 +15.0 -5.0 ±15 ±100 1.56	Volts Volts Volts Volts Volts mA Ohms V/μs μs μs kbps	Applies to transmitter inputs Applies to transmitter inputs R _L = 3k\Omega to Gnd R _L = 3k\Omega to Gnd R _L = ∞ V _{OUT} = Gnd V _{CC} =0V; V _{OUT} = $\pm 2V$ R _L =3k Ω , C _L =50pF; From +3V to -3V or -3V to +3V Rise/fall time, between +3V & -3V ; R _L =3k Ω , C _L =1000pF; From 1.5V of T _{IN} to 50% of V _{OUT} R _L =3k Ω , C _L =1000pF; From 1.5V of T _{IN} to 50% of V _{OUT} R _L =3k Ω , C _L =1000pF	
RS-232 Receiver TTL Output Levels V _{OL} V _{OH} Receiver Input High Threshold	2.4	1.7	0.4 3.0	Volts Volts	I _{SINK} = 4mA I _{SOURCE} = -4mA	

SPECIFICATIONS (CONTINUED)

 T_{MN} to T_{MAX} and $V_{CC} = 5V\pm5\%$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 Receiver Low Threshold Input Voltage Range Input Impedance Hysteresis Transmission Rate Propagation Delay t _{PHL}	0.8 -15 3 0.2 10	1.2 5 0.5	+15 7 1.0	Volts Volts kOhms Volts Mbps ns	$V_{IN}=\pm 15V$ $V_{cc}=+5V$ From 50% of V_{IN} to 1.5V of R_{OUT} From 50% of V_{IN} to 1.5V of R_{OUT}
t _{PLH} Data Rate	460	100 600	600	ns kbps	
POWER REQUIREMENTS No Load Supply Current Shutdown Supply Current		15	25 75	mA μA	No load; V _{cc} =5.0V; T _A =25°C T _A =25°C, V _{cc} =5.0V
AC PARAMETERS Differential Mode t _{PZL} ; Enable to Output low t _{PZH} ; Enable to Output high t _{PLZ} ; Disable from Output low t _{PHZ} ; Disable from Output high		200 200 200 200	1000 1000 1000 1000	ns ns ns ns	C_L =100pF, Figures 2 & 4, S ₂ closed C_L =100pF, Figures 2 & 4, S ₁ closed C_L =15pF, Figures 2 & 4, S ₂ closed C_L =15pF, Figures 2 & 4, S ₁ closed
Receiver Delay Time from Enable Mode to Tri-state Mode					
Single-Ended Mode t _{PZL} ; Enable to Output low t _{PZH} ; Enable to Output high t _{PLZ} ; Disable from Output low t _{PHZ} : Disable from Output high		200 200 200 200	1000 1000 1000 1000	ns ns ns ns	C_{RL} =15pF, Figures 1 & 6, S ₁ closed C_{RL} =15pF, Figures 1 & 6, S ₂ closed C_{RL} =15pF, Figures 1 & 6, S ₁ closed C_{RL} =15pF, Figures 1 & 6, S ₂ closed
Differential Mode t_{PZL} ; Enable to Output low t_{PZH} ; Enable to Output high t_{PLZ} ; Disable from Output low t_{PHZ} ; Disable from Output high		200 200 200 200	1000 1000 1000 1000	ns ns ns ns	$\begin{array}{l} C_{\textrm{RL}} = 15\textrm{pF}, \ \textrm{Figures 1 \& 6, S}_{1} \ \textrm{closed} \\ C_{\textrm{RL}} = 15\textrm{pF}, \ \textrm{Figures 1 \& 6, S}_{2} \ \textrm{closed} \\ C_{\textrm{RL}} = 15\textrm{pF}, \ \textrm{Figures 1 \& 6, S}_{1} \ \textrm{closed} \\ C_{\textrm{RL}} = 15\textrm{pF}, \ \textrm{Figures 1 \& 6, S}_{2} \ \textrm{closed} \end{array}$
Notes:1.Measured from 2.5\2.Measured from one3.Measured from 1.5\4.Measured from 2.5\	⊢half of R / of T _{i⊾} to	_{iN} to 2.5V o one–half o	of R _{out} .		

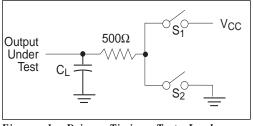


Figure 1. Driver Timing Test Load Circuit

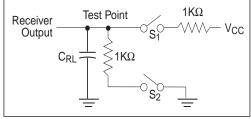


Figure 2. Receiver Timing Test Load Circuit

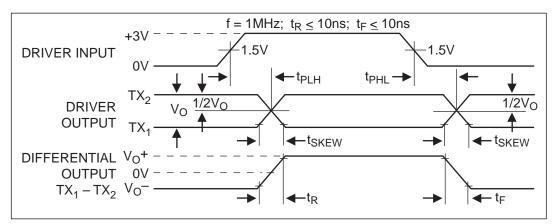


Figure 3. Driver Propagation Delays

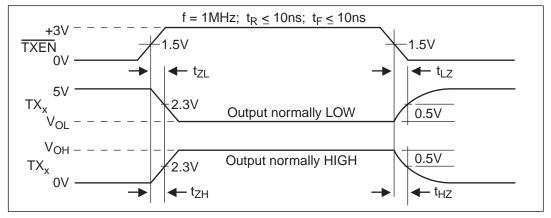


Figure 4. Driver Enable and Disable Times

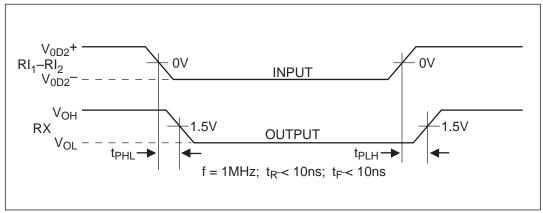


Figure 5. Receiver Propagation Delays

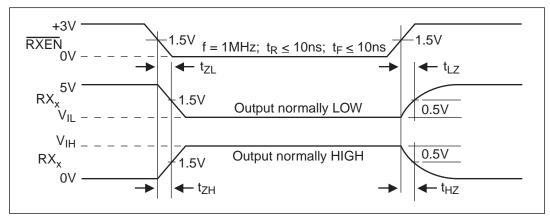


Figure 6. Receiver Enable and Disable Times

THEORY OF OPERATION...

The **SP333** is a single chip device that can be configured via software for either RS-232 or AppleTalkTM interface modes at any time. The **SP333** is made up of three basic circuit elements: single-ended drivers and receivers, differential drivers and receivers, and charge pump.

APPLETALK™ DRIVERS/RECEIVERS...

To program the **SP333** for MacMode, Pin 25 should be connected to a logic HIGH. In MacMode, the **SP333** offers a complete AppleTalk serial interface.

The driver section of the AppleTalk interface is made up of a differential driver and a singleended inverting driver. The differential driver has voltage swings that are typically $\pm 5V$ on each output pin under loaded conditions, and typically $\pm 8V$ under no-load conditions. The differential driver can maintain $\pm 3.6V$ (minimum) swings (per pin) under worst case load conditions of 450Ω between the differential output.

The differential driver is equipped with a tristate control pin. When TXEN is a logic LOW, the differential driver is active. When the TXEN pin is a logic HIGH, the differential driver outputs are tri-stated. The TXEN pin only functions in MacMode. The differential AppleTalk driver can support data rates up to 10Mbps. The single-ended AppleTalk driver also has typical voltage output swings of $\pm 5V$ under loaded conditions, and $\pm 8V$ under no-load conditions. The single-ended AppleTalk driver can maintain $\pm 3.6V$ (minimum) swings under worst case conditions of 450Ω to ground. The single-ended AppleTalk driver can support data rates over 400kbps.

The receiver section of the **SP333** is made up of a differential receiver, a single-ended non-inverting receiver, and a single-ended inverting receiver. The differential receiver has an input sensitivity of ± 200 mV over a common mode range of ± 7 V. The receivers have a typical input resistance of 15k Ω (12k Ω minimum). The differential receiver can receive data up to 10Mbps.

The single-ended non-inverting receiver has a ± 200 mV input threshold, however, the input voltage can vary between ± 7 V. The typical input resistance of the single-ended non-inverting receiver is 15k Ω (12k Ω minimum). The single-ended non-inverting receiver can also receive data up to 10Mbps.

The **SP333** also has a single-ended inverting receiver input. This receiver is basically an RS-232 receiver (R5 receiver) and is typically used as a GPI (General Purpose Input) in the AppleTalk interface. The GPI input has TTL-compatible input thresholds that can receive

signals up to ± 15 V. The input resistance of the single-ended inverting receiver is typically 5k Ω (3k Ω to 7k Ω). The GPI receiver can operate up to 10Mbps.

SINGLE ENDED DRIVERS/RECEIVERS...

RS-232 (V.28) Drivers...

The single-ended drivers and receivers comply the with the RS-232E and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is ±9V with no load and is guaranteed to be greater than $\pm 5V$ under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of $3k\Omega$ and 2500pF, the four RS-232 drivers can still maintain ±5V output levels. The drivers can operate over 400kbps; the propagation delay from input to output is typically 1.5µs. During shutdown, the driver outputs will be put into a high impedance tri-state mode.

RS-232 (V.28) Receivers...

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four

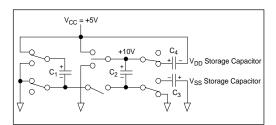


Figure 7. Charge Pump Phase 1

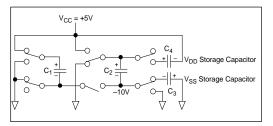


Figure 9. Charge Pump Phase 3

receivers features 500mV of hysteresis margin to minimize the affects of noisy tranmission lines. The inputs also have a $5k\Omega$ resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic HIGH state. The input resistance will maintain $3k\Omega$ - $7k\Omega$ over a $\pm 15V$ range. The maximum operating voltage range for the receiver is $\pm 30V$, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on-chip ESD protection circuitry, the receiver inputs will be clamped to $\pm 15V$ levels; this should not affect operation at $\pm 30V$ olts. The RS-232 receivers can operate over 400kbps.

CHARGE PUMP...

The charge pump is a Sipex-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. The capacitor values of the **SP333** can be as low as 0.1μ F. *Figure 11a* shows the waveform found on the positive side of capacitor C2, and *Figure 11b* shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

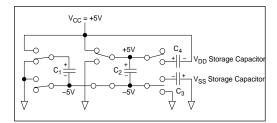


Figure 8. Charge Pump Phase 2

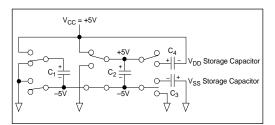


Figure 10. Charge Pump Phase 4

Phase 1

-Vss charge storage- During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

Phase 2

-Vss transfer- Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

Phase 3

-Vdd charge storage- The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is 10V.

Phase 4

-Vdd transfer- The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated 10V across C2 to C4,

the Vdd storage capacitor. Simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors should be 0.1μ F with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V- pins. The value of the external supply voltages must be no greater than $\pm 10V$. The current drain from the $\pm 10V$ supplies is used for the RS-232 drivers. For the RS-232 driver, the current requirement is 3.5mA per driver. The external power supplies should provide a power supply sequence of either: $\pm 10V$, $\pm 10V$, and then $\pm 5V$; or $\pm 10V$, and then $\pm 5V$. It is critical that the $\pm 10V$ supplies are on before V_{CC} .

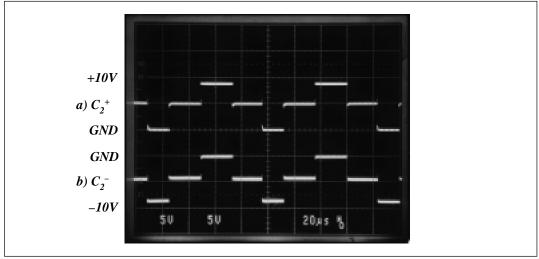


Figure 11. Charge Pump Waveforms

Shutdown Mode

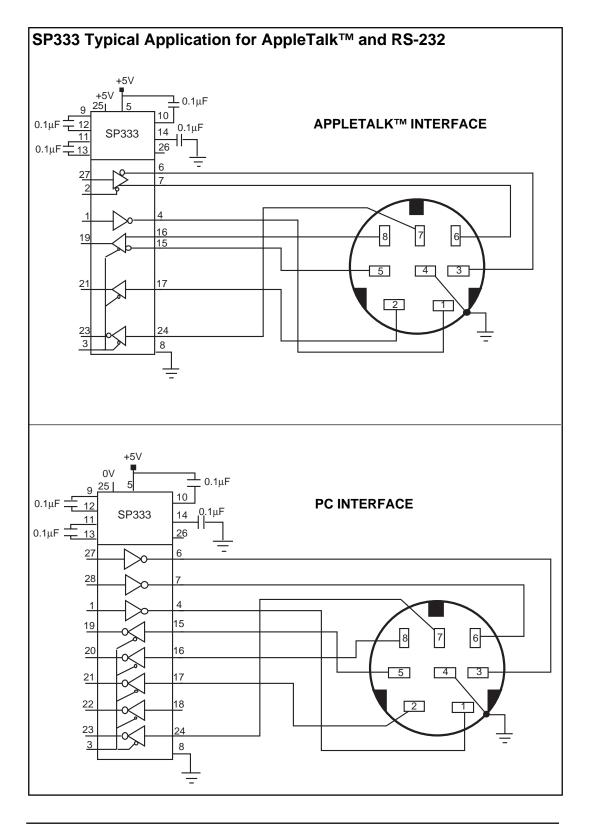
The **SP333** can be put into a low power shutdown mode by connecting the Shutdown pin (SD, Pin 26) to a logic HIGH. During Shutdown, the driver outputs are put into a high impedance tri-state, and the charge pump is put into stand-by mode. The supply current drops to less than 10 μ A during shutdown and can be activated in either RS-232 or AppleTalk mode. For normal operation, the SD pin should be connected to a logic LOW.

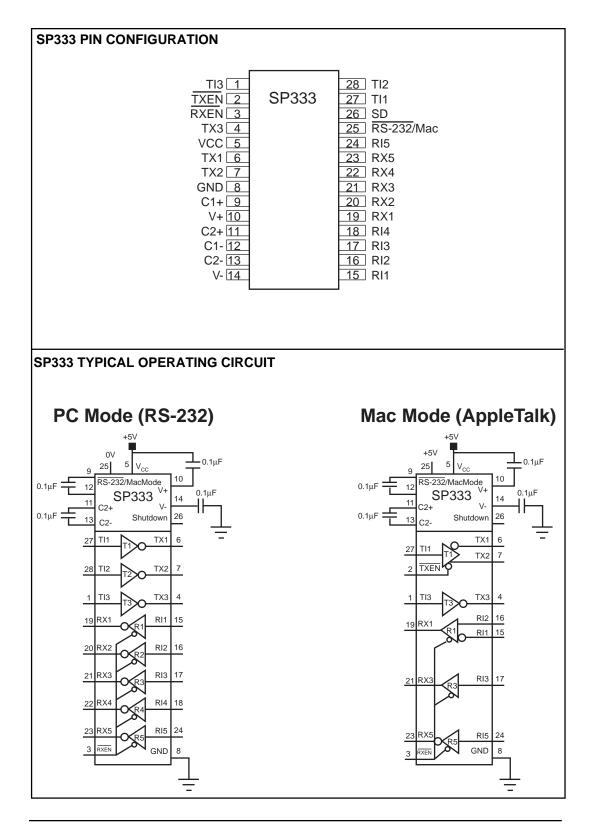
Receiver Enable

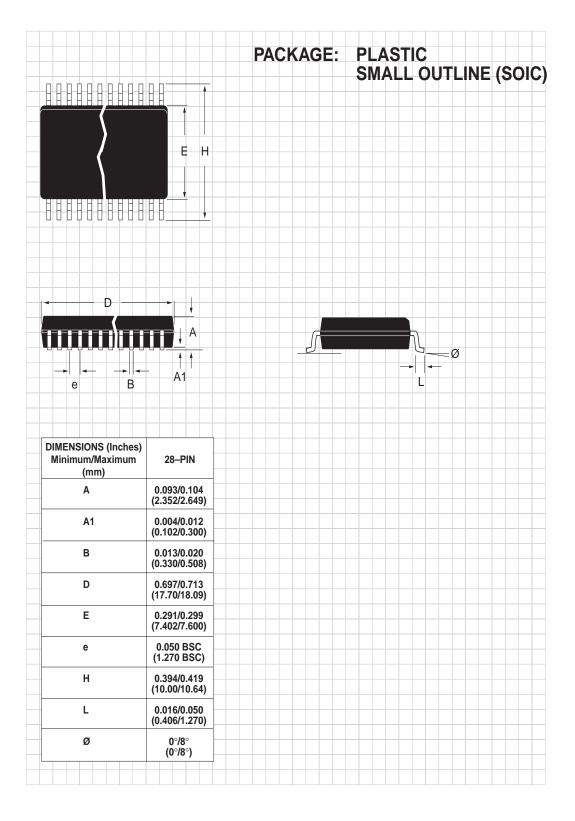
The **SP333** has a control line to enable or disable the receiver outputs. Pin 3 (\overline{RXEN}) is active LOW; a logic LOW on Pin 3 will enable the receiver outputs. A logic HIGH on Pin 3 will disable the receiver outputs. The receiver enable function can be initiated in either RS-232 or AppleTalk mode.

Wake-Up

The **SP333** also features a "wake-up" function. The wake up function allows the RS-232 receivers to remain active during Shutdown mode unless they are disabled by the Receiver Enable control pin (Pin 3). The wake-up feature allows users to take advantage of the low power Shutdown mode and keep the receivers active to accept an incoming "ring indicator" signal.







TGoddard/SP333/9617R0

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP333CT	0°C to +70°C	
SP333ET		



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