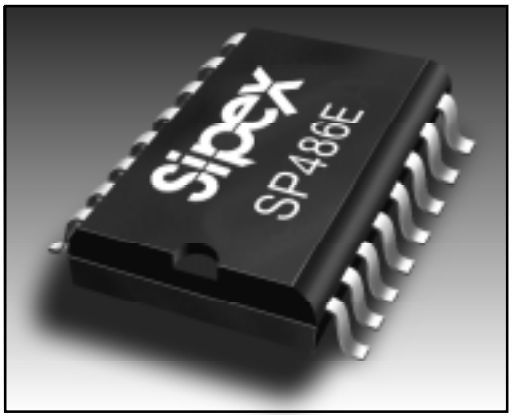
SP486E and SP487E

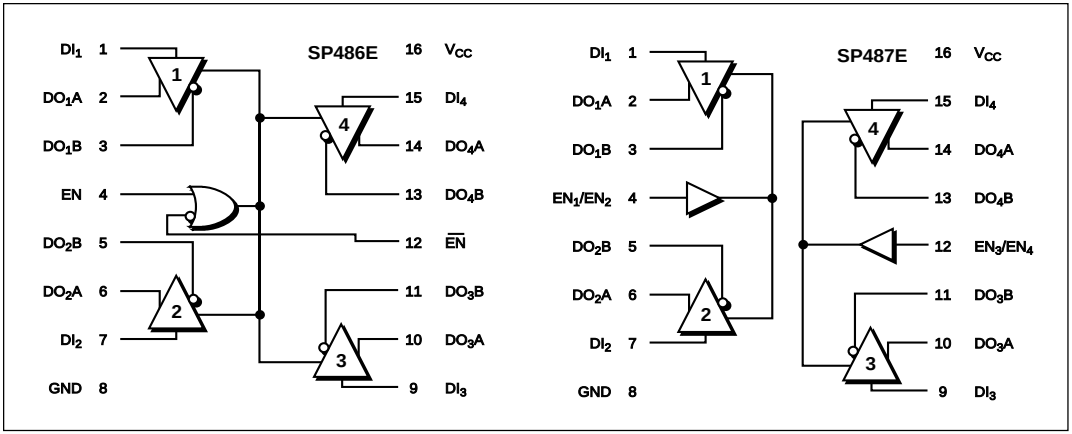
Enhanced Quad RS-485/RS-422 Line Drivers

- RS-485 or RS-422 Applications
- Quad Differential Line Drivers
- Driver Output Disable
- –7V to +12V Common Mode Output Range
- 100µA Supply Current
- Single +5V Supply Operation
- Superior Drop-in Replacement for SN75172, SN75174, LTC486, and LTC487
- Improved ESD Specifications:
  ±15kV Human Body Model
  ±15kV IEC1000-4-2 Air Discharge
  ±8kV IEC1000-4-2 Contact Discharge



DESCRIPTION…

The **SP486E** and **SP487E** are low-power quad differential line drivers that meet the specifications of RS-485 and RS-422 serial protocols with enhanced ESD performance. The ESD tolerance has been improved on these devices to over ±15kV for both Human Body Model and IEC1000-4-2 Air Discharge Method. These devices are superior drop-in replacements to **Sipex's SP486** and **SP487** devices as well as popular industry standards. As with the original versions, the **SP486E** features a common driver enable control and the **SP487E** provides independent driver enable controls for each pair of drivers. Both feature wide common-mode input ranges. Both are available in 16-pin plastic DIP and SOIC packages.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

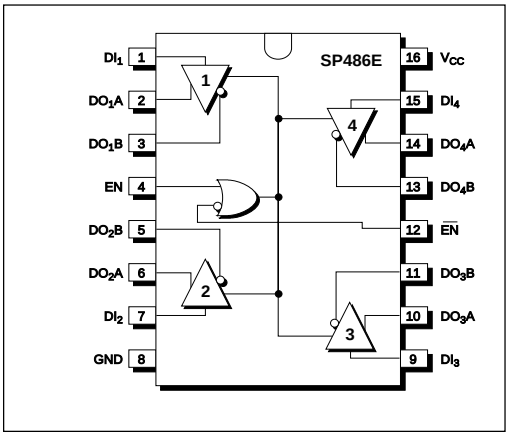
V_{CC} ..... +7V
Input Voltages
Logic ..... –0.5V to (V_{CC} +0.5V)
Drivers ..... –0.5V to (V_{CC} +0.5V)
Driver Output Voltage ..... ±14V
Input Currents
Logic ..... ±25mA
Driver ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Power Dissipation
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)
Lead Temperature (soldering, 10 sec) ..... 300°C

SPECIFICATIONS

V_{CC} = 5V±5%; typicals at 25°C; $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS					
Digital Inputs					DI, EN, $\overline{EN}$, EN_1/EN_2, EN_3/EN_4
Voltage					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Input Current			±2	µA	V_{IN} = 0V to V_{CC}
DRIVER OUTPUTS					
Differential Voltage			V_{CC}	Volts	I_O = 0; unloaded
	2			Volts	R_L = 50Ω(RS-422)
	1.5	2	V_{CC}	Volts	R_L = 27Ω (RS-485); *Fig. 1*
Change in Output Magnitude for Complementary Output State			0.2	Volts	R_L = 27Ω or 50Ω ; *Fig. 1*
Common Mode Output Voltage		2.3	3	Volts	R_L = 27Ω or 50Ω; *Fig. 1*
Change in Common Mode Output Magnitude for Complementary Output State			0.2	Volts	R_L = 27Ω or 50Ω; *Fig. 1* R_L = 50Ω (RS-422) R_L = 27Ω (RS-485)
Maximum Data Rate	10			Mbps	
Short–circuit Current					
V_{OH}			±250	mA	–7V ≤V_O ≤ +12V
V_{OL}			±250	mA	–7V ≤V_O ≤ +12V
High Impedance Output Current		±2	±200	µA	V_O = –7V to +12V
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		0.5	10	mA	No load, output enabled
		0.5	10	µA	No load, output disabled
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–C	0		+70	°C	
–E	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package					
–_P	16–pin Plastic DIP				
–_T	16–pin SOIC				

PINOUT — SP486E



SP486E PINOUT

Pin 1 — DI_1 — Driver 1 Input — If Driver 1 output is enabled, logic 0 on DI_1 forces driver output DO_1A low and DO_1B high. A logic 1 on DI_1 with Driver 1 output enabled forces driver DO_1A high and DO_1B low.

Pin 2 — DO_1A — Driver 1 output A.

Pin 3 — DO_1B — Driver 1 output B.

Pin 4 — EN — Driver Output Enable. Please refer to **SP486E** *Truth Table (1).*

Pin 5 — DO2B — Driver 2 output B.

Pin 6 — DO_2A — Driver 2 output A.

Pin 7 — DI_2 — Driver 2 Input — If Driver 2 output is enabled, logic 0 on DI_2 forces driver output DO_2A low and DO_2B high. A logic 1 on DI_2 with Driver 2 output enabled forces driver DO_2A high and DO_2B low.

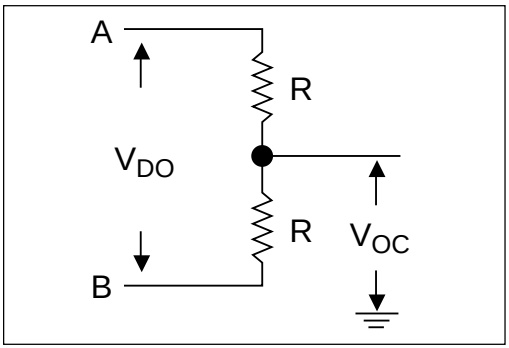


Figure 1. Driver DC Test Load

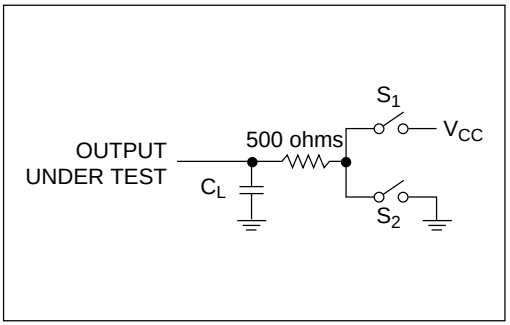


Figure 3. Driver Timing Test Load

Pin 8 — GND — Digital Ground.

Pin 9 — DI_3 — Driver 3 Input — If Driver 3 output is enabled, logic 0 on DI_3 forces driver output DO_3A low and DO_3B high. A logic 1 on DI_3 with Driver 3 output enabled forces driver DO_3A high and DO_3B low.

Pin 10 — DO_3A — Driver 3 output A.

Pin 11 — DO_3B — Driver 3 output B.

Pin 12 — $\overline{EN}$ — Driver Output Disable. Please refer to **SP486E** *Truth Table (1).*

Pin 13 — DO_4B — Driver 4 output B.

Pin 14 — DO_4A — Driver 4 output A.

Pin 15 — DI_4 — Driver 4 Input — If Driver 4 output is enabled, logic 0 on DI_4 forces driver output DO_4A low and DO_4B high. A logic 1 on DI_4 with Driver 3 output enabled forces driver DO_4A high and DO_4B low.

Pin 16 — Supply Voltage V_{CC} — $4.75V \le V_{CC} \le 5.25V$.

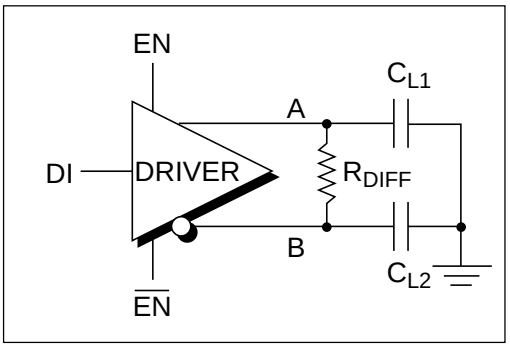
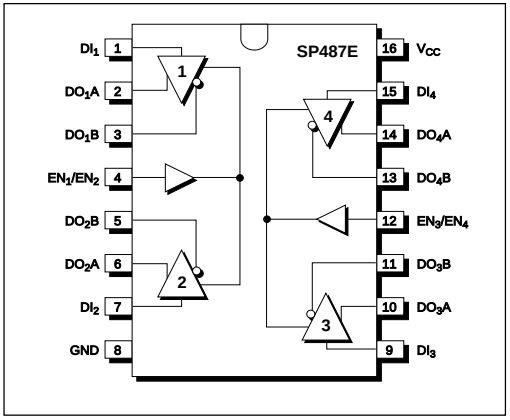


Figure 2. Driver Timing Test

PINOUT — SP487E



SP487E PINOUT

Pin 1 — DI_1 — Driver 1 Input — If Driver 1 output is enabled, logic 0 on DI_1 forces driver output DO_1A low and DO_1B high. A logic 1 on DI_1 with Driver 1 output enabled forces driver DO_1A high and DO_1B low.

Pin 2 — DO_1A — Driver 1 output A.

Pin 3 — DO_1B — Driver 1 output B.

Pin 4 — EN_1/EN_2 — Driver 1 and 2 Output Enable. Please refer to **SP487E** *Truth Table (2).*

Pin 5 — DO_2B — Driver 2 output B.

Pin 6 — DO_2A — Driver 2 output A.

Pin 7 — DI_2 — Driver 2 Input — If Driver 2 output is enabled, logic 0 on DI_2 forces driver output DO_2A low and DO_2B high. A logic 1 on DI_2 with Driver 2 output enabled forces driver DO_2A high and DO_2B low.

Pin 8 — GND — Digital Ground.

Pin 9 — DI_3 — Driver 3 Input — If Driver 3 output is enabled, logic 0 on DI_3 forces driver output DO_3A low and DO_3B high. A logic 1 on DI_3 with Driver 3 output enabled forces driver DO_3A high and DO_3B low.

Pin 10 — DO_3A — Driver 3 output A.

INPUT	ENABLES		OUTPUTS	
DI	EN	$\overline{EN}$	OUTA	OUTB
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Hi–Z	Hi–Z

Table 1. SP486E Truth Table

Pin 11 — DO_3B — Driver 3 output B.

Pin 12 — EN_3/EN_4 — Driver 3 and 4 Output Enable. Please refer to **SP487E** *Truth Table (2).*

Pin 13 — DO_4B — Driver 4 output B.

Pin 14 — DO_4A — Driver 4 output A.

Pin 15 — DI_4 — Driver 4 Input — If Driver 4 output is enabled, logic 0 on DI_4 forces driver output DO_4A low and DO_4B high. A logic 1 on DI_4 with Driver 3 output enabled forces driver DO_4A high and DO_4B low.

Pin 16 — Supply Voltage V_{CC} — $4.75V \leq V_{CC} \leq 5.25V$.

FEATURES...

The **SP486E** and **SP487E** are low–power quad differential line drivers meeting RS-485 and RS-422 standards. The **SP486E** features active high and active low common driver enable controls; the **SP487E** provides independent, active high driver enable controls for each pair of drivers. The driver outputs are short–circuit limited to 200mA. Data rates up to 10Mbps are supported. Both are available in 16–pin plastic DIP and SOIC packages.

INPUT	ENABLES	OUTPUTS	
DI	EN1/EN2 or EN3/EN4	OUTA	OUTB
H	H	H	L
L	H	L	H
X	L	Hi–Z	Hi–Z

Table 2. SP487E Truth Table

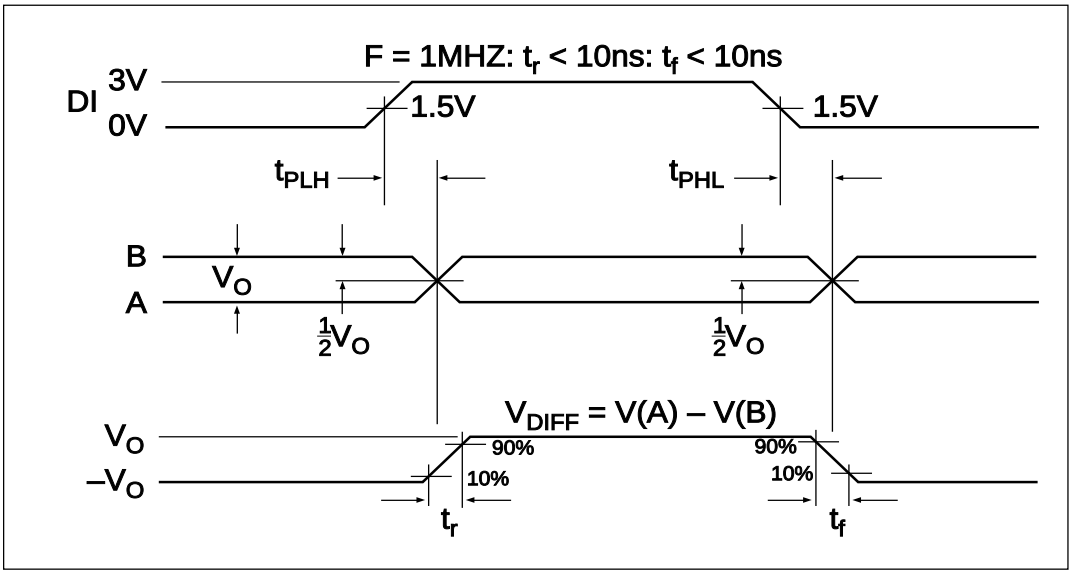


Figure 4. Driver Propagation Delays

AC PARAMETERS

V_{CC} = 5V±5%; typicals at 25°C; T_{AMB} = 25°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PROPAGATION DELAY					
Driver Input to Output					R_{DIFF} = 54 Ohms, C_{L1}= C_{L2}= 100pF; *Figure 2*
Low to High (t_{PLH})	20	40	60	ns	
High to Low (t_{PHL})	20	40	60	ns	
Differential Skew (t_{SKEW})		5	15	ns	$t_{SKEW} = \lvert t_{PLH} - t_{PHL} \rvert$
Driver Rise Time (t_R)					10% to 90%
SP486E		20		ns	
SP487E		20		ns	
Driver Fall Time (t_F)					90% to 10%
SP486E		20		ns	
SP487E		20		ns	
DRIVER ENABLE					
To Output High		60	110	ns	C_L = 100pF; *Figures 3 and 5* (S_2 closed)
To Output Low		60	115	ns	C_L = 100pF; *Figures 3 and 5* (S_1 closed)
DRIVER DISABLE					
From Output Low		60	130	ns	C_L = 15pF; *Figures 3 and 5* (S_1 closed)
From Output High		60	130	ns	C_L = 15pF; *Figures 3 and 5* (S_2 closed)

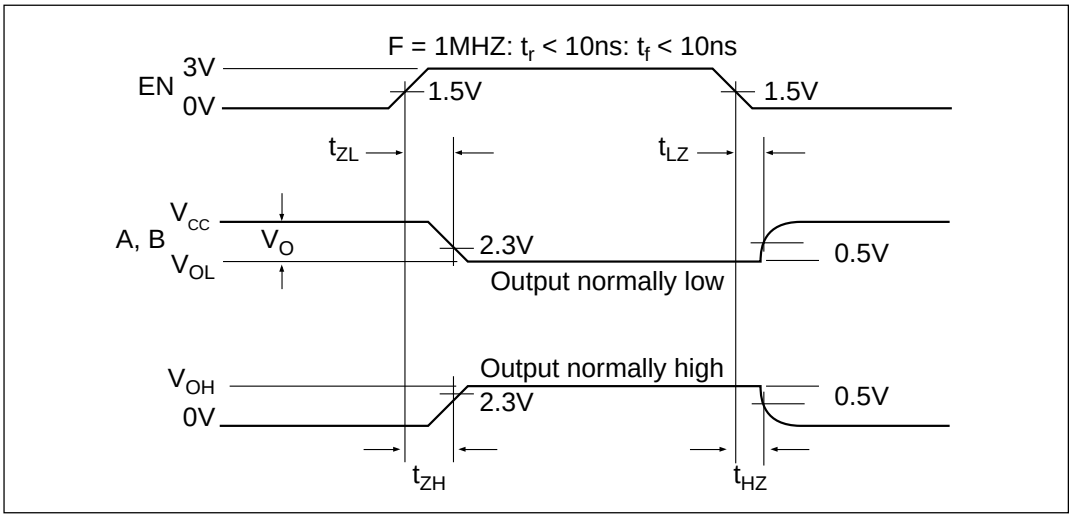


Figure 5. Driver Enable/Disable Timing

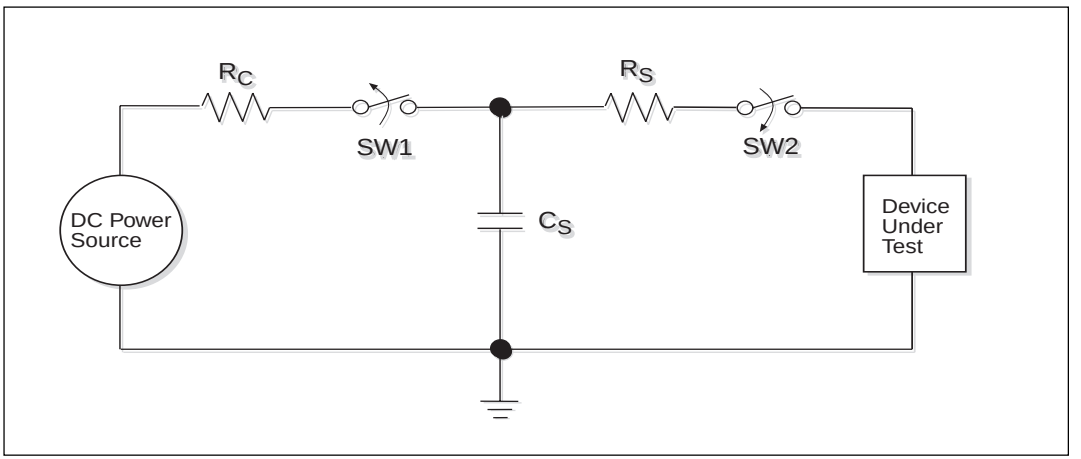


Figure 6. ESD Test Circuit for Human Body Model

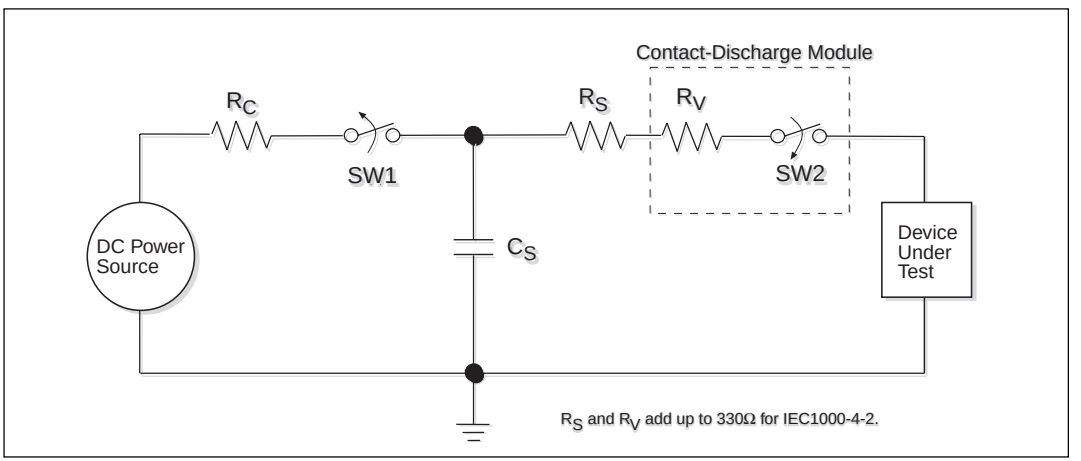


Figure 7. ESD Test Circuit for IEC1000-4-2

ESD TOLERANCE

The **SP486E** and **SP487E** devices incorporate ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 6*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 7*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

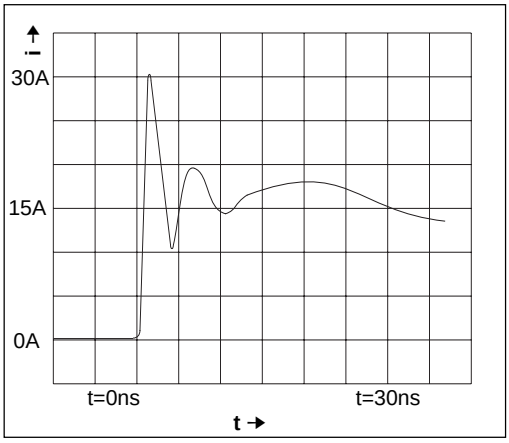


Figure 8. ESD Test Waveform for IEC1000-4-2

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in *Figures 6 and 7* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

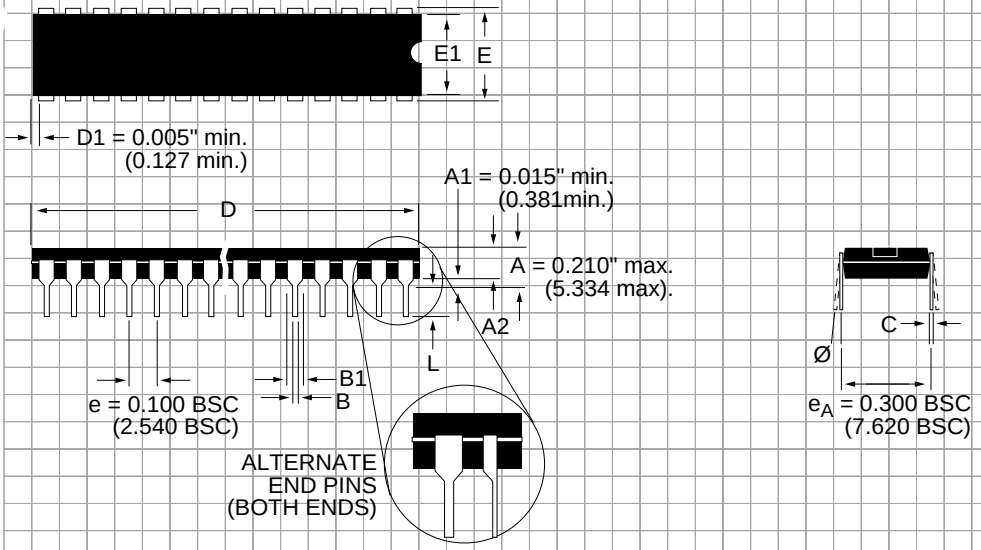
For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kW an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330W an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

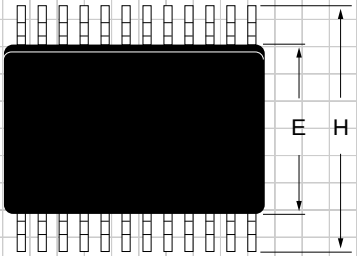
Table 3. Transceiver ESD Tolerance Levels

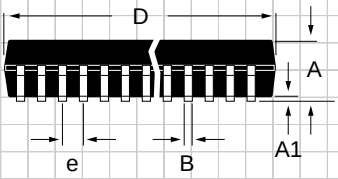
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

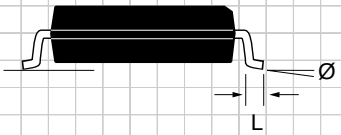


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.780/0.800 (19.812/20.320)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)







DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.398/0.413 (10.10/10.49)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

Quad RS485 Drivers:

Model	Enable/Disable	Temperature Range	Package
SP486ECP	Common; active Low and Active High	0°C to +70°C	16–pin Plastic DIP
SP486ECT	Common; active Low and Active High	0°C to +70°C	16–pin SOIC
SP486EEP	Common; active Low and Active High	–40°C to +85°C	16–pin Plastic DIP
SP486EET	Common; active Low and Active High	–40°C to +85°C	16–pin SOIC
SP487ECP	One per driver pair; active High	0°C to +70°C	16–pin Plastic DIP
SP487ECT	One per driver pair; active High	0°C to +70°C	16–pin SOIC
SP487EEP	One per driver pair; active High	–40°C to +85°C	16–pin Plastic DIP
SP487EET	One per driver pair; active High	–40°C to +85°C	16–pin SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

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