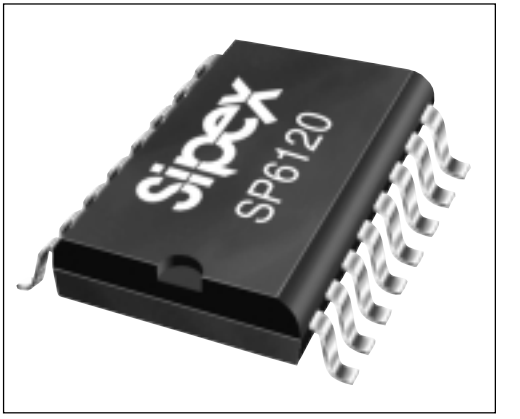
Low Voltage, AnyFET™, Synchronous ,Buck Controller

Ideal for 2A to 10A, High Performance, DC-DC Power Converters

- Optimized for Single Supply, 3V - 7V Applications
- High Efficiency: Greater Than 95% Possible
- "AnyFET™" Technology: Capable Of Switching Either PFET Or NFET High Side Switch
- Selectable Discontinuous or Continuous Conduction Mode For Use In Battery Or Bus Applications
- Fast Transient Response
- 16-Pin TSSOP, Small Size
- Accurate 1% Reference Over Line, Load and Temperature
- Accurate 10% Frequency
- Accurate, Rail to Rail, 40mV, 20% Over-Current Sensing
- Resistor Programmable Frequency
- Resistor Programmable Output Voltage
- Capacitor Programmable Soft Start
- Low Quiescent Current: 950µA, 10µA in Shutdown
- Hiccup Over-Current Protection
- Output Over-Voltage Protection

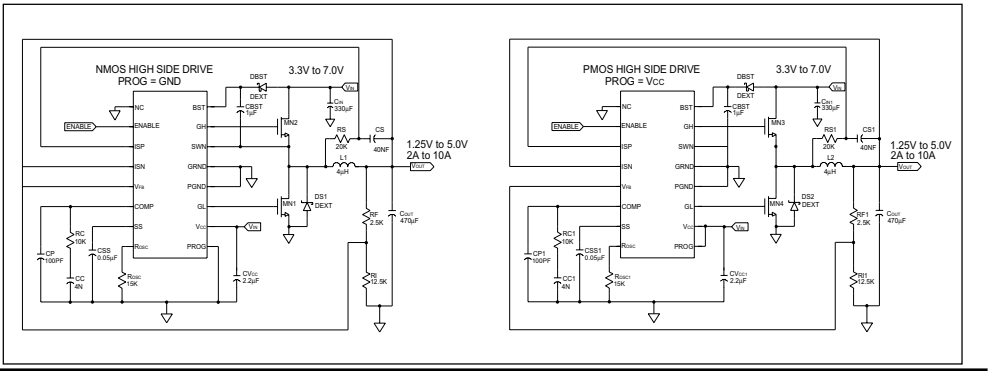


APPLICATIONS

- DSP
- Microprocessor Core
- I/O & Logic
- Industrial Control
- Distributed Power
- Low Voltage Power

DESCRIPTION

The SP6120 is a fixed frequency, voltage mode, synchronous PWM controller designed to workfrom a single 5V or 3.3V input supply. Sipex's unique "AnyFET™" Technology allows the SP6120 to be used for resolving a multitude of price/performance trade-offs. It is separated from the PWM controller market by being the first controller to offer precision, speed, flexibility, protection and efficiency over a wide range of operating conditions.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....7V
BST.....13.2V
BST-SWN.....7V
SWN.....-1V to 7V
GH.....-0.3V to BST +0.3V
GH-SWN.....7V
All Other Pins .....-0.3V to V_{CC} +0.3V

Peak Output Current < 10us
GH, GL.....2A

Storage Temperature Range.....-65˚C to +150˚C
Power Dissipation.....
Lead Temperature (solding 10 sec).....+300˚C
ESD Rating.....2kV HBM

SPECIFICATIONS

Unless otherwise specified: 0°C < T_{AMB} <70°C, 3.0V < V_{CC} <5.5V, 3.0V < BST < 13.2, R_{OSC} = 18.7kΩ, CCOMP = 0.1µF, CSS = 0.1µF, ENABLE = 3V, CGH = CGL = 1nF, VFB = 1.25V, ISP = ISN = 1.25V, SWN = GRND = PGRND = 0V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
QUIESCENT CURRENT					
V_{CC} Supply Current	No Switching	-	0.95	1.6	mA
V_{CC} Supply Current (Disabled)	ENABLE = 0V	-	5	20	µA
BST Supply Current	No Switching	-	1	20	µA
ERROR AMPLIFIER					
Error Amplifier Transconductance		420	600	780	µS
COMP Sink Current	V_{FB} = 1.3V, COMP = 0.5V, No Faults	20	30	54	µA
COMP Source Current	V_{FB} = 1.2V, COMP = 1.6V	20	30	54	µA
COMP Output Impedence		2	3	4	MOhm
V_{FB} Input Bias Current		-	60	100	nA
REFERENCE					
Error Amplifier Reference	Trimmed with Error Amp in Unity Gain	1.238	1.250	1.262	V
V_{FB} 3% Low Comparator		|-2|	|-3|	|-4|	%VREF
V_{FB} 3% High Comparator		2	3	4	%VREF
OSCILLATOR & DELAY PATH					
Oscillator Frequency		270	300	330	kHz
Oscillator Frequency #2	R_{OSC} = 11.5k	450	500	550	kHz
Duty Ratio	Loop In Control -100% DC possible	90	95	-	%
R_{OSC} Voltage	Information Only - Moves with Oscillator Trim		0.65		V
Minimum GH Pulse Width	V_{CC} > 4.5V, Ramp up COMP Voltage > 0.6V until GH starts Switching	-	-	150	ns

SPECIFICATIONS

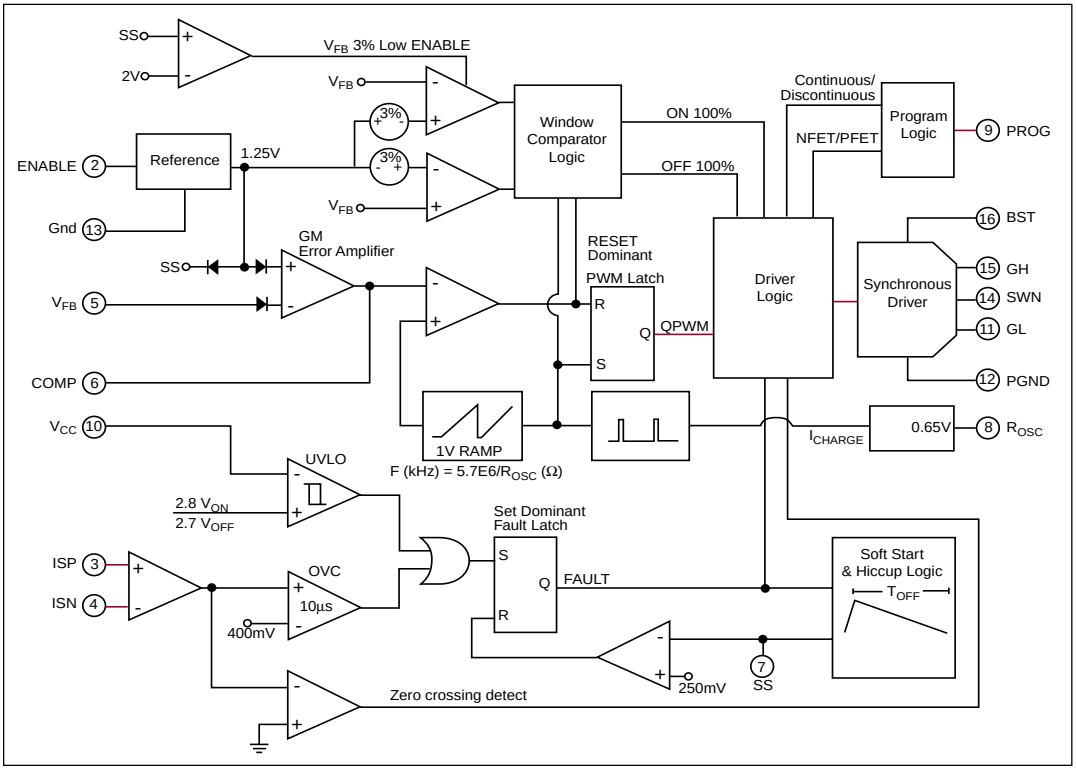
Unless otherwise specified: 0°C < T_{AMB} <70°C, 3.0V < V_{CC} <5.5V, 3.0V < BST < 13.2, R_{OSC} = 18.7kΩ, CCOMP = 0.1µF, CSS = 0.1µF, ENABLE = 3V, CGH = CGL = 1nF, VFB = 1.25V, ISP = ISN = 1.25V, SWN = GRND = PGRND = 0V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFTSTART					
SS Charge Current	VSS = 1.5V	28	40	52	µA
SS Discharge Current	VSS = 1.5V	3	4	5	µA
COMP Discharge Current	VCOMP = 0.5V, Fault Initiated	200	500	-	µA
COMP Clamp Voltage	V_{FB} < 1.0V, VSS = 2.5V	2	2.2	2.6	V
SS Ok Threshold		1.9	2.0	2.1	V
SS Fault Reset		0.2	0.25	0.3	V
SS Clamp Voltage		2	2.2	2.6	V
OVER CURRENT & ZERO CURRENT COMPARATORS					
Over Current Comparator Threshold Voltage	Rail to Rail Common Mode Input	32	40	48	mV
ISN, ISP Input Bias Current		-	60	100	nA
Zero Current Comparator Threshold	VISP - VISN	1.5	2	2.5	mV
ENABLE/UVLO					
V_{CC} Start Threshold		2.8	2.9	3.0	V
V_{CC} Stop Threshold		2.7	2.8	2.9	V
V_{CC} Hysteresis		75	100	125	mV
Enable Threshold		0.65	1.0	1.2	V
Enable Pin Source Current		0.6	4	8	µA
GATE DRIVER					
GH Rise Time		-	20	75	ns
GH Fall Time		-	20	75	ns
GL Rise Time		-	20	75	ns
GL Fall Time		-	20	75	ns
GH to GL Non-Overlap Time	V_{CC} > 4.5V	-	50	90	ns
GL to GH Non-Overlap Time	V_{CC} > 4.5V	-	50	90	ns

PIN DESCRIPTION

NAME	FUNCTION	PIN NUMBER
		SP6120
N/C	No Connection	1
ENABLE	TTL compatible input with internal 4uA pullup. Floating or Venable> 1.5V will enable the part, Venable < 0.65V disables part.	2
ISP	Current Sense Positive Input: Rail to Rail Input for Over-Current Detection, 40 mV with 10us (typ) response time.	3
ISN	Current Sense Negative Input: Rail to Rail input for Over-Current Detection	4
V_{FB}	Feedback Voltage Input: The voltage on this pin is typically a resistor divider	5
COMP	Error Amplifier Compensation Pin: Typically a pole-zero network is attached to this pin for compensating the double pole assoicated with the power supply L & C. This pin is clamped by the SS voltage and is limited to 2.6V maximum.	6
SS	Soft Start Programming Pin: This pin sources 40uA on start-up. A 0.01uF to 1uF capacitor on this pin is typically enough capacitance to soft start a power supply. In addition, hiccup mode timing is controlled by this pin through the 4uA discharge current. The SS voltage is clamped to 2.6V maximum.	7
R_{OSC}	Frequency Programming Pin: A resistor to ground is used to program frequency. Typical values - 18500 ohms, 300 kHz; 11500 ohms, 500kHz.	8
PROG	Programming Pin: PROG = GND; MODE = NFET/CONTINOUS PROG = 68kΩ to GND; MODE = NFET/DISCONTINOUS PROG = VCC; MODE = PFET/CONTINOUS PROG = 68kΩ to VCC; MODE = PFET/DISCONTINOUS	9
V_{CC}	I.C. Supply Pin: ESD structures also hooked to this pin.	10
GL	Synchronous FET Driver: 1nF/20ns typical drive capability.	11
PGND	Power Ground Pin: Used for Power Stage. Connect Directly to GND at I.C. pins for optimal performance.	12
GRND	Ground Pin: Main ground pin for I.C.	13
SWN	Switch Node Reference: High	14
GH	HIgh Side FET Driver: Can be NFET or PFET depending on Program Mode. 1nF/20ns typical drive capability. Maximum voltage rating is referenced to SWN.	15
BST	High Side Driver Supply.	16

BLOCK DIAGRAM



APPLICATIONS

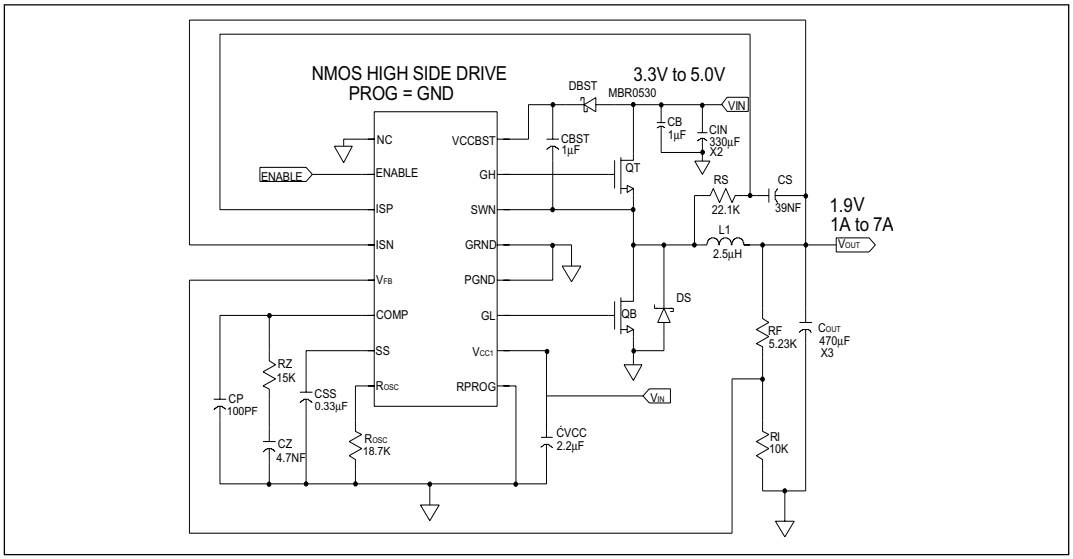


Figure 1. Schematic 3.3V to 1.9V Power Supply

QT, QB = FAIRCHILD FDS6690A
L1 = PANASONIC ETQP6F2R5SFA
DS = STMICROELECTRONICS STPS2L25U
CIN = AVX TPSE337K010R0060
COUT = AVX TPSE477K006R0050

Performance Characteristics

Refer to circuit in Figure 1 with V_{IN} = 3.3V; V_{OUT} = 1.9V, Oscillator Frequency = 300kHz, and T_{AMB} = +25°C unless otherwise noted.

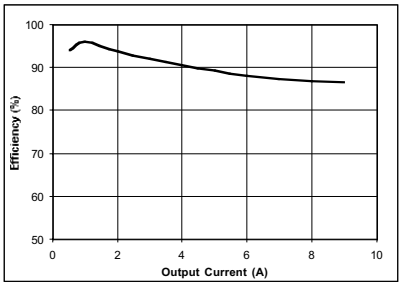


Figure 2. Efficiency vs. Output Current

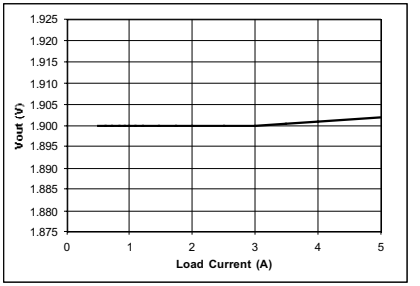


Figure 3. Load Regulation

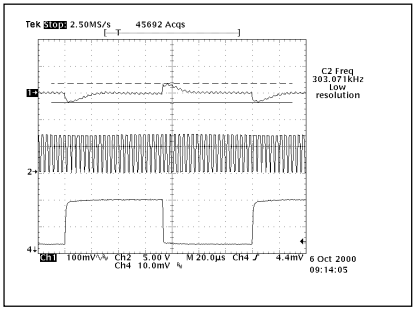


Figure 4. Load Step Response: 0.4A to 2A
Ch 1 = Vout, Ch 2 = Gate High, Ch 4 = Iout 1A/Div

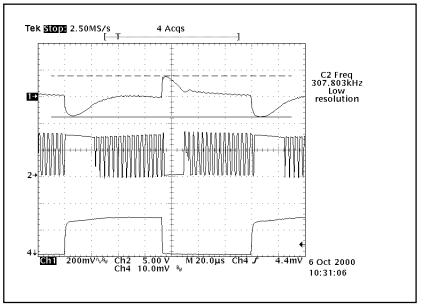


Figure 5. Load Step Response: 0.4A to 7A
Ch 1 = Vout, Ch 2 = Gate High, Ch 4 = Iout 5A/Div

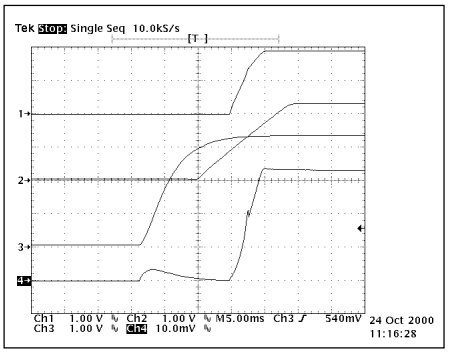


Figure 6. Start-Up Response: 5ADC Load
Ch 1 = Vout, Ch 2 = Soft Start Pin, Ch 3 = Vin, Ch 4 = Input Current 1A/Div

FEATURES

General Overview:

The SP6120 is a constant frequency, voltage mode PWM controller for low voltage, DC/DC step down converters. It has a main loop where an external resistor (R_{OSC}) sets the frequency and the driver is controlled by the comparison of an error amp output (COMP) and a 1V ramp signal. The error amp has a transconductance of 600 µS, an output impedance of 3 Mohm, an internal pole at 2 MHz and a 1.25V reference input. Although the main in control loop cable of 0% and 100 % duty cycle, its response time is limited by the external component selection. Therefore, a secondary loop, including a window comparator positioned 3 % above and below the reference, has been added to insure fast response to line and load transients. A unique "Ripple & Frequency Independent" algorithm, added to the secondary loop, insures that the window comparator does not interfere with the main loop during normal operation. In addition to receiving driver commands from the main and secondary loops, the DRIVER LOGIC is also controlled by the PROGRAMMING LOGIC, FAULT LOGIC and ZERO CROSSING COMPARATOR. The PROGRAMMING LOGIC tells the DRIVER LOGIC whether the controller is using a PFET or NFET high side driver as well as whether the controller is operating in continuous or discontinuous mode. The FAULT LOGIC holds the high and low side drivers off if V_{CC} dips below 2.7V, if an over current condition exists, or if the part is disabled through the ENABLE pin. The ZERO CROSSING COMPARATOR turns the lower driver off if the conduction current reaches zero and the DRIVER LOGIC has made an attempt to turn the lower driver on and the PROGRAMMING LOGIC is set for discontinuous mode. Lastly, the 4 ohm drivers have internal gate non-overlap circuitry and are designed to drive MOSFETS associated with converter designs in the 5 A – 10 A range. Typically the high side driver is referenced to the SWN pin; further improving the efficiency and performance of the converter.

Enable:

Low quiescent mode or "Sleep Mode" is initiated by pulling the ENABLE pin below 600 mV. The ENABLE pin has an internal 4 µA pull-up current and does not require any external interface for normal operation. If the ENABLE pin is driven from a voltage source, the voltage must be above 1.3 V in order to guarantee proper "awake" operation. Assuming that V_{CC} is above 2.9 V, the SP6120 transitions from "Sleep Mode" to "Awake Mode" in about 20 µs – 30 µs and from "Awake Mode" to "Sleep Mode" in a few microseconds. SP6120 quiescent current in sleep mode is 20 uA maximum. uring Sleep Mode, the high side and low side MOSFETS are turned off and the COMP and SS pins are held low.

UVLO:

Assuming that the ENABLE pin is either pulled high or floating, the voltage on the V_{CC} pin then determines operation of the SP6120. As V_{CC} rises, the UVLO block monitors V_{CC} and keeps the high side and low side MOSFETS off and the COMP and SS pins low until V_{CC} reaches 2.9 V. If no faults are present, the SP6120 will initiate a soft start when V_{CC} exceeds 2.9 V. Hysteresis (about 100mV) in the UVLO comparator provides noise immunity at start-up.

Soft Start*:*

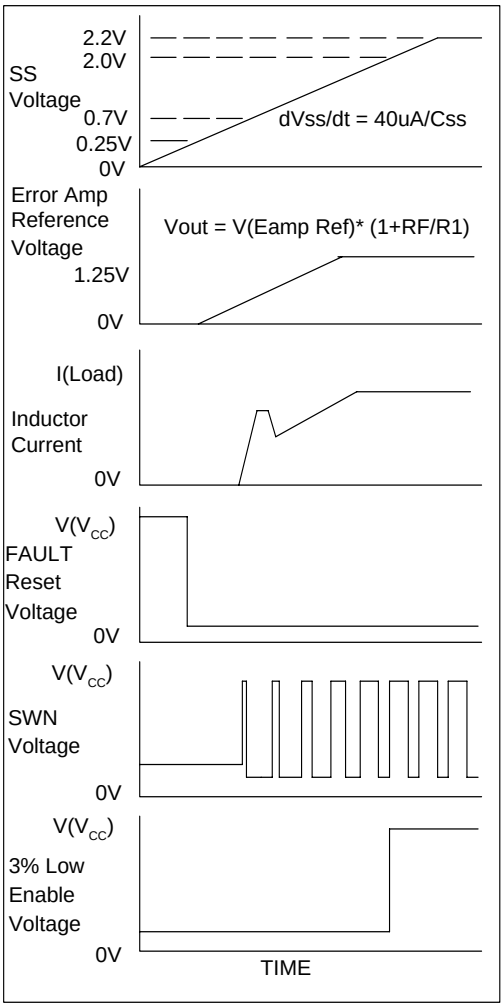
(see figures on next page)

Soft start is required on step-down controllers to prevent excess inrush current through the power train during start-up. Typically this is managed by sourcing a controlled current into a programming capacitor (on the SS pin) and then using the voltage across this capacitor to slowly ramp up either the error amp reference or the error amp output (COMP). The control loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady-state duty cycle as the output voltage increases to its regulated value. As a result of controlling the inductor volt*second product during startup, inrush current is also controlled.

Soft Start: (cont'd)

The presence of the output capacitor creates extra current draw during startup. Simply stated, dVOUT/dt requires an average sustained current in the output capacitor and this current must be considered while calculating peak inrush current and over current thresholds. Since the SP6120 ramps up the error amp reference voltage, an expression for the output capacitor current can be written as:

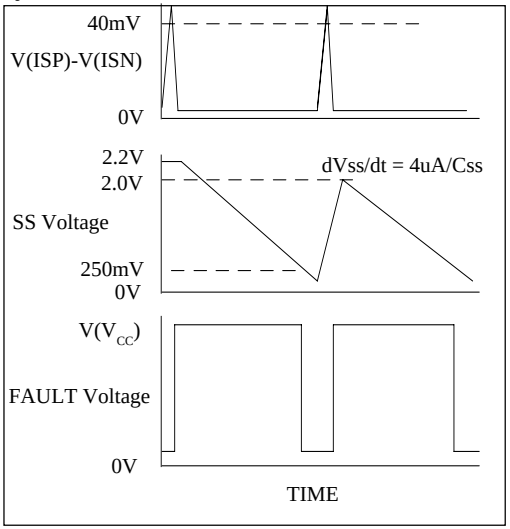
ICout = (Cout/Css) * (Vout/1.25) * 40uA



As the figure shows, the SS voltage controls a variety of signals. First, provided all the external fault conditions are removed, the fault latch is reset and the SS cap begins to charge. When the SS voltage reaches around 0.3V, the error amp reference begins to track the SS voltage while maintaining the 0.3V differential. As the SS voltage reaches 0.7V, the driver begins to switch the high side and low side FETs with narrow pulses in an effort to keep the converter output regulated. As the error amp reference ramps upward, the driver pulses widen until a steady state value is reached. The "bump" in the inductor current transfer curve is indicative of excess charge current incurred due to the finite propagation delay of the controller. When the SS voltage reaches 2.0V, the secondary loop including the 3% window comparator is enabled. Lastly, the SS voltage is clamped at 2.2V, ending the soft start charge cycle.

Hiccup Mode:

When the converter enters a fault mode, the driver holds the high side and low side FETs off for a finite period of time. Provided the part is enabled, this time is set by the discharge of the SS capacitor. The discharge time is roughly 10 times the charge interval thereby giving the power supply plenty of time to cool during an over current fault. The driver off-time is predominantly determined by the discharge time. Restart will occur just like a normal soft start cycle.



Hiccup Mode (cont'd):

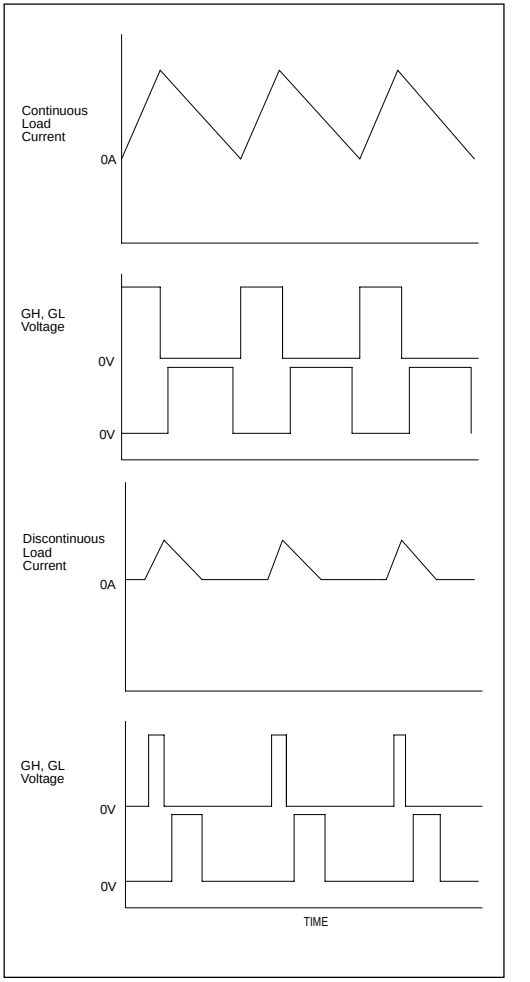
However, if a fault occurs during the soft start charge cycle, the FAULT latch is immediately set, turning off the high side and low side FETs. The FETs remain off during the remainder of the charge cycle and subsequent discharge cycle of the SS capacitor. Again, provided there are no external fault conditions, the FAULT latch will be reset when the SS voltage reaches 250 mV.

Over Current Protection:

The SP6120 over current protection scheme is designed to take advantage of three popular detection schemes: Sense Resistor, Trace Resistor or Inductor Sense. Because the detection threshold is only 40mV, both trace resistor and inductor sense become attractive protection schemes. The inductor sense scheme adds no additional dc loss to the converter and is an excellent alternative to Rdson based schemes; providing continuous current sensing and flexible FET selection. An internal, 10us filter conditions the over current signal from transients generated during load steps. In addition, because the over current inputs, ISP and ISN, are capable of rail to rail operation, the SP6120 provides excellent over current protection during conditions where V_{IN} approaches V_{OUT}.

Zero Crossing Detection:

In some applications, it may be undesirable to have negative conduction current in the inductor. This situation happens when the ripple current in the inductor is higher than the load current. Therefore, the SP6120 provides an option for "discontinuous" operation. If the PROGRAM LOGIC (see next section) is set for discontinuous mode, then the DRIVER LOGIC looks at the ZERO CROSSING COMPARATOR and the state of the lower gate driver. If the low side FET was "on" and V(ISP)-V(ISN) < 0 then the low side FET is immediately turned off and held off until the high side FET is turned "on". When the high side FET turns "on" , the DRIVER LOGIC is reset. The following figures show continuous and discontinuous operation for a converter with an NFET high side FET.



Program Logic:

The PROGRAM pin of the SP6120 adds a new level of flexibility to the design of DC/DC converters. A 10 uA current flows either into or out of the PROGRAM pin depending on the initial potential presented to the pin. If no resistor is present, the PROGRAM LOGIC simply looks at the potential on the pin, sets the mode to "continuous" and programs NFET or PFET high side drive accordingly. If the 68 kilohm resistor is present, the voltage drop across the resistor signals the SP6120 to put the DRIVER LOGIC in "discontinuous" mode. With one pin and a 68k resistor, the SP6120 can be configured for a variety of operating modes:

PROGRAM LOGIC TRUTH TABLE		
PROGRAM PIN	NFET OR PFET	MODE
Start to GND	NFET	Continuous
68 kΩ to GND	NFET	Discontinuous
Short to V_{CC}	PFET	Continuous
68 kΩ to V_{CC}	PFET	Discontinous

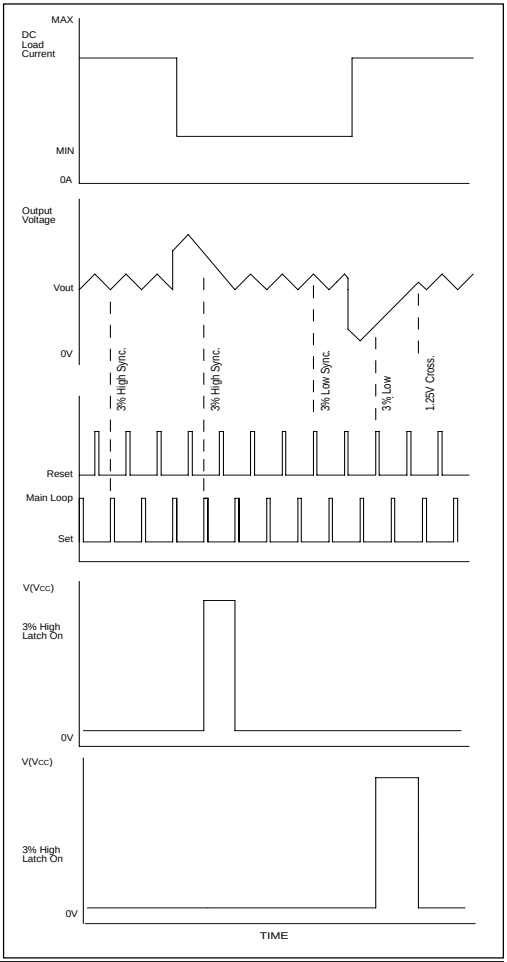
The NFET/PFET programmability is for the high side MOSFET. When designing DC/DC converters, it is not always obvious when to use an NFET with a charge pump or a simple PFET for the high side FET. Often, the controller has to be changed, making performance evaluations difficult. This difficulty is worsened by the limited availability of true low voltage controllers. In addition, by also programming the mode, continuous or discontinuous, switch mode power designs that are successful in bus applications can now find homes in portable applications.

Secondary Loop (3% Window Comparator):

DSP, microcontroller and microprocessor applications have very strict supply voltage requirements. In addition, the current requirements to these devices can change drastically. Linear regulators, typically the workhorse for DC/DC step-down, do a great job managing accuracy and transient response at the expense of efficiency. On the other hand, PWM switching regulators typically do a great job managing efficiency at the expense of output ripple and line/load step response. The trick in PWM controller design is to emulate the transient response of the linear regulator.

Of course improving transient response should be transparent to the power supply designer. Very often this is not the case. Usually the very circuitry that improves the controllers transient response adversely interferes with the main PWM loop or complicates the board level design of the power converter.

The SP6120 handles line/load transient response in a new way. First, a window comparator detects whether the output voltage is above or below the regulated value by 3%. Then, tproprietary "Ripple & Frequency Independent" algorithm synchronizes the output of the window comparator with the peak and valley of the inductor current waveform. 3% low detection is synchronized with inductor current peak; 3% high detection is synchronized with the inductor current valley. However, in order to eliminate any additional loops, the current peak and valley are determined by the edges associated with the on-time in the main loop. The set pulse corresponding to the start of an on-time indicates a current valley and the reset pulse corresponding to the end of an on-time indicates a current peak. In effect, the main loop determines the status of the secondary loop.



Secondary Loop (cont'd):

Notice that the output voltage appears to coast toward the regulated value during periods where the main loop would be telling the drivers to switch. It is during this interval that the 3% window comparator has taken control away from the main loop. The main loop regains control only if the output voltage crosses through its regulated value. Also notice WHERE the 3% comparator takes over. The output voltage is considered "high" only if the TROUGH of the ripple is above 3%. The output voltage is considered "low" only if the PEAK of the ripple is below 3%. By managing the secondary loop in this fashion, the SP6120 can improve the transient response of high performance power converters without causing strange disturbances in low to moderate performance systems.

Driver Logic:

Signals from the PWM latch (QPWM), Fault latch (FAULT), PROGRAM LOGIC, ZERO CROSSING COMPARATOR, and 3% WINDOW COMPARATORS all flow into the DRIVER LOGIC. The following is a truth table for determining the state of the GH and GL voltages for given inputs:

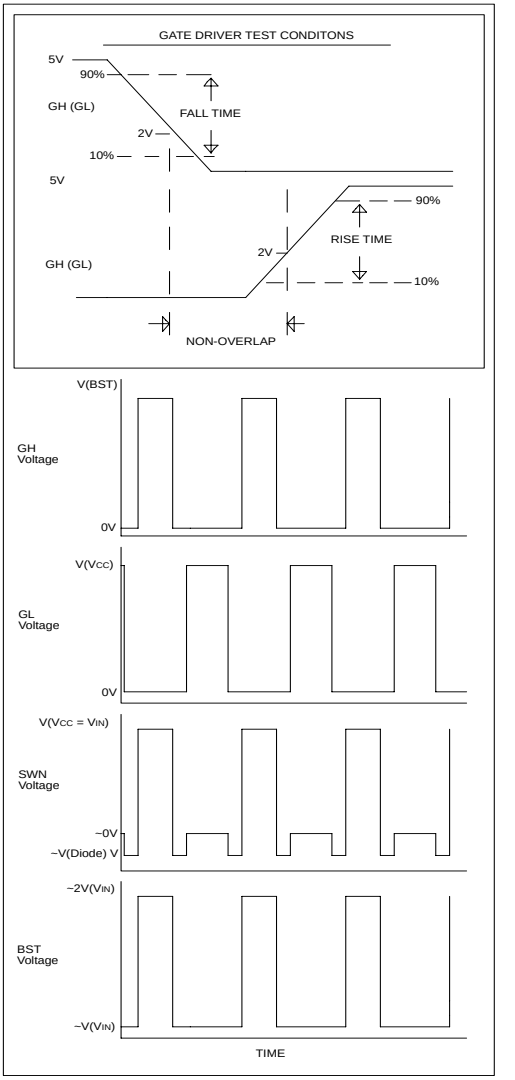
DRIVER LOGIC TRUTH TABLE

FAULT	1	1	0	0	0	0	0	0	0	0
QPWM or 3% COMP	X	X	1	1	0	0	0	0	0	0
NFET/PFET	N	P	N	P	N	P	N	P	N	P
CONT/DISC	X	X	X	X	C	C	D	D	D	D
ZERO CROSS	X	X	X	X	X	X	0	0	1	1
GH	0	1	1	0	0	1	0	1	0	1
GL	0	0	0	0	1	1	1	1	0	0

The QPWM and 3% Comparators are grouped together because 3% Low is the same as QPWM = 1 and 3% High is the same as QPWM = 0.

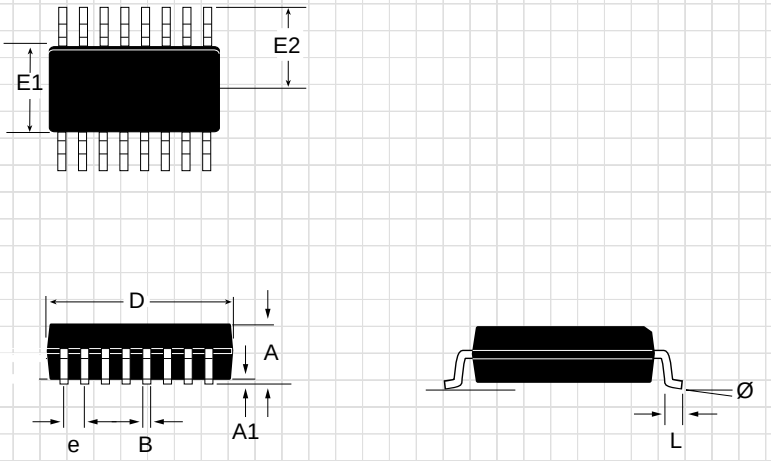
Output Drivers:

The driver stage consists of one high side, 4 ohm driver, GH and one low side, 4ohm, NFET driver, GL. As previously stated, the high side driver can be configured to drive a PFET or an NFET high side switch. The high side driver can also be configured as a switch node referenced driver. Due to voltage constraints, this mode is mandatory for 5V, single supply, high side NFET applications. The following figure shows typical driver waveforms for the 5V, high side NFET design.



As with all synchronous designs, care must be taken to ensure that the MOSFETs are properly chosen for non-overlap time, peak current capability and efficiency.

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)



DIMENSIONS in inches (mm) Minimum/Maximum	16–PIN
A	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)
D	0.193/0.201 (4.90/5.10)
E1	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)
E2	0.126 BSC (3.20 BSC)
L	0.020/0.030 (0.50/0.75)
Ø	0°/8°

ORDERING INFORMATION

Model	Operating Temperature Range	Package Type
SP6120CY	0˚C to +70˚C	16-Pin TSSOP

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

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