# Sipex

SP682

Ultra-Low Power Inverting Voltage Doubler

- Low Power Voltage Conversion
- +2.4V to +5.5V Input Range
- 99% Voltage Conversion Efficiency
- Typical 60µA Supply Current
- Requires Only Three External Capacitors
- Includes Low Power Shutdown Option
- Ideal in Portable Applications Such As
    - Handheld Instruments
    - Cellular Phones
    - Personal Digital Assistants
    - Laptops and Notebooks
- Pin Compatible Upgrade to the TC682
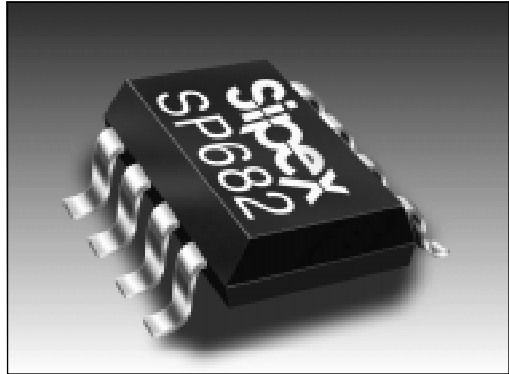
DESCRIPTION...

The **SP682** is a monolithic charge pump voltage converter that produces a doubled, negative voltage from a single positive supply. The **SP682** charge pump outputs a −10V voltage from a +5V input. Three external charge pump capacitors are required to support the voltage conversion and voltage doubling process. An internal oscillator generates a 12kHz clock which cycles the internal switching that charges the storage and transfer capacitors. The charge pump architecture is fabricated using a low power BiCMOS process technology.

The **SP682** charge pump is ideal for low power applications requiring a typical +3V battery source such as a lithium cell. Typical applications are handheld instruments, notebook and laptop computers, cellular phones, and data acquisition or GP systems. The **SP682** is packaged in either a 8-pin DIP, 8-pin SOIC or 8-pin µSOIC for surface mount applications.

TYPICAL OPERATING CIRCUIT...
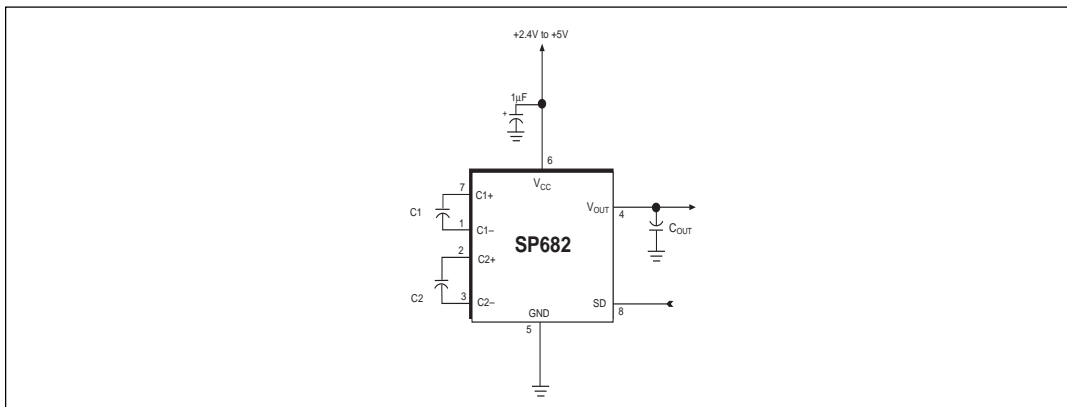
ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}..+7V
V_{OUT}..–11V
Storage Temperature..........................-65˚C to +150˚C
Power Dissipation:
       8-pin Plastic DIP.............................750mW
       8-pin Plastic SOIC..........................500mW
Package Derating:
8-pin Plastic DIP
       $\varnothing_{JA}$..97 °C/W
8-pin Plastic SOIC
       $\varnothing_{JA}$..115 °C/W

SP682 SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX} and V_{CC} = +5V unless otherwise noted.

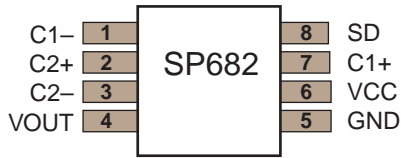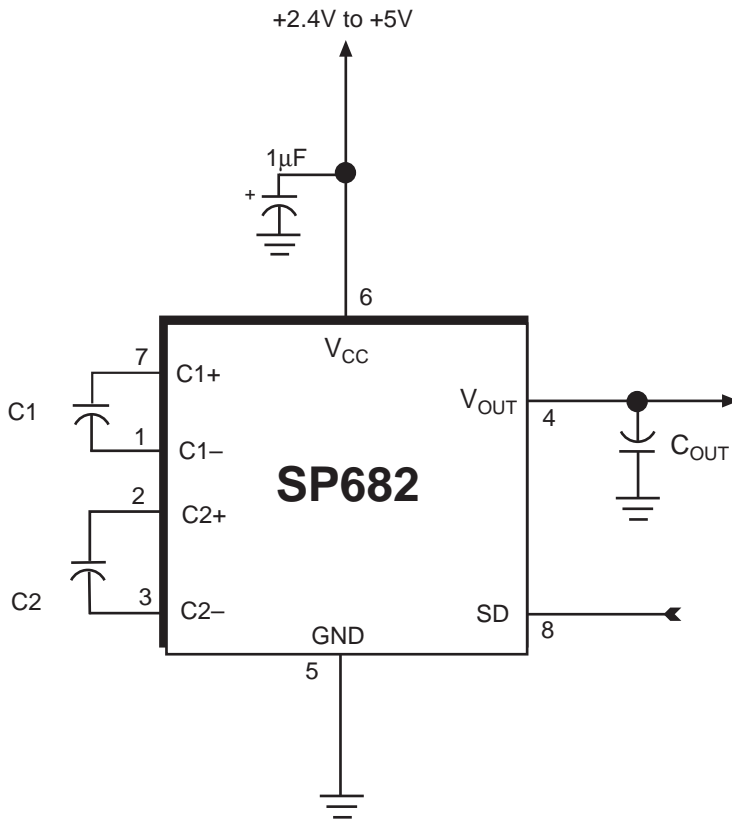|	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SUPPLY CURRENT					**CHARGE PUMP CAPACITORS: 3.3µF**
I_{CC}		60	120	µA	$R_L = \infty$, T_A = +25°C
			200	µA	$R_L = \infty$
			1	µA	T_A = +25°C,
					SD = +5V Separate Supply
CHARGE PUMP OUTPUT					**CHARGE PUMP CAPACITORS: 3.3µF**
V_{OUT}	–9.9	–9.99		Volts	$R_L = \infty$
	–9.0	–9.5		Volts	R_L = 2kΩ
OUTPUT SOURCE RESISTANCE					
R_{OUT}		140	180	Ω	I_L = 10mA, T_A = +25°C
			230	Ω	I_L = 10mA
		380	450	Ω	I_L = 5mA, V_{CC} = +2.8V
OSCILLATOR FREQUENCY					
f_{OSC}		12	20	kHz	$f_{osc} = 2 \times f_{C1+}$
VOLTAGE CONVERSION EFFICIENCY					
V_{OUT}	99	99.9		%	$R_L = \infty$
V_{OUT}	90	95		%	R_L = 2kΩ
START-UP TIMING					
t_{DVO}; V_{OUT} Power On Delay		12		ms	R_L = 2kΩ
SHUTDOWN TIMING					
t_{EN}; Shutdown to V_{OUT} Delay		5		ms	R_L = 2kΩ
POWER REQUIREMENTS					
V_{CC}	+2.4		+5.5	Volts	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range					
- C	0		+70	°C	
- E	-40		+85	°C	

Figure 1. SP682 Pinout

Figure 2. Typical Operating Circuit

THEORY OF OPERATION

The **SP682**'s charge pump design is a simplified version of **Sipex**'s original patented charge pump design (5,306,954) except that it only generates a negative output. The charge pump requires external capacitors to store the charge. Figure 1 shows the waveform found on the negative side of capacitor C2. There is a free–running oscillator, running at 12kHz, that controls the two phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{OUT} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{OUT} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{OUT} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

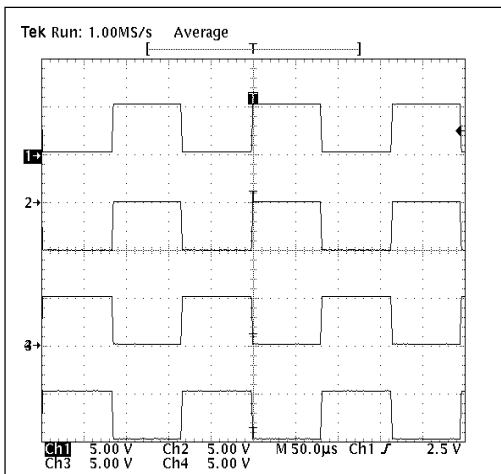The oscillator frequency or clock rate for the charge pump is designed for low power operation. The oscillator operates at a frequency of about 12kHz (20kHz maximum) which conserves power as opposed to higher frequencies which draws more power from V_{CC}. The external charge pump capacitors specified is 3.3µF but the absolute minimum should be 1µF.

EFFICIENCY INFORMATION

A charge pump theoretically produces a doubled voltage at 100% efficiency. However in the real world, there is a small voltage drop on the output which reduces the output efficiency. The **SP682** can usually run 99.9% efficient without driving a load. While driving a 1kΩ load, the **SP682** remains at least 90% efficient.

$$\text{Output Voltage Efficiency} = V_{OUT}/(-2*V_{CC});$$
$$V_{OUT} = -2*V_{CC} + V_{DROP}$$
$$V_{DROP} = (I_{OUT})*(R_{OUT})$$

$$\text{Power Loss} = I_{OUT}*(V_{DROP})$$

The efficiency changes as the external charge pump capacitors are varied. Larger capacitor values will strengthen the output and reduce output ripple usually found in all charge pumps. Although smaller capacitors will cost less and save board space, lower values will reduce the output drive capability and also increase the output ripple.
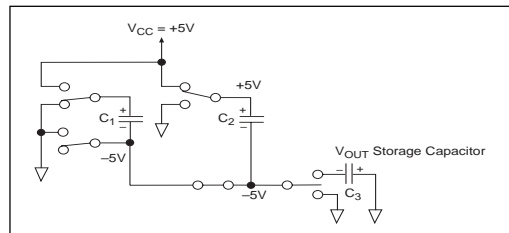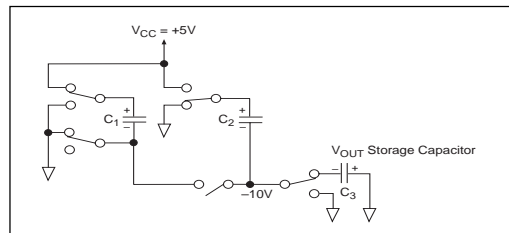

Figure 4. Charge Pump Phase 1

Figure 5. Charge Pump Phase 2

Figure 3. Charge Pump Waveform

The ESR of the charge pump capacitors also determine the output resistance. Assuming that switch resistances are approximately equal, the output resistance can be derived as shown below:

$$R_{OUT} = 16*(R_{SW1-4}) + 4*(ESR_{C1} + ESR_{C2}) + ESR_{C3} \\ + 1 / (f_{OSC} * C1) + 1 / (f_{OSC} * C2)$$

R_{OUT} is typically 140Ω at +25°C with VCC at +5V using 3.3μF capacitors. The total internal switch resistance ($16*R_{SW}$) is approximately 90Ω. The table below shows the comparison of R_{OUT} versus C1&C2.

C1, C2 (μF)	ROUT (Ω)
0.05	4085
0.10	2084
0.47	510
1.00	285
3.30	140
4.70	125
10.00	105
22.00	94

Table 1. R_{OUT} .vs. C1, C2

The output voltage ripple is also affected by the capacitors, specifically C_{OUT}. Larger values will reduce the output ripple for a given load of current. The formula representation is:

$$V_{RIPPLE} = \{1 / [2 * (f_{OSC} * C3)] + 2 * (ESR_{C3})\} * I_{OUT}$$

To minimize the output ripple, the C_{OUT} storage capacitor can be increased to over 10μF whereas the pump capacitors can range from 1μF to 5μF. *Table 2* shows the typical V_{RIPPLE} for given C_{OUT} values.

C_{OUT} (μF)	V_{RIPPLE} (mV)
0.50	1020
1.00	520
3.30	172
4.70	120
10.00	70
22.00	43

Table 2. C3 .vs. V_{RIPPLE}

SHUTDOWN FEATURE

The **SP682** charge pump includes a shutdown feature (pin 8) which disables the charge pump when the V_{OUT} is not needed. A logic "1" will activate the shutdown. If shutdown is not needed, it can be left open where an internal pull-down resistor will always keep the charge pump active. Typical input current for the shutdown pin is 3μA. The shutdown feature is another option for conserving power in portable applications.
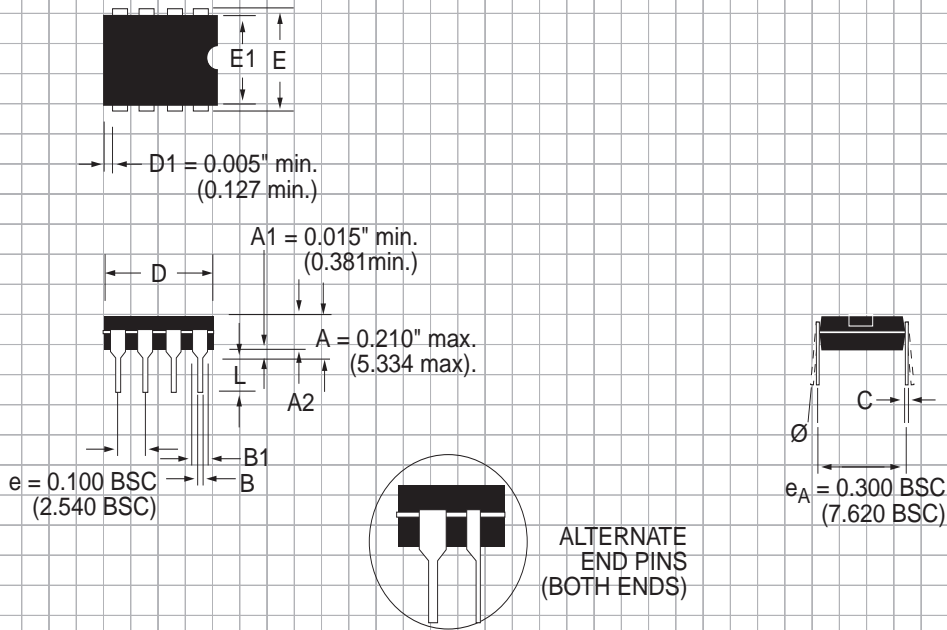
PARALLEL DEVICES

Multiple **SP682** charge pumps can be connected in parallel. However, the effective output resistance now is the output resistance of a single device divided by the number of devices. Connecting multiple pumps allows the user to save on the storage capacitor. The charge pump capacitors still must be separate for each device.

APPLICATIONS INFORMATION

The **SP682** charge pump produces a doubled, inverted voltage from the V_{CC} input. As such, it can serve in many applications where a negative –5V to –10V output is needed. Typical applications include powering analog switches, and biasing LCD displays and panels.
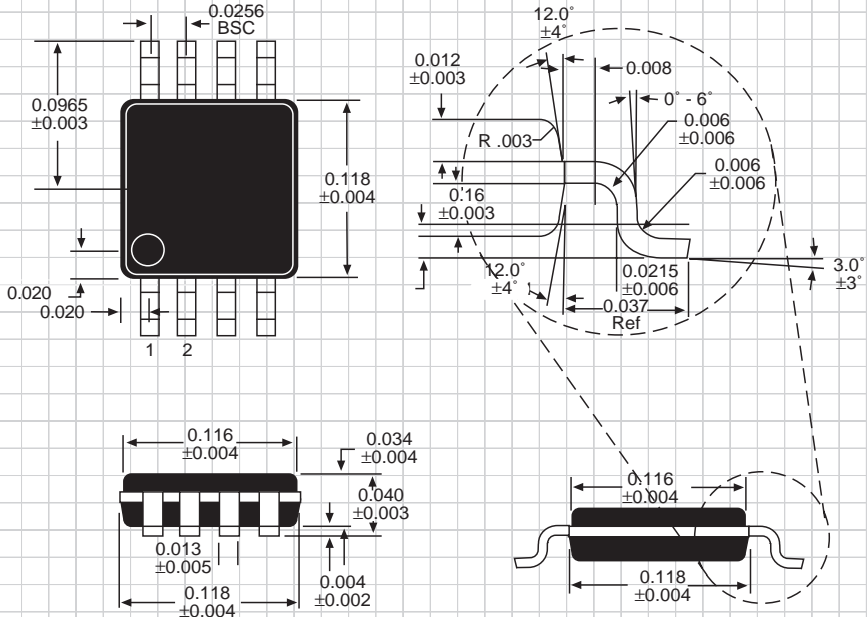
PACKAGE: 8-PIN PLASTIC DUAL–IN–LINE (NARROW)

E1 | E

D1 = 0.005" min.
(0.127 min.)

A1 = 0.015" min.
(0.381 min.)

D

A = 0.210" max.
(5.334 max).

L

A2

B1

e = 0.100 BSC
(2.540 BSC)

B

C

Ø

e_A = 0.300 BSC
(7.620 BSC)

ALTERNATE
END PINS
(BOTH ENDS)

DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)

PACKAGE: 8-PIN PLASTIC SMALL OUTLINE (SOIC) (NARROW)
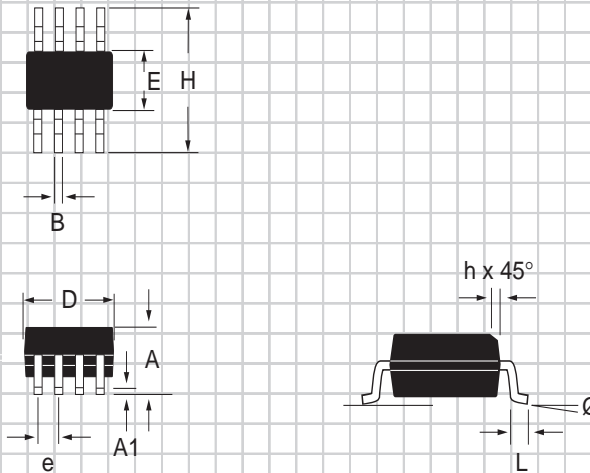
DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249
B	0.014/0.019 (0.35/0.49)
D	0.189/0.197 (4.80/5.00)
E	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

PACKAGE: PLASTIC MICRO SMALL OUTLINE (μSOIC)

0.0256 BSC

0.0965 ±0.003

0.118 ±0.004

0.020

0.020

1 2

12.0° ±4°

0.012 ±0.003

0.008

0° - 6°

0.006 ±0.006

R .003

0.006 ±0.006

0.16 ±0.003

12.0° ±4°

0.0215 ±0.006

3.0° ±3°

0.037 Ref

0.116 ±0.004

0.034 ±0.004

0.040 ±0.003

0.013 ±0.005

0.118 ±0.004

0.004 ±0.002

0.116 ±0.004

0.118 ±0.004

All package dimensions in inches
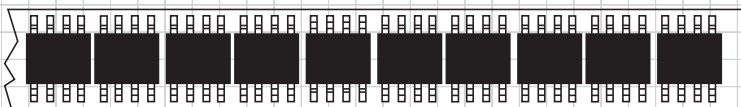
50 μSOIC devices per tube

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP682CP	-0°C to +70°C	8-pin Plastic DIP
SP682CN	-0°C to +70°C	8-pin Plastic SOIC
SP682CU	-0°C to +70°C	8-pin Plastic μSOIC
SP682EP	-40°C to +85°C	8-pin Plastic DIP
SP682EN	-40°C to +85°C	8-pin Plastic SOIC
SP682EU	-40°C to +85°C	8-pin Plastic μSOIC

Sipex
Corporation

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