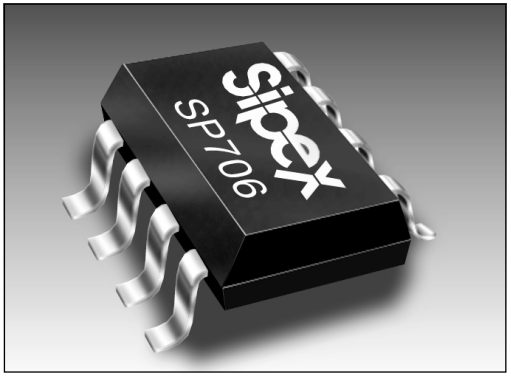
+3.0V/+3.3V Low Power Microprocessor Supervisory Circuits

- Precision Low Voltage Monitor:
  SP706P/R and **SP708R** at +2.63V
  SP706S and **SP708S** at +2.93V
  SP706T and **SP708T** at +3.08V
- RESET Pulse Width - 200ms
- Independent Watchdog Timer - 1.6 sec Timeout (**SP706P/S/R/T**)
- 40µA Maximum Supply Current
- Debounced TTL/CMOS Manual-Reset Input
- $\overline{\text{RESET}}$ Asserted Down to V_{CC} = 1V
- RESET Output:
  SP706P Active-High
  SP706R/S/T Active-Low
  SP708R/S/T Both Active High + Active Low
- WDI Can Be Left Floating, Disabling the Watchdog Function



- Built-In V_{cc} Glitch Immunity
- Available in 8-pin PDIP, NSOIC, and µSOIC packages
- Voltage Monitor for Power Failure or Low Battery Warning
- Pin Compatible Enhancement to Industry Standards **706P/R/S/T** and **708R/S/T**

DESCRIPTION

The SP706P/S/R/T, SP708R/S/T series is a family of microprocessor (µP) supervisory circuits that integrate myriad components involved in discrete solutions which monitor power-supply and battery, in µP, and digital systems. The SP706P/S/R/T, SP708R/S/T series will significantly improve system reliability and operational efficiency when compared to results obtained with discrete components. The features of the SP706P/S/R/T, SP708R/S/T series include a watchdog timer, a µP reset, a Power Fail Comparator, and a manual-reset input. The SP706P/S/R/T, SP708R/S/T series is ideal for +3.0V or +3.3V applications in automotive systems, computers, controllers, and intelligent instruments. The SP706P/S/R/T, SP708R/S/T series is an ideal solution for systems in which critical monitoring of the power supply to the µP and related digital components is demanded.

Part Number	RESET Active	RESET Threshold	Manual Reset	PFI Accuracy	Watchdog Input
SP706P	HIGH	2.63V	YES	4%	YES
SP706R	LOW	2.63V	YES	4%	YES
SP706S	LOW	2.93V	YES	4%	YES
SP706T	LOW	3.08V	YES	4%	YES
SP708R	LOW/HIGH	2.63V	YES	4%	NO
SP708S	LOW/HIGH	2.93V	YES	4%	NO
SP708T	LOW/HIGH	3.08V	YES	4%	NO

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Terminal Voltage (with respect to GND):
V_{CC}.....-0.3V to +6.0V
All Other Inputs (Note 1).....-0.3V to (V_{CC} +3.0V)

Input Current:
V_{CC}.....20mA
GND.....20mA
Output Current (all outputs).....20mA
ESD Rating.....2kV

Continuous Power Dissipation
Plastic DIP
(derate 9.09mW/^{O}C above +70^{O}C).....727mW
SO
(derate 5.88mW/^{O}C above +70^{O}C).....471mW
Mini SO
(derate 4.10mW/^{O}C above +70^{O}C).....330mW
Storage Temperature Range.....-65˚C to +160˚C
Lead Temperature (solding 10 sec).....+300˚C

SPECIFICATIONS

V_{cc} = 2.7V to 5.5V for SP70_P/R, V_{CC} = 3.0 to 5.5V for SP70_S, V_{CC} = 3.15V to 5.5V for SP70_T, T_A= T_{MIN} to T_{MAX} to T_{MAX}, unless otherwise noted, typical at 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, V_{CC}	1.0		5.5	V	
Supply Current, I_{SUPPLY}		25	40	µA	MR=V_{CC} or Floating, WDI Floating
Reset Threshold	2.55 2.85 3.00	2.63 2.93 3.08	2.70 3.00 3.15	V	**SP70_P/R** **SP70_S** **SP70_T**
Reset Threshold Hysteresis		20		mV	Note 2
Reset Pulse Width, t_{RS}	140	200	280	ms	Note 2
$\overline{RESET}$ Output Voltage					
V_{OH}	0.8xV_{CC}			V	$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE} = 500µA
V_{OL}			0.3		$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SINK} =1.2mA
V_{OH}	V_{CC}-1.5				4.5V<V_{CC}<5.5V, I_{SOURCE} = 800µA
V_{OL}			0.4		4.5V<V_{CC}<5.5V, I_{SINK} = 3.2mA
RESET Output Voltage					
V_{OH}	V_{CC}-0.6			V	$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE} = 215µA
V_{OL}			0.3		$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE} =1.2mA
V_{OH}	V_{CC}-1.5				4.5V<V_{CC}<5.5V, I_{SOURCE} = 800µA
V_{OL}			0.4		4.5V<V_{CC}<5.5V, I_{SOURCE} = 3.2mA
Watchdog Timeout Period, t_{WD}	1.00	1.60	2.25	s	V_{CC}<3.6V
WDI Pulse Width, t_{WP}	50			ns	V_{IL} = 0.4V, V_{IH} = 0.8xV_{CC}
WDI Input Threshold,					
V_{IL}			0.6	V	$V_{RST\ (MAX)}$ <V_{CC} <3.6V
V_{IH}	0.7xV_{CC}				$V_{RST\ (MAX)}$ <V_{CC} <3.6V
V_{IL}			0.8		V_{CC} = 5.0V
V_{IH}	3.5				V_{CC} = 5.0V
WDI Input Current	-1	0.02	1	µA	WDI = 0 or V_{CC}

SPECIFICATIONS (continued)

V_{cc} = 2.7V to 5.5V for SP70_P/R, V_{CC} = 3.0 to 5.5V for SP70_S, V_{CC} = 3.15V to 5.5V for SP70_T, T_A= T_{MIN} to T_{MAX} to T_{MAX}, unless otherwise noted, typical at 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$\overline{WDO}$ Output Voltage					
V_{OH}	$0.8xV_{CC}$				$V_{RST(MAX)}<V_{CC}<3.6V$, I_{SOURCE} = 500µA
V_{OL}			0.3	V	$V_{RST(MAX)}<V_{CC}<3.6V$, I_{SINK} =1.2mA
V_{OH}	V_{CC}-1.5				4.5V<V_{CC}<5.5V, I_{SOURCE} = 800µA
V_{OL}			0.4		4.5V<V_{CC}<5.5V, I_{SINK} = 3.2mA
$\overline{MR}$ Pull-Up Current	25	70	250	µA	MR = 0V,$V_{RST(MAX)}<V_{CC}<3.6V$
	100	250	600		MR = 0V,4.5V<V_{CC}<5.5V
$\overline{MR}$ Pulse Width, t_{MR}	500			ns	$V_{RST(MAX)}<V_{CC}<3.6V$
	150				4.5V<V_{CC}<5.5V
$\overline{MR}$ Input Threshold					
V_{IL}			0.6		$V_{RST(MAX)}<V_{CC}<3.6V$
V_{IH}	$0.7xV_{CC}$			V	$V_{RST(MAX)}<V_{CC}<3.6V$
V_{IL}			0.8		4.5V<V_{CC}<5.5V
V_{IH}	2.0				4.5V<V_{CC}<5.5V
$\overline{MR}$ to Reset Out Delay, t_{MD}			750	ns	$V_{RST(MAX)}<V_{CC}<3.6V$,NOTE 2
			250		4.5V<V_{CC}<5.5V,NOTE 2
PFI Input Threshold	1.20	1.25	1.30	V	V_{CC} = 3.0V for the **SP70_P/R**,V_{CC} = 3.3V for the **SP70_S/T**,PFI falling
PFI Input Current	-25.00	0.01	25.00	nA	
$\overline{PFO}$ Output Voltage					
V_{OH}	$0.8xV_{CC}$				$V_{RST(MAX)}<V_{CC}<3.6V$, I_{SOURCE} = 500µA
V_{OL}			0.3	V	$V_{RST(MAX)}<V_{CC}<3.6V$,I_{SINK} =1.2mA
V_{OH}	V_{CC}-1.5				4.5V<V_{CC}<5.5V, I_{SOURCE} = 800µA
V_{OL}			0.4		4.5V<V_{CC}<5.5V, I_{SINK} = 3.2mA

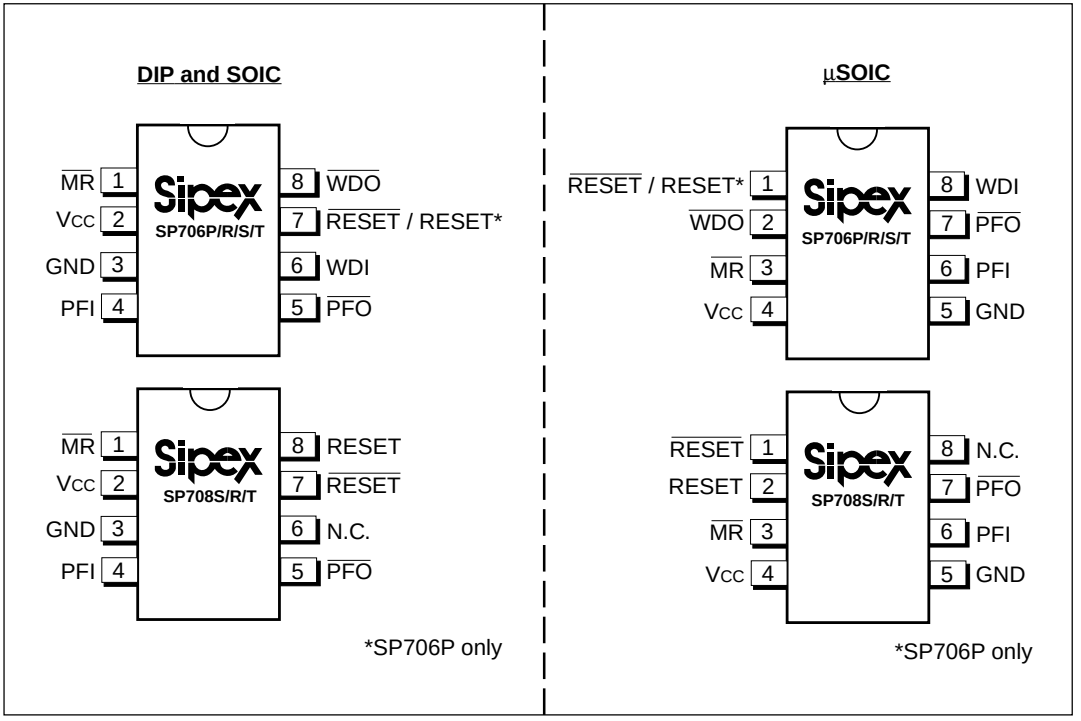


Figure 1. Pinouts

NAME	FUNCTION	PIN DESCRIPTION					
		SP706P		SP706R/S/T		SP708R/S/T	
		DIP/ SOIC	µSOIC	DIP/ SOIC	µSOIC	DIP/ SOIC	µSOIC
$\overline{MR}$	Manual Reset - This input triggers a reset pulse when pulled below 0.8V. This active-LOW input has an internal 70µA pull-up current. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch	1	3	1	3	1	3
V_{CC}	Voltage input.	2	4	2	4	2	4
GND	Ground reference for all signals	3	5	3	5	3	5
PFI	Power-Fail Input - When this voltage monitor input is less than 1.25V, $\overline{PFO}$ goes LOW. Connect PFI to ground or V_{CC} when not in use.	4	6	4	6	4	6
$\overline{PFO}$	Power-Fail Output - This output is HIGH until PFI is less than 1.25V.	5	7	5	7	5	7
WDI	Watchdog Input - If this input remains HIGH or LOW for 1.6s, the internal watchdog timer times out and $\overline{WDO}$ goes LOW. Floating WDI or connecting WDI to a high-impedance tri-state buffer disables the watchdog feature. The internal watchdog timer clears whenever $\overline{RESET}$ is asserted, WDI is tri-stated, or whenever WDI sees a rising or falling edge.	6	8	6	8	-	-
N.C.	No Connect.	-	-	-	-	6	8
$\overline{RESET}$	Active-LOW $\overline{RESET}$ Output - This output pulses LOW for 200ms when triggered and stays LOW whenever V_{CC} is below the reset threshold. It remains LOW for 200ms after V_{cc} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to MR.	-	-	7	1	7	1
$\overline{WDO}$	Watchdog Output - This output pulls LOW when the internal watchdog timer finishes its 1.6s count and does not go HIGH again until the watchdog is cleared. WDO also goes LOW during low-line conditions. Whenever V_{CC} is below the reset threshold, WDO stays LOW. However, unlike $\overline{RESET}$, WDO does not have a minimum pulse width. As soon as V_{CC} is above the reset threshold, WDO goes HIGH with no delay.	8	2	8	2	-	-
RESET	Active-HIGH RESET Output - This output is the complement of $\overline{RESET}$. Whenever RESET is HIGH, $\overline{RESET}$ is LOW, and vice versa. Note the **SP708R/S/T** has a reset output only.	7	1	-	-	8	2

Table 1. Device Pin Description

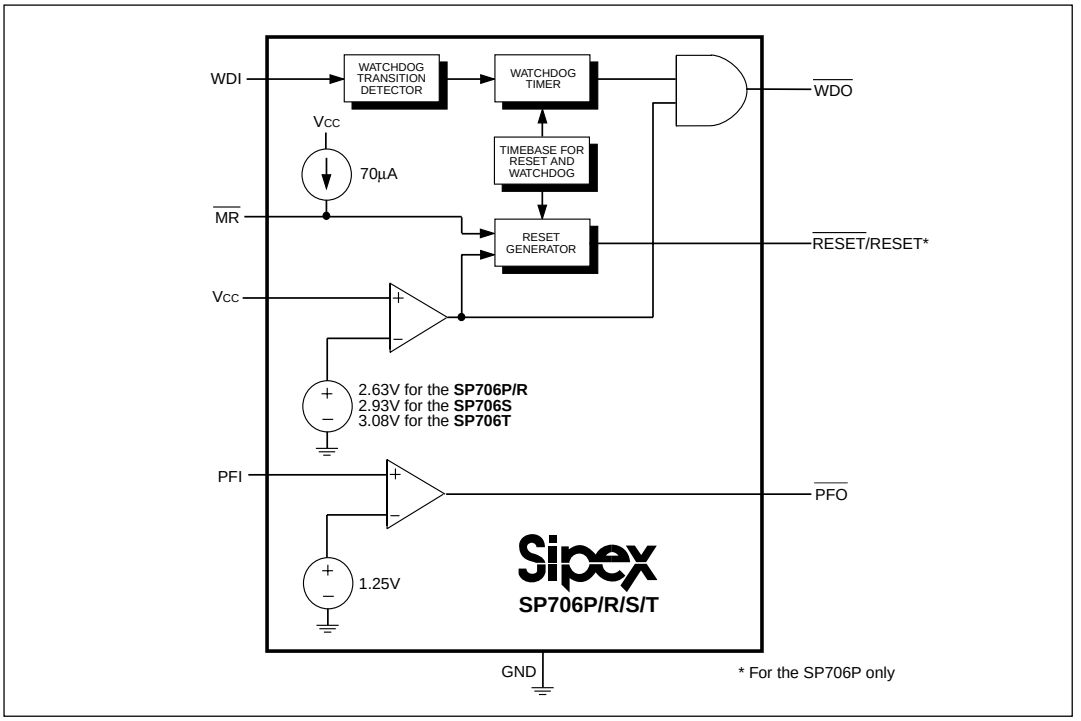
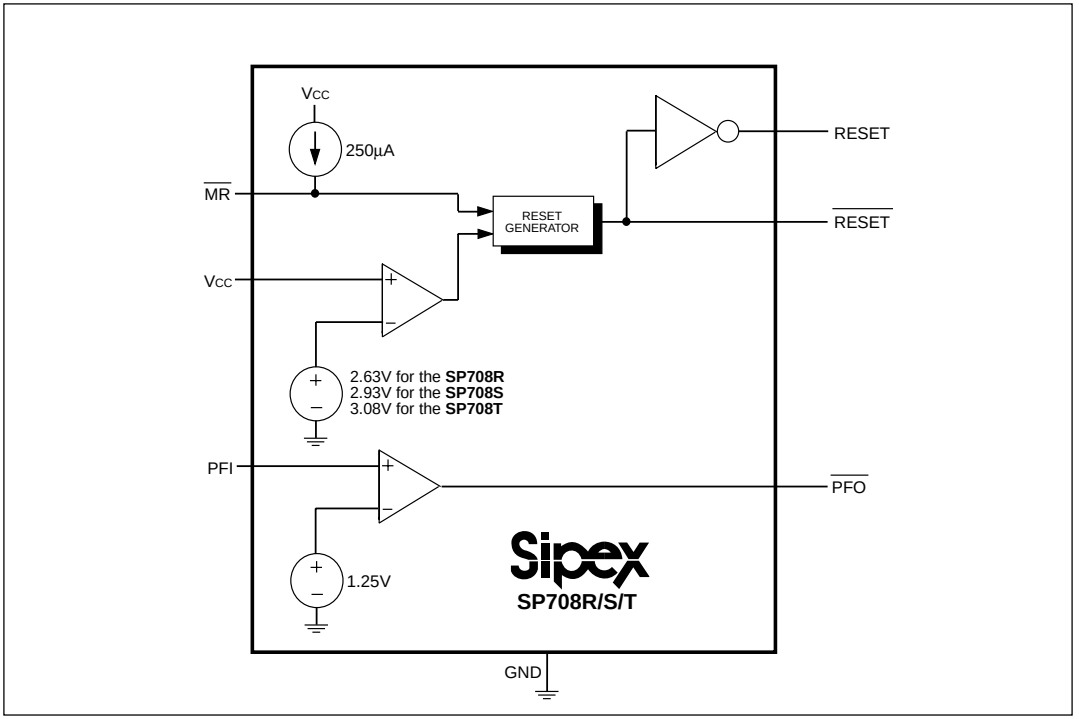


Figure 2. Internal Block Diagram for the SP706P/R/S/T



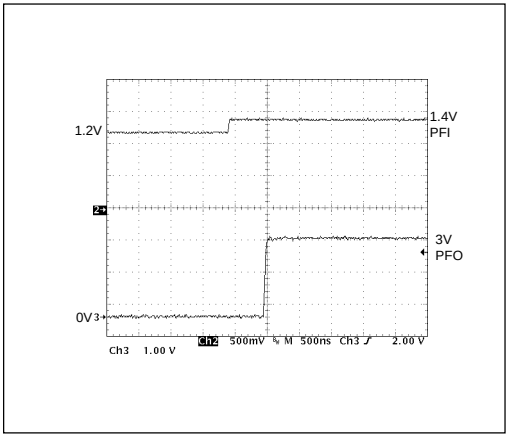


Figure 4A. Power-Fail Comparator De-assertion Response Time.

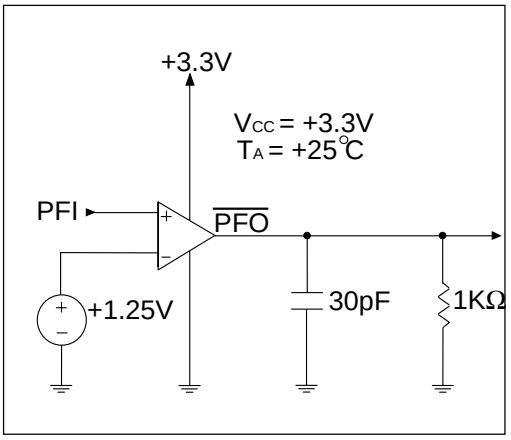


Figure 4B. Circuit for the Power-Fail Comparator De-assertion Response Time.

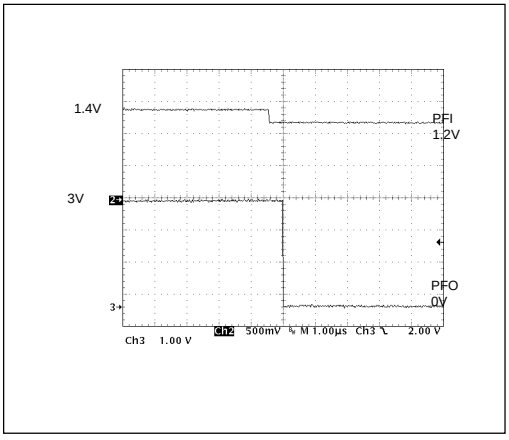


Figure 5A. Power-Fail Comparator Assertion Response Time.

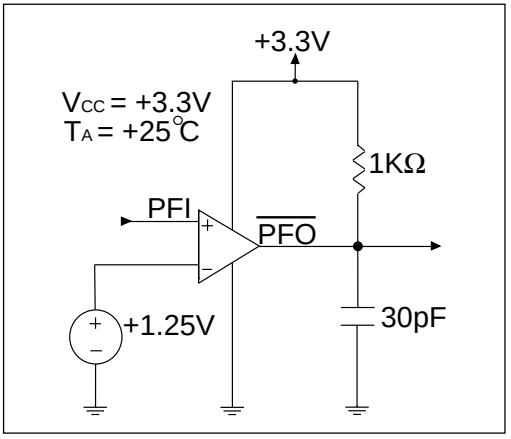


Figure 5B. Circuit for the Power-Fail Comparator Assertion Response Time.

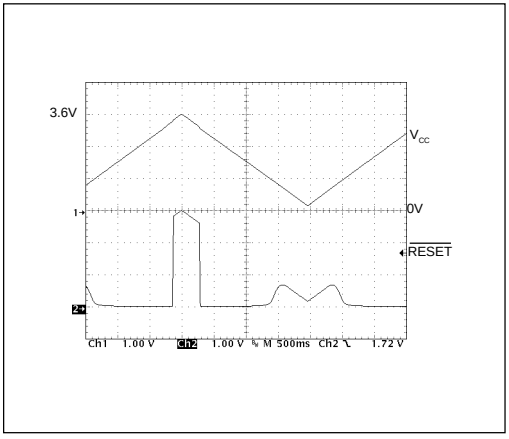


Figure 6A. SP706 $\overline{RESET}$ Output Voltage vs. Supply Voltage.

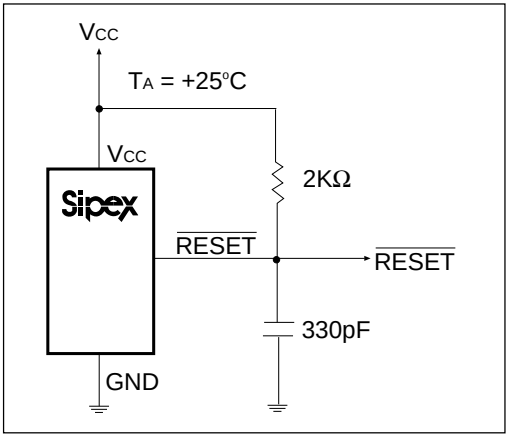


Figure 6B. Circuit for the SP706 $\overline{RESET}$ Output Voltage vs. Supply Voltage.

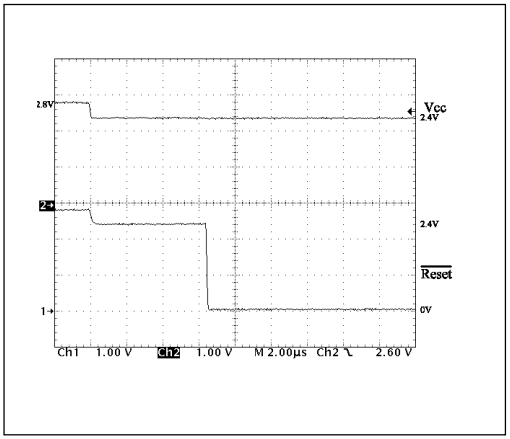


Figure 7A. SP706 $\overline{RESET}$ Response Time

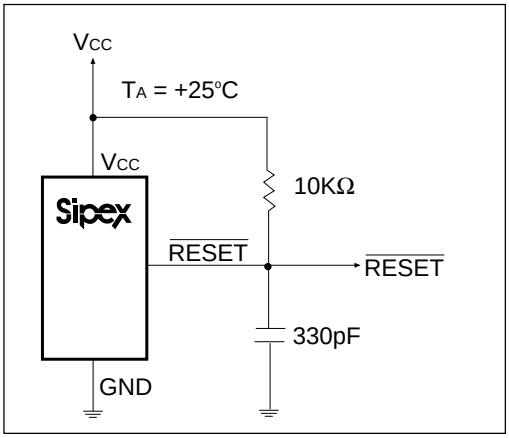


Figure 7B. Circuit for the SP706 $\overline{RESET}$ Response Time

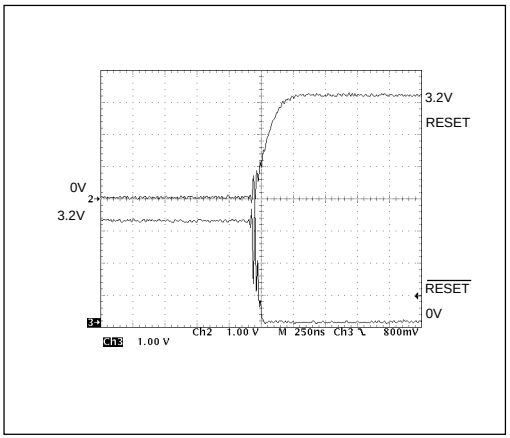


Figure 8. SP708 RESET and $\overline{RESET}$ Assertion

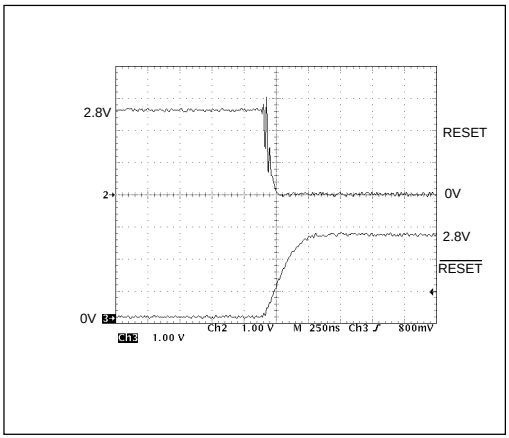


Figure 9. SP708 RESET and $\overline{RESET}$ De-Assertion

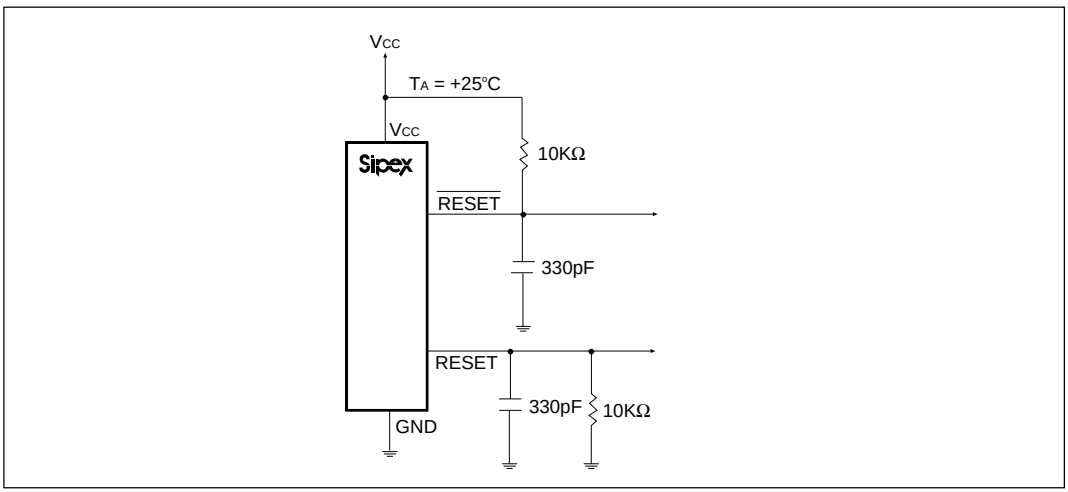


Figure 10. Circuit for the SP708 RESET and $\overline{RESET}$ Assertion and De-Assertion

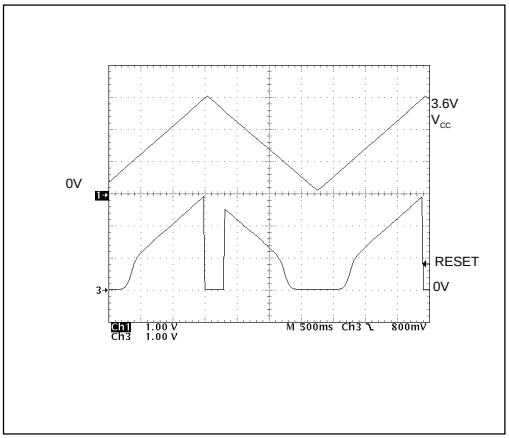


Figure 11. SP708 RESET Output Voltage vs. Supply Voltage

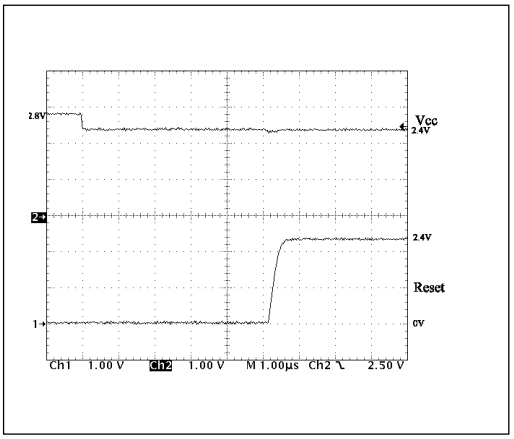


Figure 12. SP708 RESET Response Time

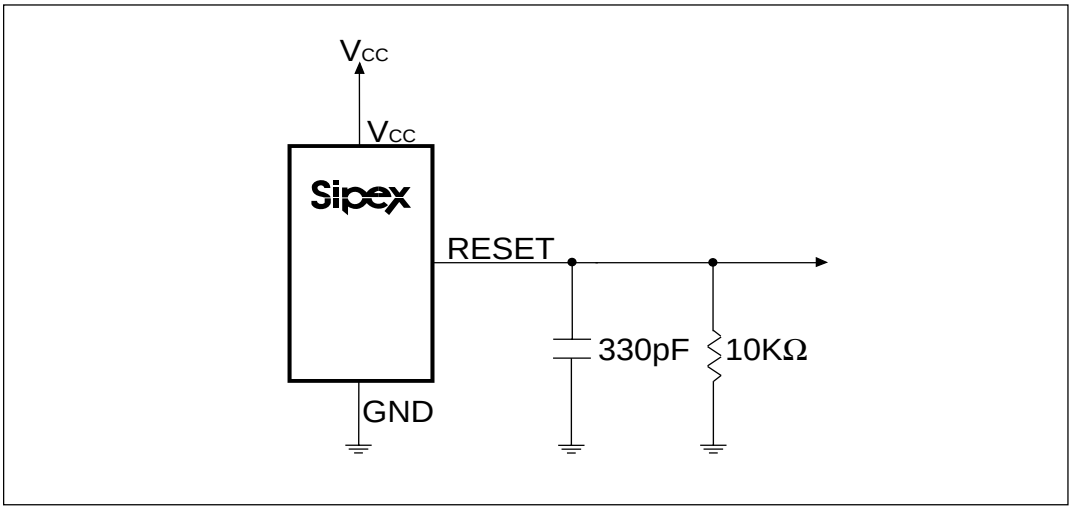


Figure 13. Circuit for the SP708 RESET Output Voltage vs. Supply Voltage and the RESET Response Time Figures

FEATURES

The SP706P/R/S/T-SP708R/S/T series provides four key functions:

1. A reset output during power-up, power-down and brownout conditions.
2. An independent watchdog output that goes LOW if the watchdog input has not been toggled within 1.6 sec.
3. A 1.25V threshold detector for power-fail warning, low battery detection, or monitoring a power supply other than +3.3V/+3.0V.
4. An active-LOW manual-reset that allows RESET to be triggered by a pushbutton switch.

The SP706R/S/T devices are the same as the SP708R/S/T devices except for the active-HIGH RESET substitution of the watchdog timer. The SP706P device is the same as the SP706R device except an active-HIGH RESET is provided rather than an active-LOW $\overline{\text{RESET}}$.

THEORY OF OPERATION

The SP706P/R/S/T-SP708R/S/T series is a microprocessor (µP) supervisory circuit that monitors the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity of a system. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the SP706P/R/S/T-SP708R/S/T series are described, in more detail, below.

RESET Output

A microprocessor's reset input starts the µP in a known state. The SP706P/R/S/T-SP708R/S/T series asserts reset during power-up and prevents code execution errors during power-down or brownout conditions.

During power-up, once V_{CC} reaches 1V, $\overline{\text{RESET}}$ is a guaranteed logic LOW of 0.4V or less. As V_{CC} rises, RESET stays LOW. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after 200ms. $\overline{\text{RESET}}$ pulses LOW whenever V_{CC} dips below the reset threshold, such as in a brownout condition. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. During power-down, once V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The active-HIGH RESET output is simply the complement of the $\overline{\text{RESET}}$ output and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-HIGH reset pulse.

Watchdog Timer

The SP706P/R/S/T-SP708R/S/T series watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not tri-stated, $\overline{\text{WDO}}$ goes LOW. As long as $\overline{\text{RESET}}$ is asserted or the WDI input is tri-stated, the watchdog timer will stay cleared and will not count. As soon as $\overline{\text{RESET}}$ is released and WDI is driven HIGH or LOW, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{\text{WDO}}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{\text{WDO}}$ will go LOW independent of the current status of the watchdog timer. Normally this would trigger an NMI but $\overline{\text{RESET}}$ goes LOW simultaneously, and thus overrides the NMI.

If WDI is left unconnected, $\overline{\text{WDO}}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{\text{WDO}}$ goes LOW only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

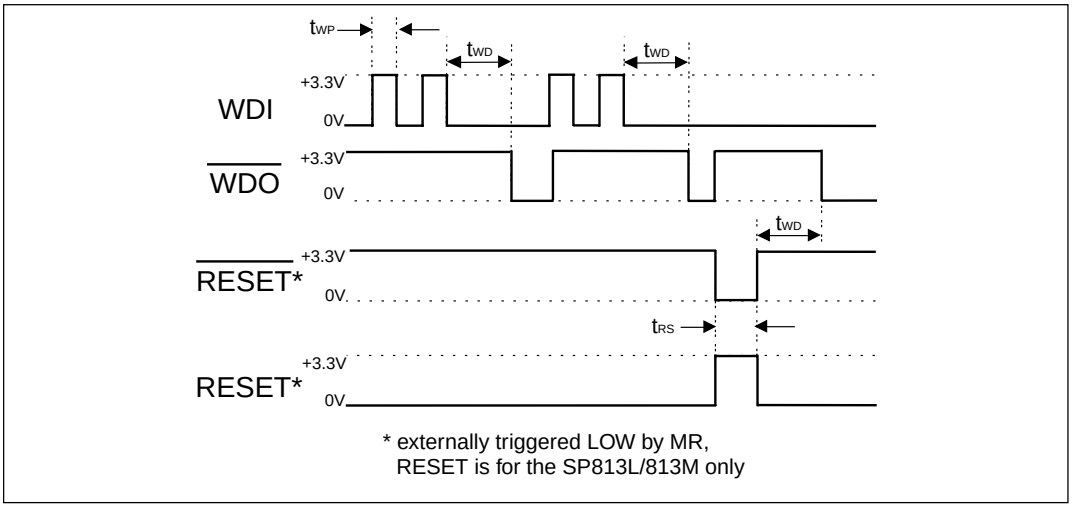


Figure 14. Watchdog Timing Waveforms

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider as shown in *Figure 16*. Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

Manual Reset

The manual-reset input ($\overline{MR}$) allows RESET to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum RESET pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a RESET pulse in the SP706P/R/S/T-SP708R/S/T series. Simply connect $\overline{WDO}$ to $\overline{MR}$.

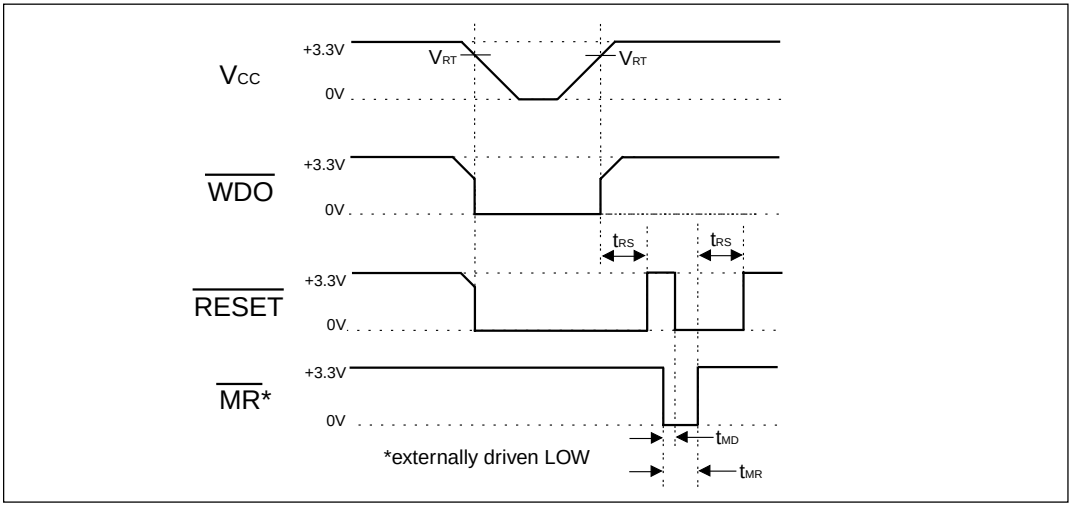


Figure 15. Timing Diagrams with WDI Tri-stated. The RESET Output is the Inverse of the RESET Waveform Shown.

Ensuring a Valid RESET Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the $\overline{RESET}$ output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{RESET}$ pin, any stray charge or leakage currents will be shunted to ground, holding $\overline{RESET}$ LOW. The resistor value is not critical. It should be about 100KΩ, large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{RESET}$ can be used to monitor voltages other than the +3.3V/+3.0V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a RESET pulse when PFI drops below 1.25V. *Figure 17* shows the SP706R/S/T-SP708R/S/T series configured to assert $\overline{RESET}$ when the +3.3V/+3.0V supply falls below the RESET threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage Supply

The power-fail comparator can also monitor a negative supply rail, shown in *Figure 18*. When the negative rail is good (a negative voltage of large magnitude), PFO is LOW. By adding the resistors and transistor as shown, a HIGH PFO triggers RESET. As long as PFO remains HIGH, the SP706P/R/S/T-SP708R/S/T series will keep RESET asserted (where $\overline{RESET}$ = LOW and RESET = HIGH). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

Interfacing to mPs with Bidirectional RESET Pins

µPs with bidirectional RESET pins, such as the Motorola 68HC11 series, can contend with the $\overline{RESET}$ output. If, for example, the $\overline{RESET}$

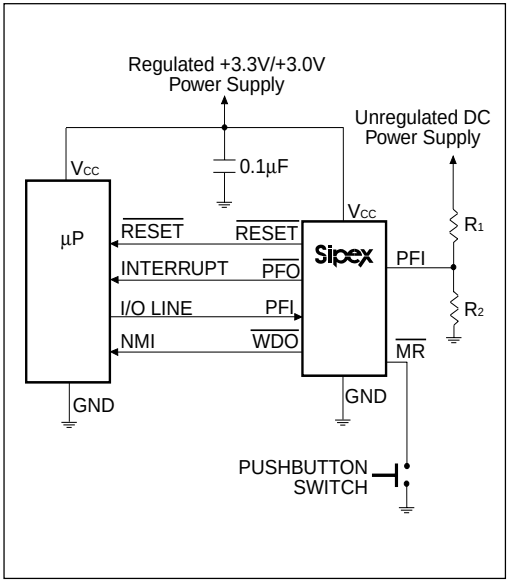


Figure 16. Typical Operating Circuit

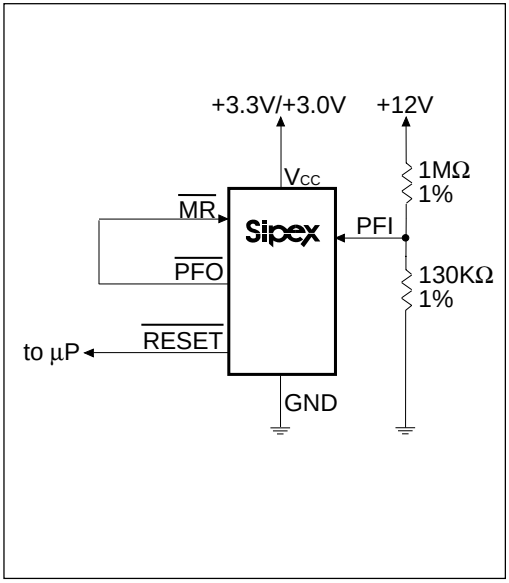


Figure 17. Monitoring Both +3.3V/+3.0V and +12V Power Supplies

output is driven HIGH and the µP wants to pull it LOW, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{\text{RESET}}$ output and the µP reset I/O, as shown if *Figure 19*. Buffer the $\overline{\text{RESET}}$ output to other system components.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 20 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are not generated. The data was generated using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e. goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued. A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Applications

The SP706P/R/S/T-SP708R/S/T series offers unmatched performance and the lowest power consumption for these industry standard devices. Refer to *Figures 21* and *22* for supply current performance characteristics rated against temperature and supply voltages.

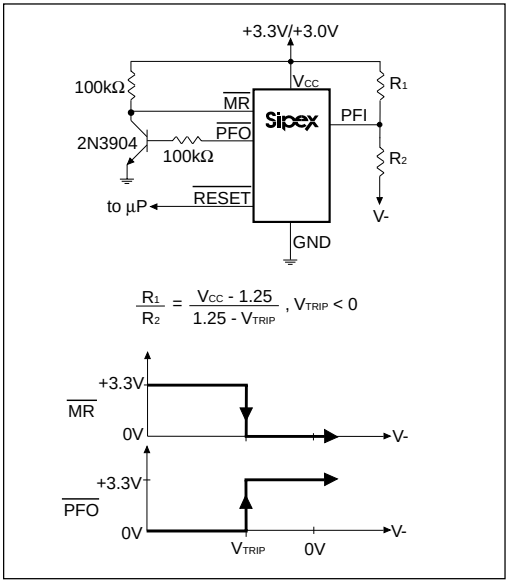


Figure 18. Monitoring a Negative Voltage Supply

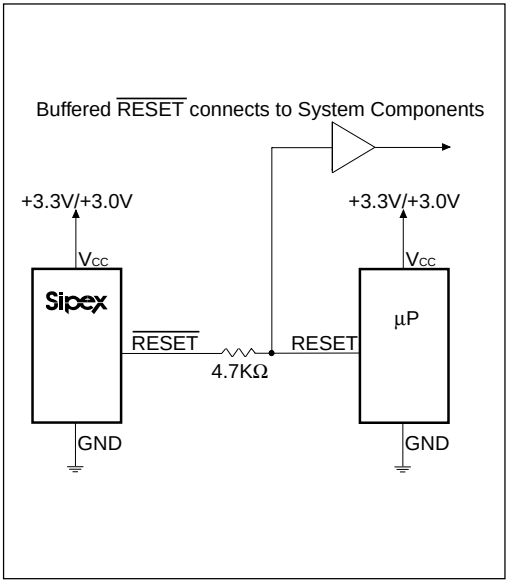


Figure 19. Interfacing to Microprocessors with Bidirectional RESET I/O for the SP706

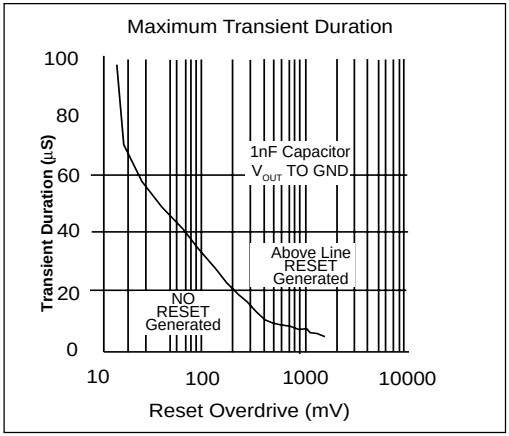


Figure 20. Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

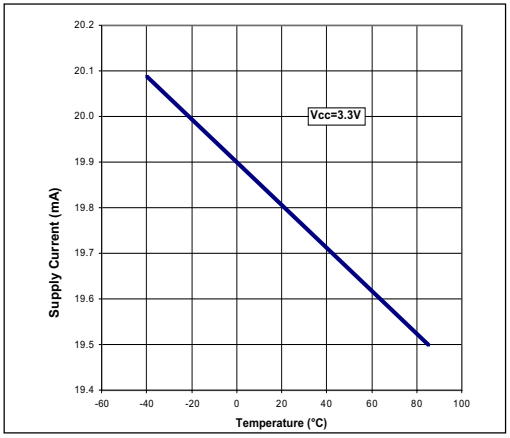


Figure 21. Supply Current vs. Temperature

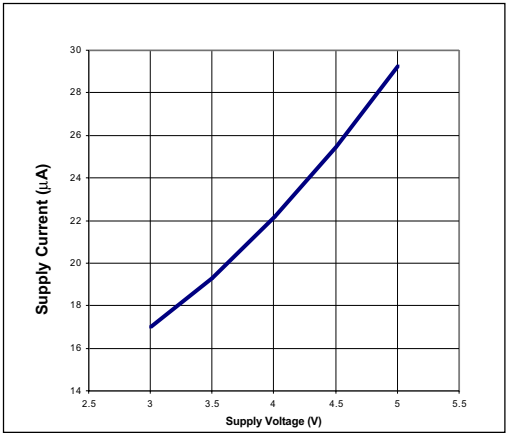
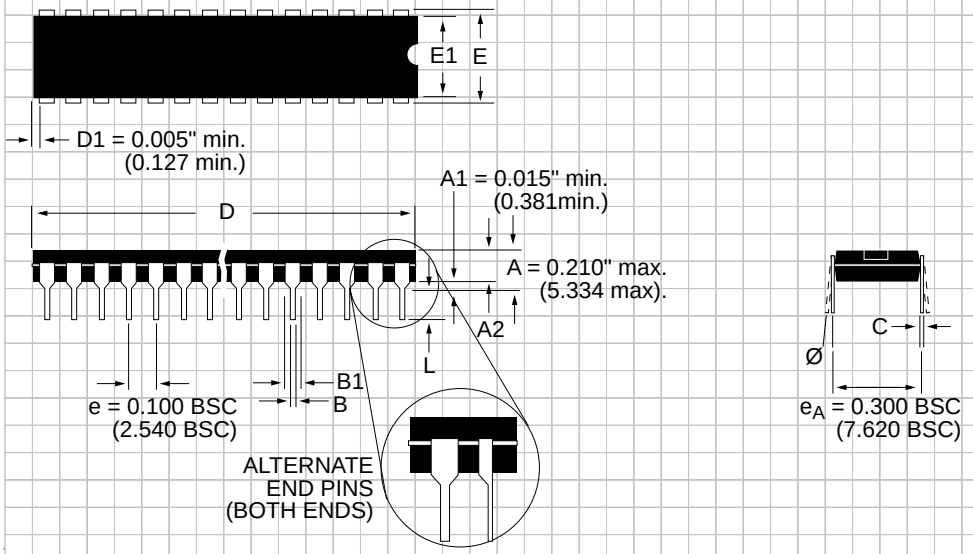


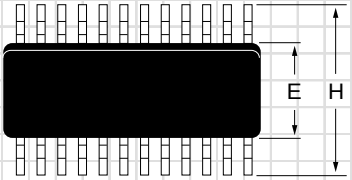
Figure 22. Supply Current vs. Supply Voltage

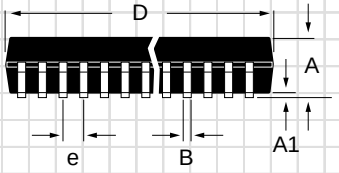
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

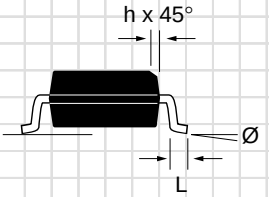


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)

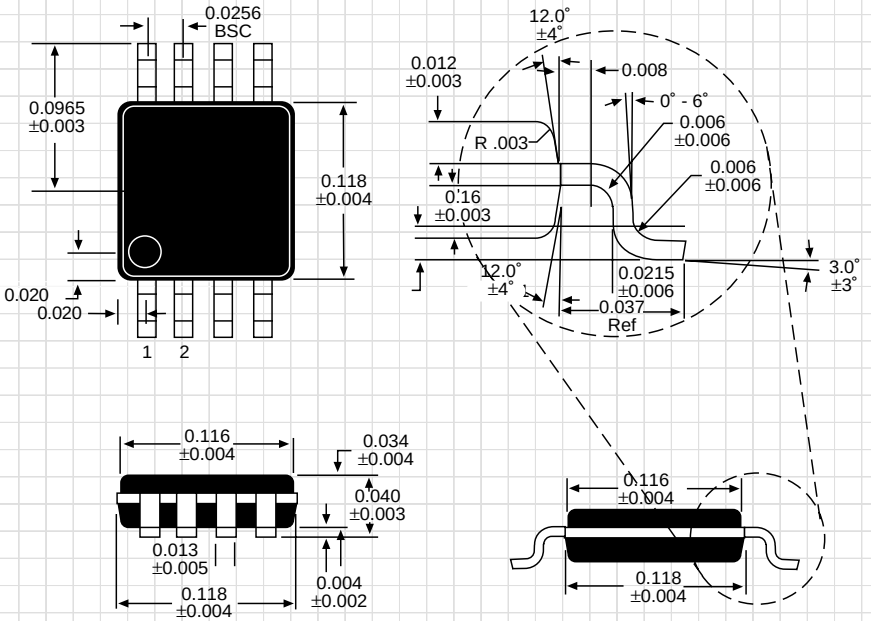




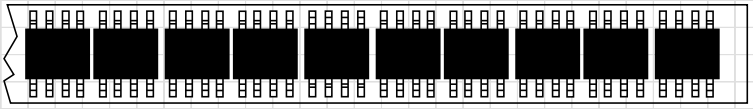


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249
B	0.014/0.019 (0.35/0.49)
D	0.189/0.197 (4.80/5.00)
E	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

PACKAGE: PLASTIC MICRO SMALL OUTLINE (μSOIC)



All package dimensions are in inches



50 USOIC devices per tube

ORDERING INFORMATION

Model	Temperature Range	Package
SP706PCP	0°C to +70°C	8–pin PDIP
SP706PCN	0°C to +70°C	8–pin NSOIC
SP706PCU	0°C to +70°C	8-pin µSOIC
SP706RCP	0°C to +70°C	8–pin PDIP
SP706RCN	0°C to +70°C	8–pin NSOIC
SP706RCU	0°C to +70°C	8-pin µSOIC
SP706SCP	0°C to +70°C	8–pin PDIP
SP706SCN	0°C to +70°C	8–pin NSOIC
SP706SCU	0°C to +70°C	8-pin µSOIC
SP706TCP	0°C to +70°C	8–pin PDIP
SP706TCN	0°C to +70°C	8–pin NSOIC
SP706TCU	0°C to +70°C	8-pin µSOIC
SP706PEP	-40°C to +85°C	8–pin PDIP
SP706PEN	-40°C to +85°C	8–pin NSOIC
SP706PEU	-40°C to +85°C	8-pin µSOIC
SP706REP	-40°C to +85°C	8–pin PDIP
SP706REN	-40°C to +85°C	8–pin NSOIC
SP706REU	-40°C to +85°C	8-pin µSOIC
SP706SEP	-40°C to +85°C	8–pin PDIP
SP706SEN	-40°C to +85°C	8–pin NSOIC
SP706SEU	-40°C to +85°C	8-pin µSOIC
SP706TEP	-40°C to +85°C	8–pin PDIP
SP706TEN	-40°C to +85°C	8–pin NSOIC
SP706TEU	-40°C to +85°C	8-pin µSOIC
SP708RCP	0°C to +70°C	8–pin PDIP
SP708RCN	0°C to +70°C	8–pin NSOIC
SP708RCU	0°C to +70°C	8-pin µSOIC
SP708SCP	0°C to +70°C	8–pin PDIP
SP708SCN	0°C to +70°C	8–pin NSOIC
SP708SCU	0°C to +70°C	8-pin µSOIC
SP708TCP	0°C to +70°C	8–pin PDIP
SP708TCN	0°C to +70°C	8–pin NSOIC
SP708TCU	0°C to +70°C	8-pin µSOIC
SP708REP	-40°C to +85°C	8–pin PDIP
SP708REN	-40°C to +85°C	8–pin NSOIC
SP708REU	-40°C to +85°C	8-pin µSOIC
SP708SEP	-40°C to +85°C	8–pin PDIP
SP708SEN	-40°C to +85°C	8–pin NSOIC
SP708SEU	-40°C to +85°C	8-pin µSOIC
SP708TEP	-40°C to +85°C	8–pin PDIP
SP708TEN	-40°C to +85°C	8–pin NSOIC
SP708TEU	-40°C to +85°C	8-pin µSOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600