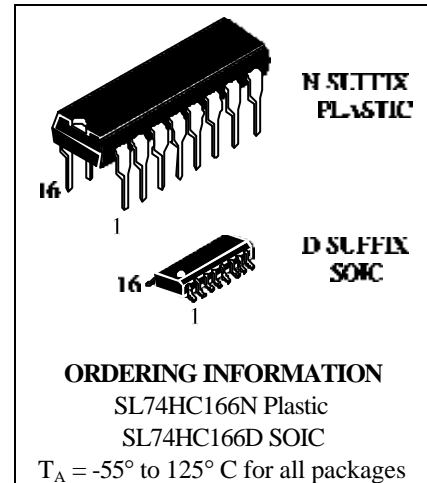


# 8-Bit Serial or Parallel-Input/ Serial-Output Shift Register High-Performance Silicon-Gate CMOS

The SL74HC166 is identical in pinout to the LS/ALS166. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device is a parallel-in or serial-in, serial-out shift register with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flop to zero.

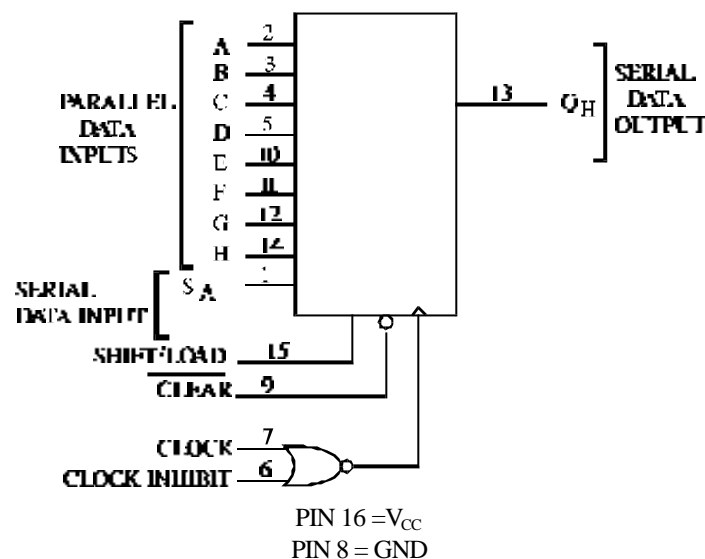
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



### PIN ASSIGNMENT

S <sub>A</sub>	1	16	V <sub>CC</sub>
A	2	15	Shift-Load
B	3	14	I <sub>1</sub>
C	4	13	Q <sub>11</sub>
D	5	12	G
Clock Inhibit	6	11	F
Clock	7	10	E
GND	8	9	Clear

### LOGIC DIAGRAM



# SL74HC166

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC}+1.5$	V
$V_{OUT}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
$I_{IN}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC}=2.0\text{ V}$	0	1000	
	$V_{CC}=4.5\text{ V}$	0	500	
	$V_{CC}=6.0\text{ V}$	0	400	





This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low -Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	8.0	80	160	μA

## FUNCTION TABLE

Inputs						Internal Outputs		Output
Clear	Shift/Load	Clock Inhibit	Clock	S <sub>A</sub>	Parallel A...H	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>H</sub>
L	X	X	X	X	X	L	L	L
H	X	X		X	X	No change		
H	L	L		X	a...h	a	b	h
H	H	L		H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L		L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	X	X	X	No change		

X = don't care

a...h = the level of steady state input voltage at input A through H respectively

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## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Minimum Clock Frequency (50% Duty Cycle) (Figures 2 and 4)	2.0	6.0	5.0	4.2	MHz
		4.5	31	25	21	
		6.0	36	28	25	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q <sub>H</sub> (Figures 2,3 and 4)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t <sub>PHL</sub>	Maximum Propagation Delay, Clear to Q <sub>H</sub> (Figures 1 and 4)	2.0	150	200	230	ns
		4.5	30	40	48	
		6.0	26	34	40	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	16	20	25	
		6.0	14	18	20	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)	Typical @25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	140			

## TIMING REQUIREMENTS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Shift/Load to Clock (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	18	20	
t <sub>su</sub>	Minimum Setup Time, Data before Clock (or Clock Inhibit) (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	18	20	
t <sub>w</sub>	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	

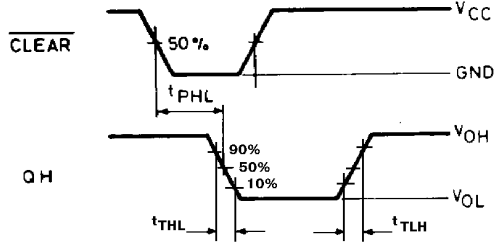


Figure 1. Switching Waveforms

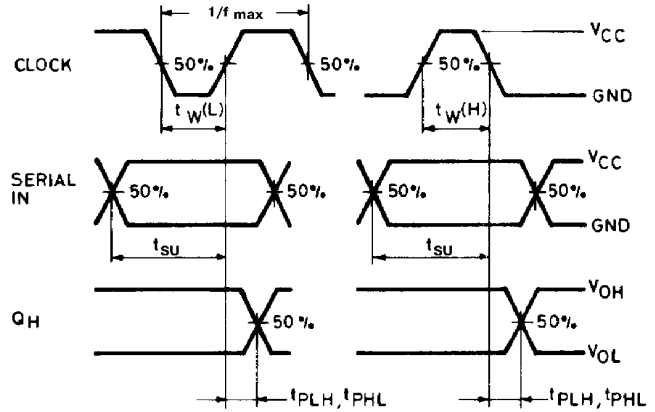


Figure 2. Switching Waveforms

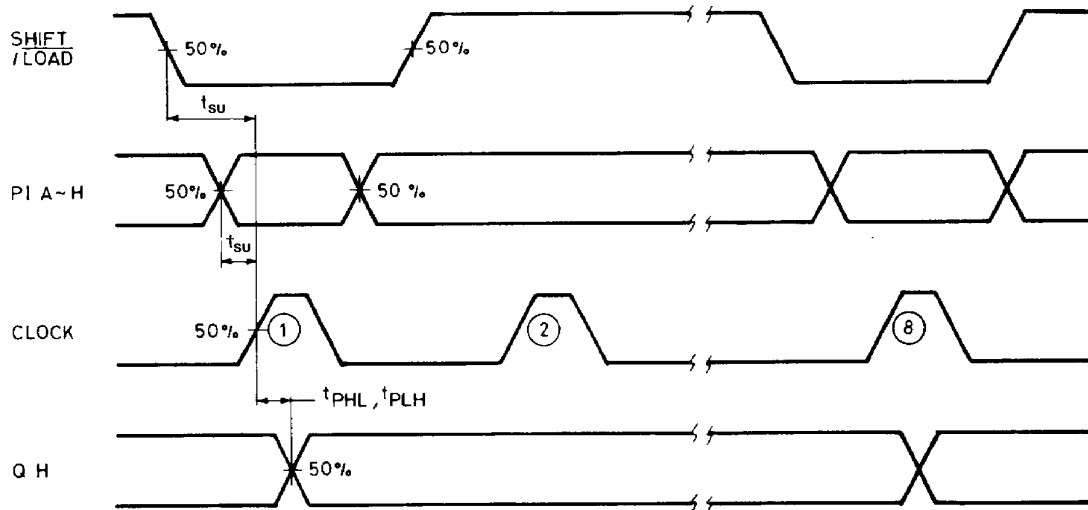
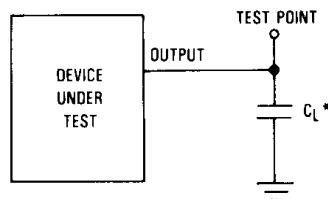


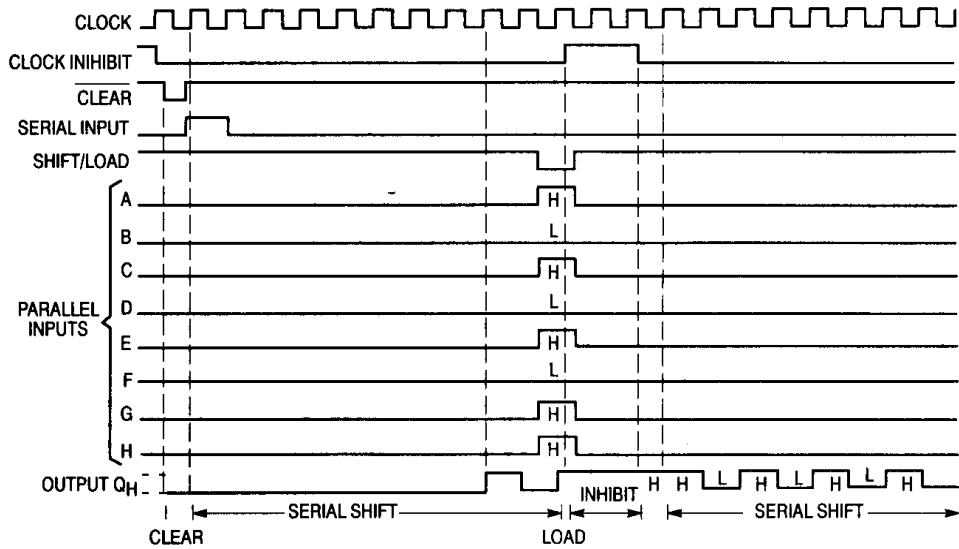
Figure 3. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

## TIMING DIAGRAM



## EXPANDED LOGIC DIAGRAM

