Synchronous 4 Bit Counters; Binary, Direct Reset

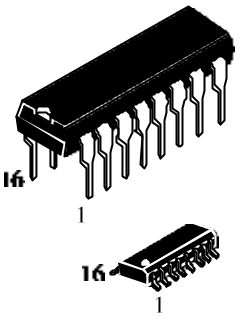
This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change conicident with each other when so instructed by the count-enable inputs and internal gating.

This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input wave form.

This counter is fully programmable; that is the outputs may be preset to either level. As presetting is synchronous setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishiing this function are two counter-enable inputs and a ripple carry output. Both countenable inputs (ENABLE P and ENABLE T) must be high to count, and ENABLE T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high level portion of the Q_A output. The high-level overflow ripple carry pulse can be enable successive cascaded stages. Transitions at the ENPor ENT are allowed regardless of the level of the clock input.

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs



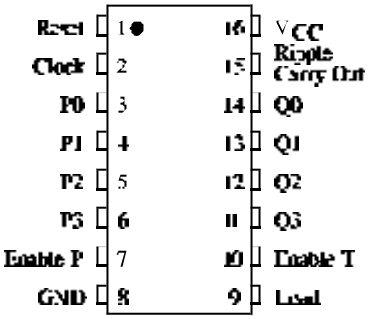
N SUFFIX
PLASTIC

D SUFFIX
SOIC

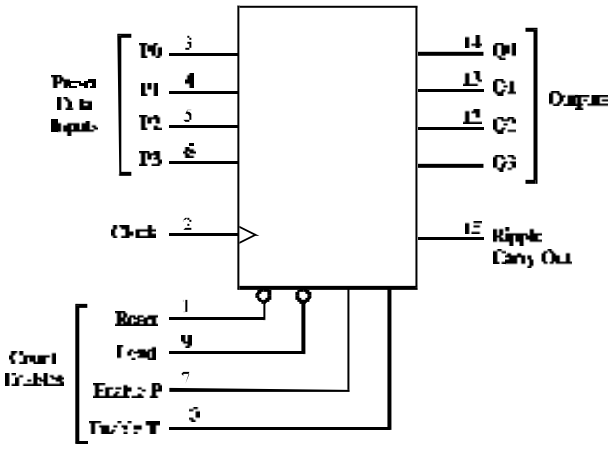
ORDERING INFORMATION

SL74LS161N Plastic
SL74LS161D SOIC
T_A = 0° to 70° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs					Outputs				Function
Reset	Load	Enable P	Enable T	Clock	Q0	Q1	Q2	Q3	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X	↑	P0	P1	P2	P3	Preset Data
H	H	X	L	↑	No change				No count
H	H	L	X	↑	No change				No count
H	H	H	H	↑	Count up				Count
H	X	X	X	↓	No change				No count

X=don' t care
P0,P1,P2,P3 = logic level of Data inputs
Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	7.0	V
V_{OUT}	Output Voltage	5.5	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	High Level Input Voltage		2.0		V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			-0.4	mA
I_{OL}	Low Level Output Current			8.0	mA
f_{clock}	Clock frequency		0	25	MHz
$t_{w(clock)}$	Width of clock pulse		25		ns
$t_{w(reset)}$	Width of reset pulse		20		ns
t_{su}	Setup time	Data inputs P0, P1, P2, P3	20		ns
		Enable P or T	20		
		Load	20		
t_h	Hold time at any input		3		ns
T_A	Ambient Temperature Range		0	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter		Test Conditions		Guaranteed Limit Min	Guaranteed Limit Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = min, I_{IN} = -18 mA			-1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = min, I_{OH} = -0.4 mA		2.7		V
V_{OL}	Low Level Output Voltage		V_{CC} = min, I_{OL} = 4 mA			0.4	V
			V_{CC} = min, I_{OL} = 8 mA			0.5	
I_{IH}	High Level Input Current		V_{CC} = max, V_{IN} =2.7 V	Data or enable P		20	µA
				Load, clock or enable T		40	
				Reset		20	
			V_{CC} = max, V_{IN} =7.0 V	Data or enable P		0.1	mA
				Load, clock or enable T		0.2	
				Reset		0.1	
I_{IL}	Low Level Input Current		V_{CC} = max, V_{IN} =0.4 V	Data or enable P		-0.4	mA
				Load, clock or enable T Reset		-0.8	
I_O	Output Short Circuit Current		V_{CC} = max, V_O = 0 V (Note 1)		-20	-100	mA
I_{CC}	Supply Current	All outputs high	V_{CC} = max (Note 2)			31	mA
		All outputs low	V_{CC} = max (Note 3)			32	

Note 1: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 2: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 3: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2 kΩ, t_r =15 ns, t_f = 6.0 ns)

Symbol	Parameter	Min	Max	Unit
t_{PLH}	Propagation Delay, Clock to Ripple carry		35	ns
t_{PHL}	Propagation Delay, Clock to Ripple carry		35	ns
t_{PLH}	Propagation Delay, Clock (load input high) to Any Q		24	ns
t_{PHL}	Propagation Delay, Clock (load input high) to Any Q		27	ns
t_{PLH}	Propagation Delay, Clock (load input low) to Any Q		24	ns
t_{PHL}	Propagation Delay, Clock (load input low) to Any Q		27	ns
t_{PLH}	Propagation Delay, Enable T to Ripple carry		14	ns
t_{PHL}	Propagation Delay, Enable T to Ripple carry		14	ns
t_{PHL}	Propagation Delay, Reset to Any Q		28	ns

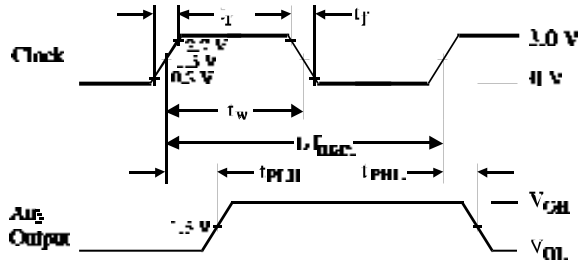


Figure 1. Switching Waveform

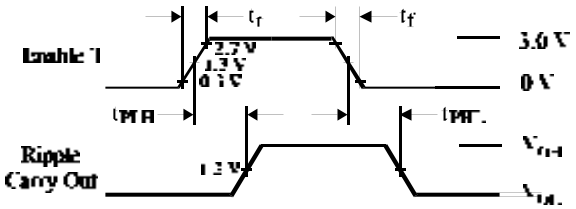


Figure 2. Switching Waveform

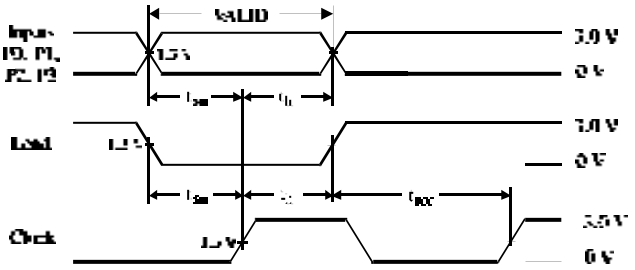


Figure 3. Switching Waveform

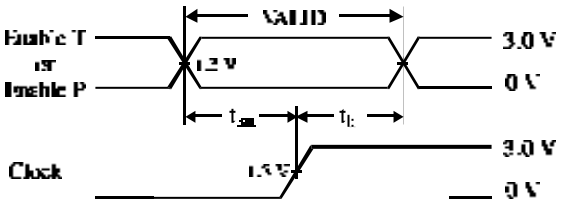
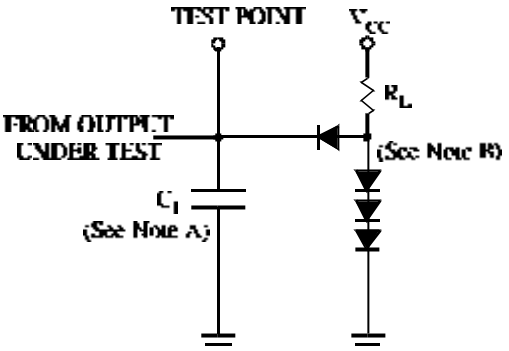
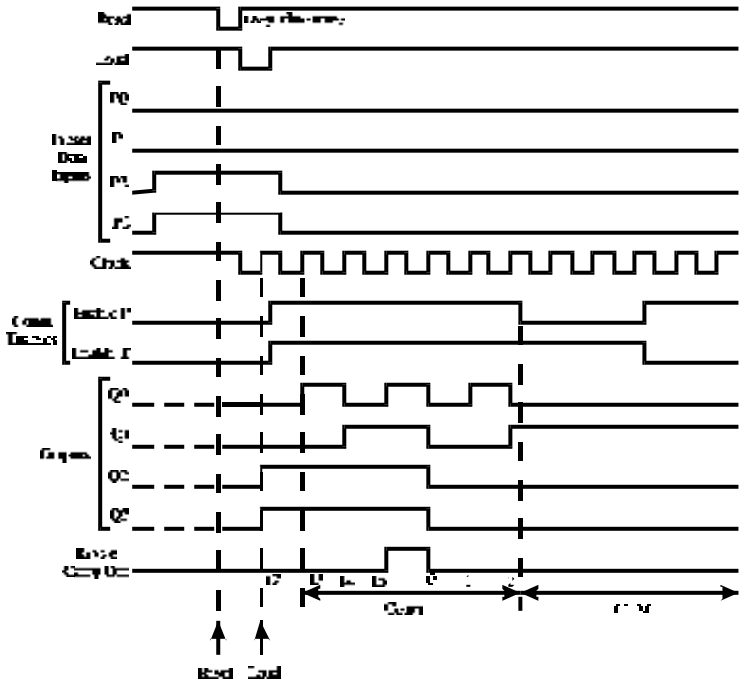


Figure 4. Switching Waveform



NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 5. Test Circuit



Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Figure 7. Timing Diagram