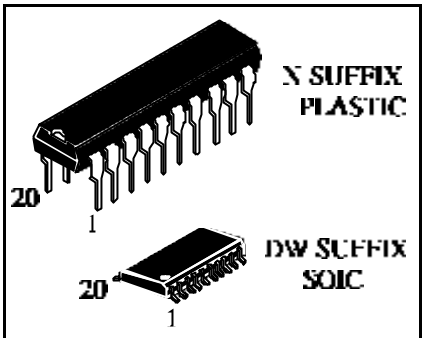
Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

These octal buffers and line drivers and designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and busoriented receivers and transmitters.

This devise features high fan-out, improved fan-in, and 400 mV noise margin.

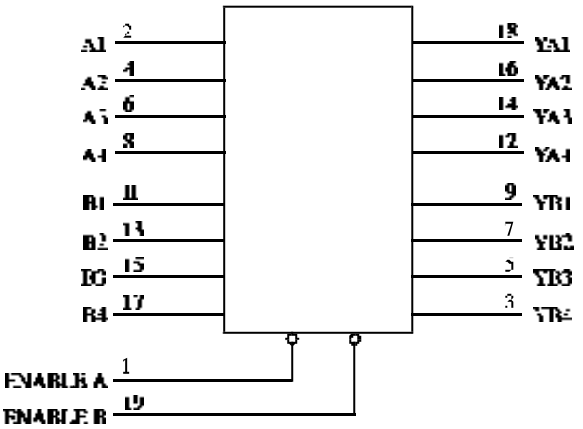
It can be used to drive terminated lines down to 133 ohms.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins



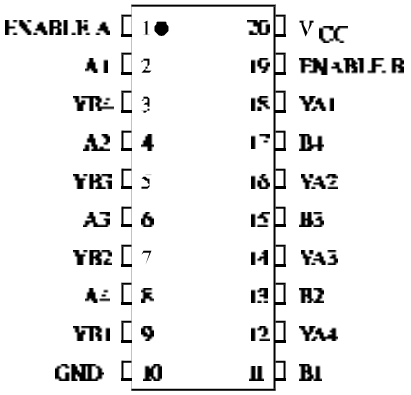
ORDERING INFORMATION
SL74LS244N Plastic
SL74LS244D SOIC
T_A = 0° to 70° C
for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A,B	YA,YB
L	L	L
L	H	H
H	X	Z

X=don' t care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	7.0	V
V_{OUT}	Output Voltage	5.5	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	High Level Input Voltage	2.0		V
V_{IL}	Low Level Input Voltage		0.8	V
I_{OH}	High Level Output Current		-15	mA
I_{OL}	Low Level Output Current		24	mA
T_A	Ambient Temperature Range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter		Test Conditions	Guaranteed Limit		Unit
				Min	Max	
V_{IK}	Input Clamp Voltage		V_{CC} = min, I_{IN} = -18 mA		-1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = min, I_{OH} = -1.0 mA	2.7		V
			V_{CC} = min, I_{OH} = -3.0 mA	2.4		
			V_{CC} = min, I_{OH} = -15 mA	2.0		
V_{OL}	Low Level Output Voltage		V_{CC} = min, I_{OL} = 12 mA		0.4	V
			V_{CC} = min, I_{OL} = 24 mA		0.5	
$V_{T+} - V_{T-}$	Hysteresis		V_{CC} = min	0.2		V
I_{OZH}	Output Off Current HIGH		V_{CC} = max, V_{OUT} = 2.7 V		20	µA
I_{OZL}	Output Off Current LOW		V_{CC} = max, V_{OUT} = 0.4 V		-20	µA
I_{IH}	High Level Input Current		V_{CC} = max, V_{IN} = 2.7 V		20	µA
			V_{CC} = max, V_{IN} = 7.0 V		0.1	mA
I_{IL}	Low Level Input Current		V_{CC} = max, V_{IN} = 0.4 V		-0.2	mA
I_O	Output Short Circuit Current		V_{CC} = max, V_O =0 V (Note 1)	-40	-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = max		27	mA
		Outputs Low	Outputs open		46	
		All outputs disabled			54	

note 1: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, t_r = 15 ns, t_f = 6.0 ns)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{PLH}	Propagation Delay, Data to Output	C_L = 45 pF, R_L = 667 Ω		18	ns
t_{PHL}	Propagation Delay, Data to Output			18	ns
t_{PZH}	Output Enable Time			23	ns
t_{PZL}	Output Enable Time			30	ns
t_{PHZ}	Output Disable Time	C_L = 5 pF		18	ns
t_{PLZ}	Output Disable Time	R_L = 667 Ω		25	ns

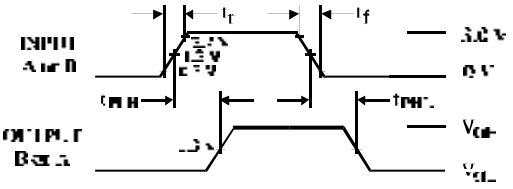
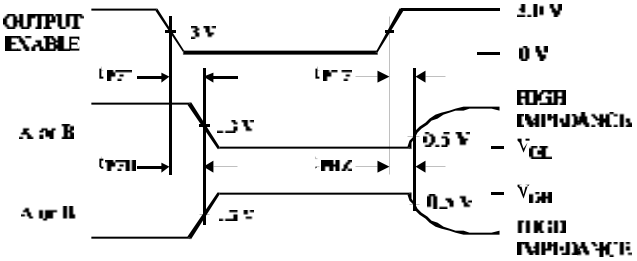
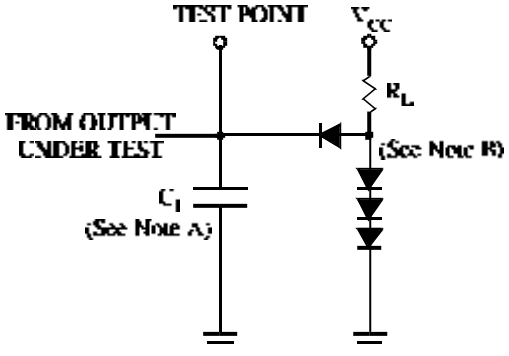


Figure 1. Switching Waveforms
(See Figure 3)



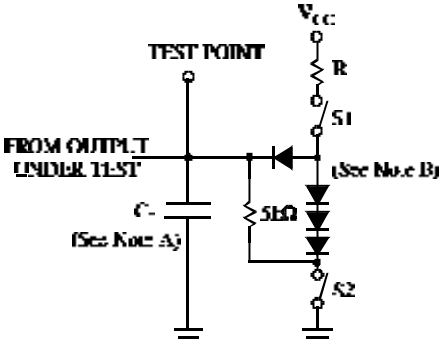
t_{PZL} - S1 closed, S2 opened
t_{PZH}- S1 opened, S2 closed
t_{PLZ}, t_{PHZ} - S1 and S2 closed

Figure 2. Switching Waveforms
(See Figure 4)



NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 3. Test Circuit



NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM