

Pre-settable Up/Down Counter

High-Voltage Silicon-Gate CMOS

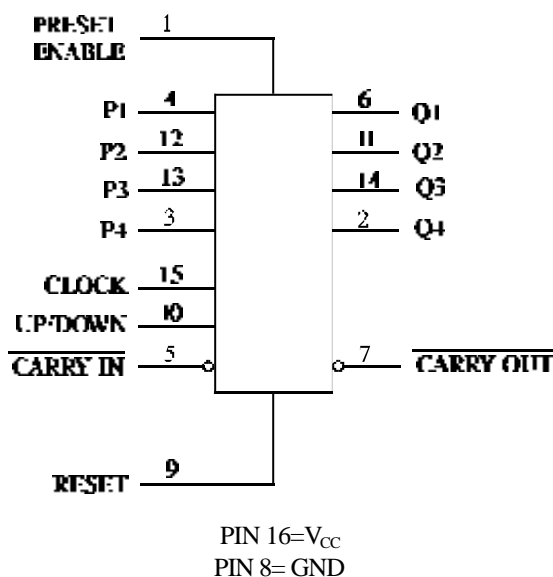
The SL4516B Pre-settable Binary Up/Down Counter consists of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. This counter can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The SL4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

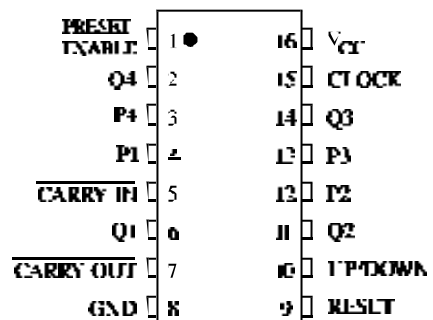
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

LOGIC DIAGRAM



ORDERING INFORMATION
 SL4516BN Plastic
 SL4516BD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs
CL	\overline{CI}	U/D	PE	R	Mode
X	H	X	L	L	NO COUNT
	L	H	L	L	COUNT UP
	L	L	L	L	COUNT DOWN
X	X	X	H	L	PRESET
X	X	X	X	H	RESET

X = don't care

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V V _{OUT} = 1.0 V or V _{CC} - 1.0 V V _{OUT} = 1.5 V or V _{CC} - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V V _{OUT} = 1.0 V or V _{CC} - 1.0 V V _{OUT} = 1.5 V or V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

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AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0	400	400	800	ns
		10	200	200	400	
		15	150	150	300	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Preset or Reset to Q (Figure 1)	5.0	420	420	840	ns
		10	210	210	420	
		15	160	160	320	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Clock to Carry Out (Figure 1)	5.0	480	480	960	ns
		10	240	240	480	
		15	180	180	360	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Carry In to Carry Out (Figure 1)	5.0	250	250	500	ns
		10	120	120	240	
		15	100	100	200	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Preset or Reset to Carry Out (Figure 1)	5.0	640	640	1280	ns
		10	320	320	640	
		15	250	250	500	
t_{THL} , t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_{su}	Minimum Setup Time, P to Preset Enable (Figure 1)	5.0	25	25	50	ns
		10	10	10	20	
		15	10	10	20	
t_{su}	Minimum Setup Time, Up/Down to Clock (Figure 1)	5.0				ns
		10				
		15				
t_{su}	Minimum Setup Time, Carry In to Clock (Figure 1)	5.0				ns
		10				
		15				
t_h	Minimum Hold Time, Clock to Carry In (Figure 1)	5.0	60	60	120	ns
		10	30	30	60	
		15	30	30	60	
t_h	Minimum Hold Time, Clock to Up/Down (Figure 1)	5.0	30	30	60	ns
		10	30	30	60	
		15	30	30	60	
t_h	Minimum Hold Time, Preset enable to P (Figure 1)	5.0	70	70	140	ns
		10	40	40	80	

		15	40	40	80	
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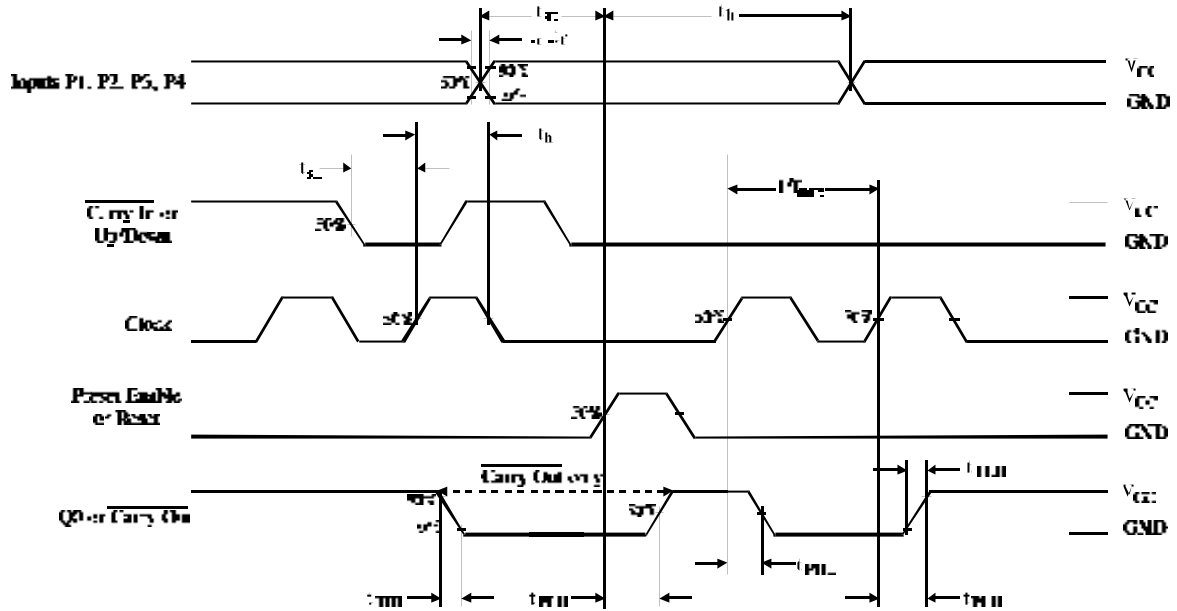
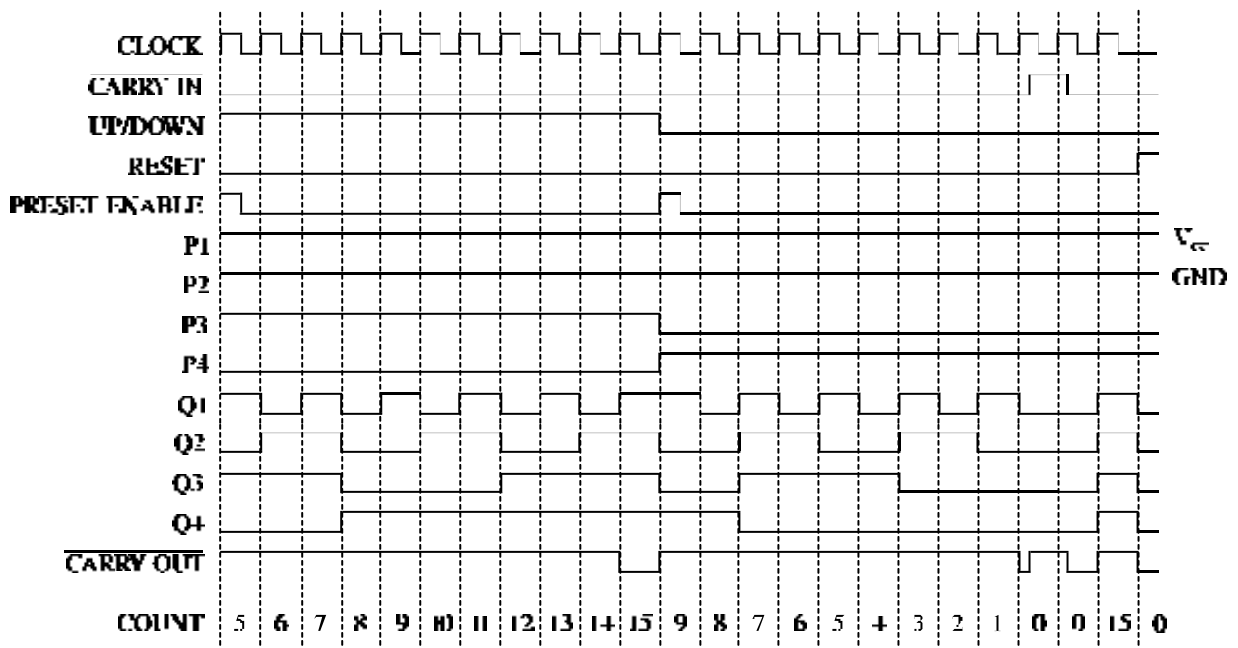


Figure 1. Switching Waveforms

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM

