SIEMENS

2M x 32-Bit Dynamic RAM Module — HYM 322030S/GS-60/-70

Advanced Information

- 2 097 152 words by 32-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 3300 mW active (-60 version)
  max. 3025 mW active (-70 version)
  CMOS – 22 mW standby
  TTL – 44 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 4 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-9) with 20.32 mm (800 mil) height
- Utilizes four 2M × 8 - DRAMs in 400 mil SOJ-packages
- 2048 refresh cycles / 32 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 322030S-60	Q67100-Q976	L-SIM-72-9	DRAM Module (access time 60 ns)
HYM 322030S-70	Q67100-Q977	L-SIM-72-9	DRAM Module (access time 70 ns)
HYM 322030GS-60	Q67100-Q2018	L-SIM-72-9	DRAM Module (access time 60 ns)
HYM 322030GS-70	Q67100-Q2019	L-SIM-72-9	DRAM Module (access time 70 ns)

The HYM 322030S/GS-60/-70 is a 8 M Byte DRAM module organized as 2 097 152 words by 32-bit in a 72-pin single-in-line package comprising four HYB 5117800BSJ 2M × 8 DRAMs in 400 mil wide SOJ-packages mounted together with four 0.2 µF ceramic decoupling capacitors on a PC board.

Each HYB 5117800BSJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 322030S/GS-60/-70 dictates the use of early write cycles.

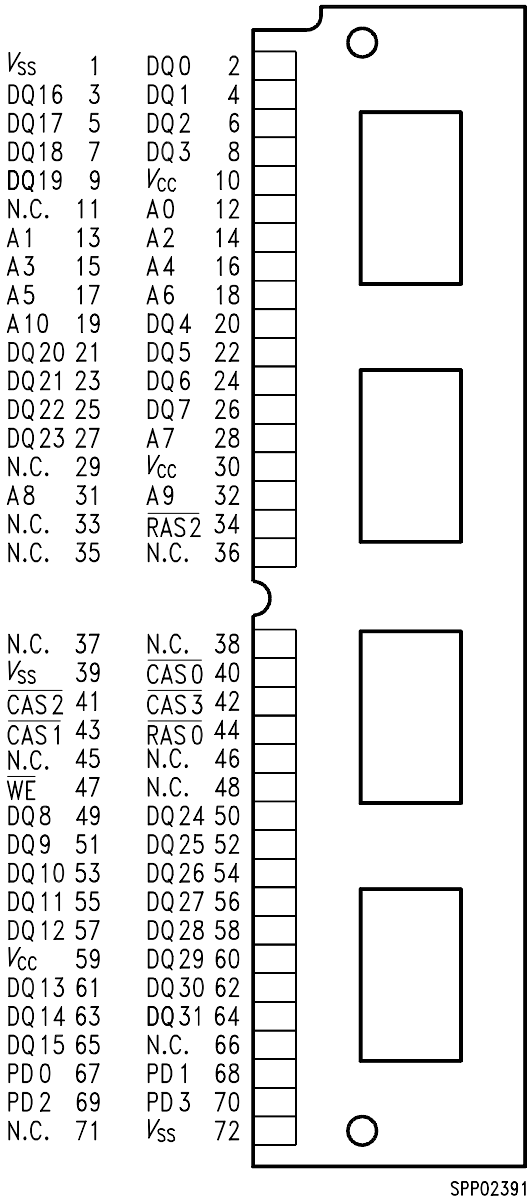
Pin Definitions and Functions

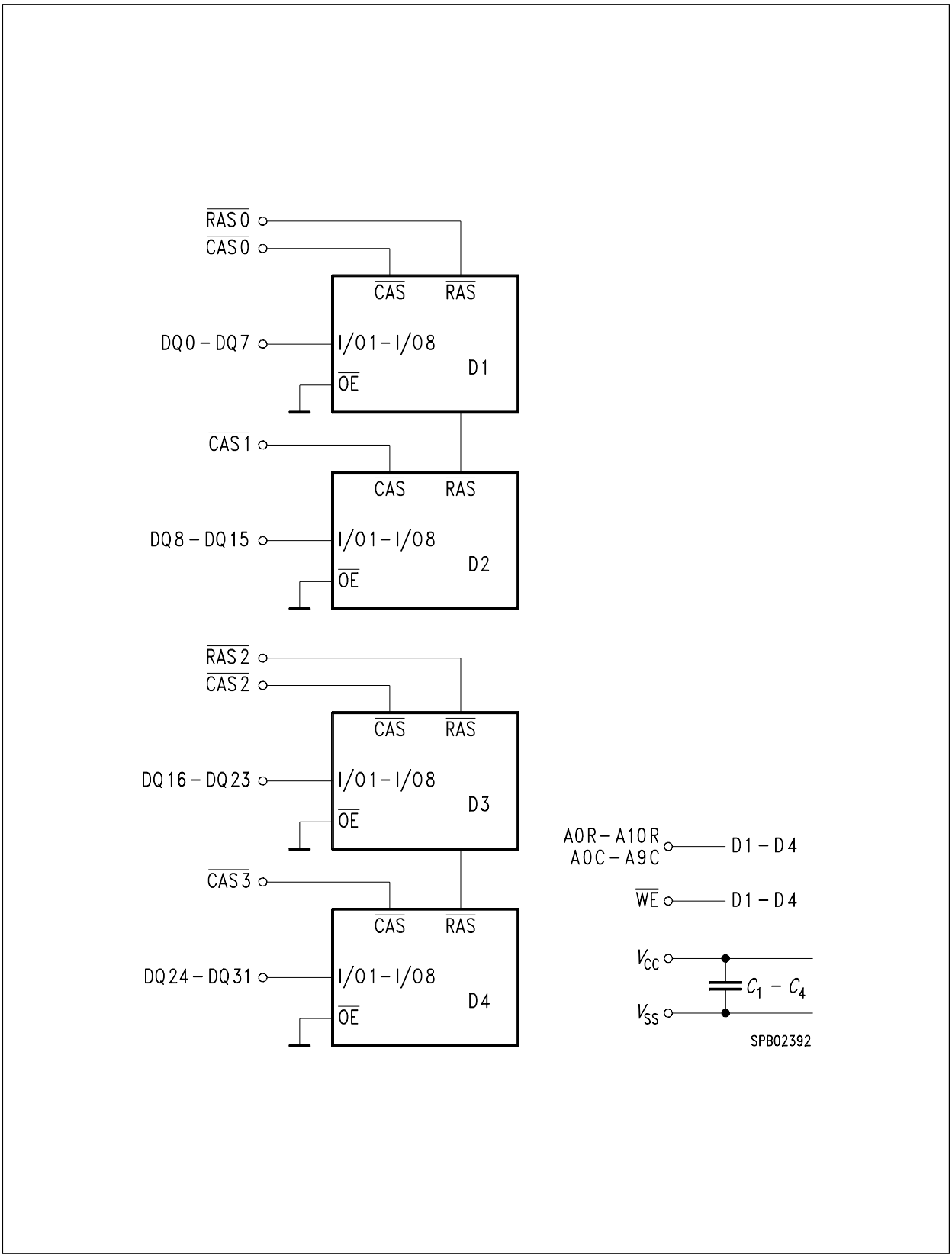
Pin No.	Function
A0R-A10R	Row Address Inputs
A0C-A9C	Column Address Inputs
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 ˚C
Storage temperature range..... – 55 to 125 ˚C
Soldering temperature ..... 260 ˚C
Soldering time..... 10 s
Input/output voltage ..... – 0.5 V to min (V_{CC} + 0.5, 7.0) V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 4.2 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]
T_A = 0 to 70 ˚C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	
Input low voltage	V_{IL}	– 0.5	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min)	I_{CC1}				
-60 version		–	550	mA	2)
-70 version		–	500	mA	3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	8	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	I_{CC3}				
-60 version		–	550	mA	2)
-70 version		–	500	mA	

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	550	mA	[2]
-70 version		–	500	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	4	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	600	mA	[2]
-70 version		–	550	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	40	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	45	pF
Input capacitance ($\overline{WE}$)	C_{I4}	–	45	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	25	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 ˚C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 322030S/GS-60		HYM 322030S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 ˚C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 322030S/GS-60		HYM 322030S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

12) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycles only.