

## 256 K × 4-Bit Dynamic RAM Low Power 256 K × 4-Bit Dynamic RAM

## HYB 514256B/BJ-50/-60/-70 HYB 514256BL/BJL-50/-60/-70

### Advanced Information

- 262 144 words by 4-bit organization
- Fast access and cycle time  
50 ns access time  
95 ns cycle time (-50 version)  
60 ns access time  
110 ns cycle time (-60 version)  
70 ns access time  
130 ns cycle time (-70 version)
- Fast page mode cycle time  
35 ns (-50 version)  
40 ns (-60 version)  
45 ns (-70 version)
- Low power dissipation  
max. 495 mW active (-50 version)  
max. 440 mW active (-60 version)  
max. 385 mW active (-70 version)  
max. 5.5 mW standby  
max. 1.1 mW standby for L-version
- Single + 5 V ( $\pm 10\%$ ) supply with a built-in  $V_{BB}$  generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-modify-write,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, hidden-refresh and fast page mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms  
512 refresh cycles/64 ms for L-version only
- Plastic Packages: P-DIP-20-2,  
P-SOJ-26/20-1

### Ordering Information

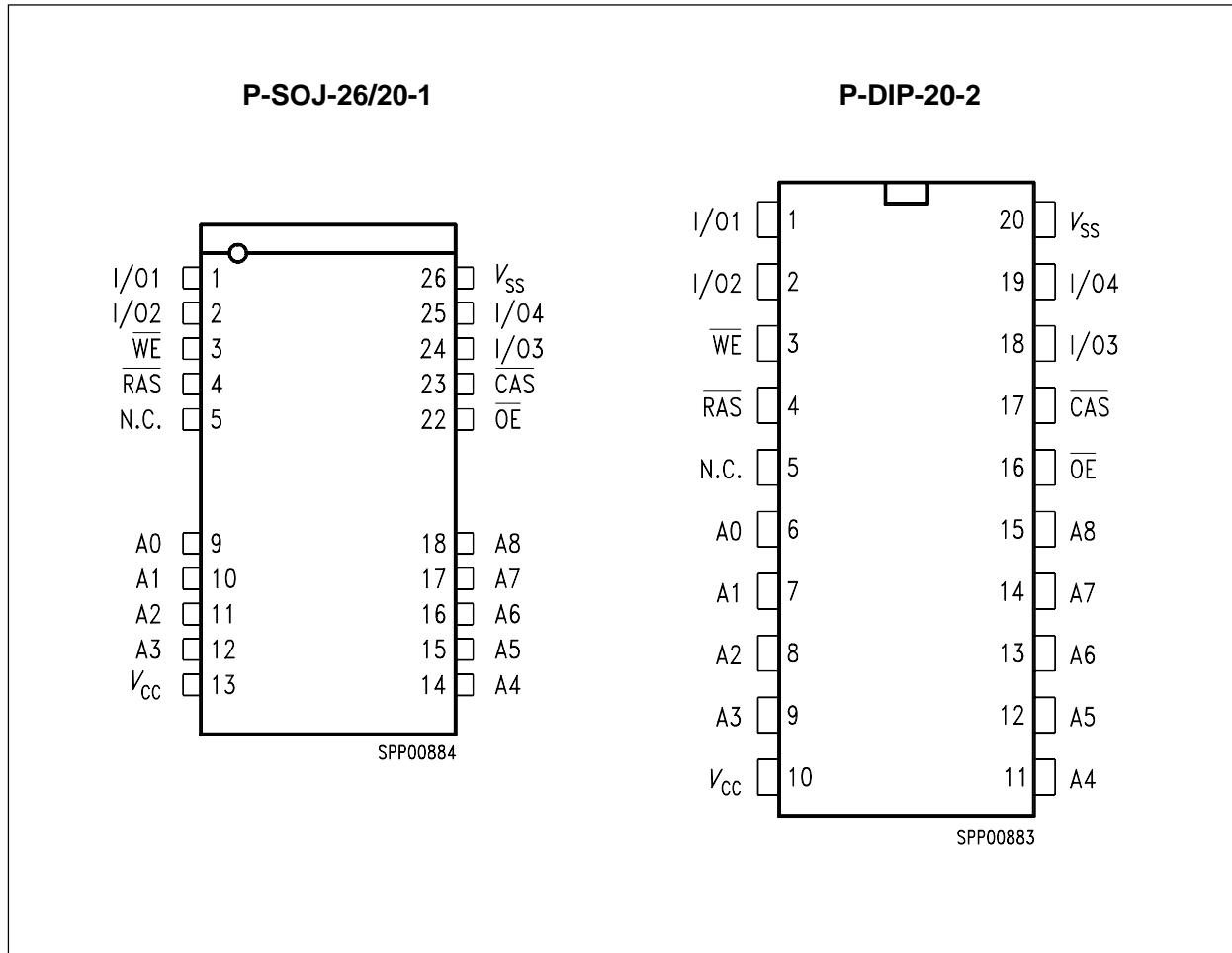
Type	Ordering Code	Package	Description
HYB 514256B-50	Q67100-Q1044	P-DIP-20-2	DRAM (access time 50ns)
HYB 514256B-60	Q67100-Q530	P-DIP-20-2	DRAM (access time 60 ns)
HYB 514256B-70	Q67100-Q433	P-DIP-20-2	DRAM (access time 70 ns)
HYB 514256BJ-50	Q67100-Q1054	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 514256BJ-60	Q67100-Q536	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 514256BJ-70	Q67100-Q537	P-SOJ-26/20-1	DRAM (access time 70 ns)
HYB 514256BL-50	on request	P-DIP-20-2	DRAM (access time 50 ns)
HYB 514256BL-60	Q67100-Q542	P-DIP-20-2	DRAM (access time 60 ns)
HYB 514256BL-70	Q67100-Q543	P-DIP-20-2	DRAM (access time 70 ns)
HYB 514256BJL-50	on request	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 514256BJL-60	Q67100-Q608	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 514256BJL-70	Q67100-Q607	P-SOJ-26/20-1	DRAM (access time 70 ns)

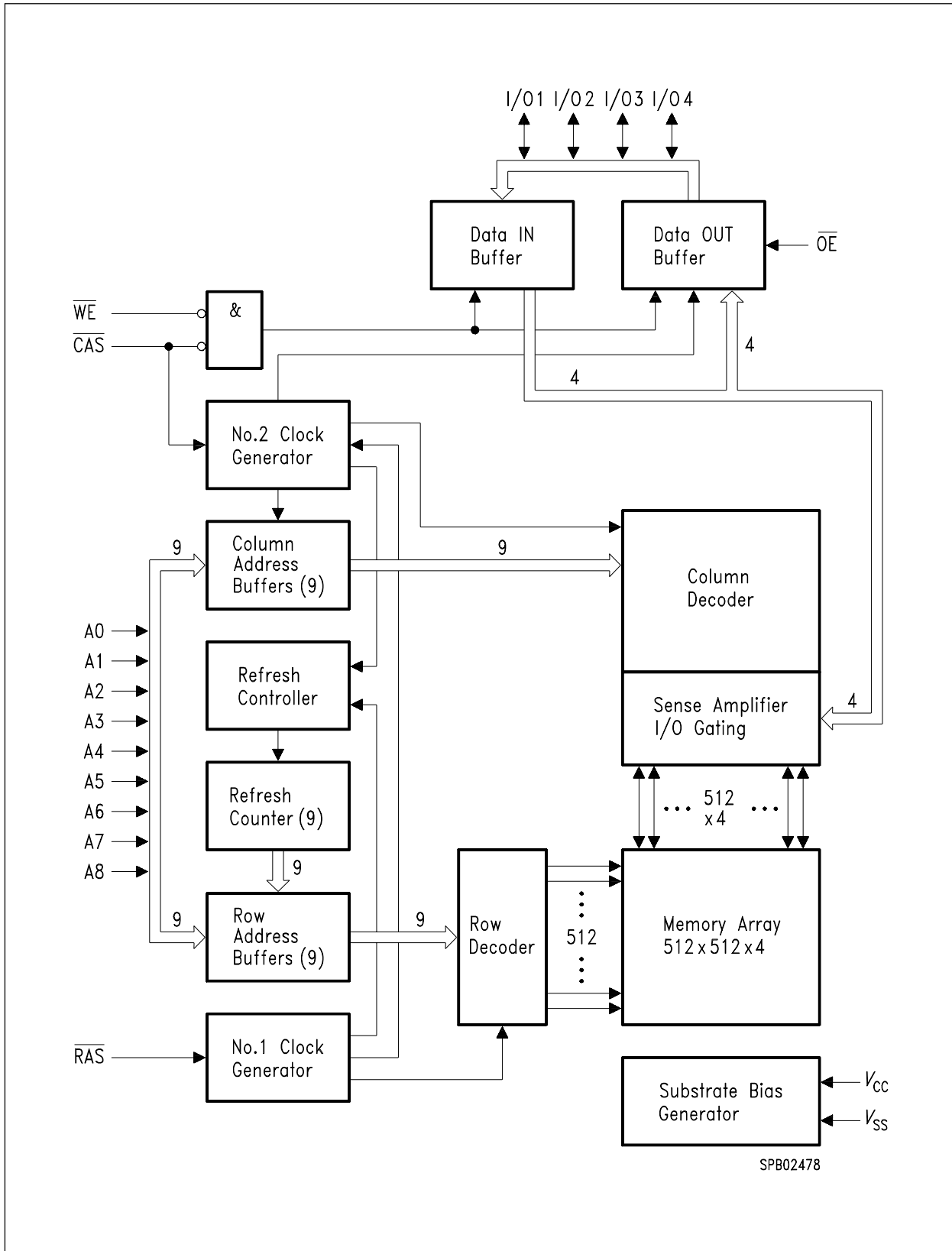
The HYB 514256B/BJ/BL/BJL is the new generation dynamic RAM organized as 262 144 words by 4-bit. The HYB 514256B/BJ/BL/BJL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256B/BJ/BL/BJL to be packaged in a standard plastic P-DIP-20-2, or plastic P-SOJ-26/20-1. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V ( $\pm 10\%$ ) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. These HYB 514256BL/BJL are specially selected for battery backup applications.

### Pin Definitions and Functions

Pin No.	Function
A0-A8	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$V_{\text{CC}}$	Power Supply (+ 5 V)
$V_{\text{SS}}$	Ground (0 V)
N.C.	No Connection

### Pin Configuration (top view)





Block Diagram

### Absolute Maximum Ratings

Operating temperature range .....	0 to + 70 °C
Storage temperature range.....	- 55 to + 150 °C
Soldering temperature .....	260 °C
Soldering time .....	10 s
Input/output voltage .....	- 1 to + 7 V
Power supply voltage.....	- 1 to + 7 V
Power dissipation.....	0.6 W
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 5$  V  $\pm$  10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.4	6.5	V	1)
Input low voltage	$V_{IL}$	- 1.0	0.8	V	1)
Output high voltage ( $I_{OUT} = - 5$ mA)	$V_{OH}$	2.4	-	V	1)
Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{OL}$	-	0.4	V	1)
Input leakage current, any input ( $0$ V $\leq V_{IN} \leq 6.5$ V, all other pins = 0 V)	$I_{I(L)}$	- 10	10	$\mu$ A	1)
Output leakage current (DO is disabled, $0$ V $\leq V_{OUT} \leq V_{CC}$ )	$I_{O(L)}$	- 10	10	$\mu$ A	1)
Average $V_{CC}$ supply current: -50 version -60 version -70 version ( $\overline{RAS}$ , $\overline{CAS}$ , address cycling: $t_{RC} = t_{RC}$ min.)	$I_{CC1}$	-	90 80 70	mA mA mA	2) 3) 2) 3) 2) 3)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$	-	2	mA	-
Average $V_{CC}$ supply current, $\overline{RAS}$ only mode: -50 version -60 version -70 version ( $\overline{RAS}$ cycling: $\overline{CAS} = V_{IH}$ ; $t_{RC} = t_{RC}$ min.)	$I_{CC3}$	-	90 80 70	mA mA mA	2) 2) 2)

### DC Characteristics (cont'd)

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 5$  V  $\pm$  10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current, fast page mode: -60 version -70 version -50 version ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: $t_{PC} = t_{PC}$ min.)	$I_{CC4}$	— — —	70 60 50	mA mA mA	2) 3) 2) 3) 2) 3)
Standby $V_{CC}$ supply current L-Version ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	$I_{CC5}$	— —	1 200	mA $\mu$ A	1) 1)
Average $V_{CC}$ supply current, $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode: -50 version -60 version -70 version ( $\overline{RAS}$ , $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ min.)	$I_{CC6}$	— — —	90 80 70	mA mA mA	2) 2) 2)
For L-version only: Battery backup current: average power supply current, battery backup mode: ( $\overline{CAS} = \overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{OE} = V_{CC} - 0.2$ V $\overline{WE} = V_{CC} - 0.2$ V or 0.2 V, $A0$ to $A8 = V_{CC} - 0.2$ V or 0.2 V, $I/O1$ to $I/O4 = V_{CC} - 0.2$ V or 0.2 V or open, $t_{RC} = 125$ $\mu$ s, $t_{RAS} = t_{RAS}$ min. $\sim$ 1 $\mu$ s)	$I_{CC7}$	—	300	$\mu$ A	2)

### AC Characteristics <sup>4) 13)</sup>

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  10 %;  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	$t_{RC}$	95	–	110	–	130	–	ns
Read-modify-write cycle time	$t_{RWC}$	140	–	160	–	185	–	ns
Fast page mode cycle time	$t_{PC}$	35	–	40	–	45	–	ns
Fast page mode read-modify-write cycle time	$t_{PRWC}$	80	–	90	–	100	–	ns
Access time from $\overline{RAS}$ <sup>6) 11)</sup>	$t_{RAC}$	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ <sup>6) 11)</sup>	$t_{CAC}$	–	15	–	15	–	20	ns
Access time from column address <sup>6) 12)</sup>	$t_{AA}$	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge <sup>6) 12)</sup>	$t_{CPA}$	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z <sup>4)</sup>	$t_{CLZ}$	0	–	0	–	0	–	ns
Output buffer turn-off delay <sup>7)</sup>	$t_{OFF}$	0	15	0	20	0	20	ns
Transition time (rise and fall) <sup>5)</sup>	$t_T$	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	$t_{RP}$	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10.000	60	10.000	70	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)	$t_{RASP}$	50	100.000	60	100.000	70	100.000	ns
$\overline{RAS}$ hold time	$t_{RSH}$	15	–	15	–	20	–	ns
$\overline{CAS}$ hold time	$t_{CSH}$	50	–	60	–	70	–	ns
$\overline{CAS}$ pulse width	$t_{CAS}$	15	10.000	15	10.000	20	10.000	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (Fast Page Mode)	$t_{RHCP}$	30	–	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM RMW)	$t_{CPWD}$	55	–	60	–	65	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time <sup>11)</sup>	$t_{RCD}$	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time <sup>12)</sup>	$t_{RAD}$	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	$t_{CP}$	10	–	10	–	10	–	ns

### AC Characteristics (cont'd) <sup>4) 13)</sup>

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  10 %;  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Row address setup time	$t_{ASR}$	0	–	0	–	0	–	ns
Row address hold time	$t_{RAH}$	10	–	10	–	10	–	ns
Column address setup time	$t_{ASC}$	0	–	0	–	0	–	ns
Column address hold time	$t_{CAH}$	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	35	–	ns
Read command setup time	$t_{RCS}$	0	–	0	–	0	–	ns
Read command hold time <sup>8)</sup>	$t_{RCH}$	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ <sup>8)</sup>	$t_{RRH}$	0	–	0	–	0	–	ns
Write command hold time	$t_{WCH}$	10	–	10	–	15	–	ns
Write command pulse width	$t_{WCP}$	10	–	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	15	–	15	–	20	–	ns
Data setup time <sup>9)</sup>	$t_{DS}$	0	–	0	–	0	–	ns
Data hold time <sup>9)</sup>	$t_{DH}$	10	–	15	–	15	–	ns
Refresh period	$t_{REF}$	–	8	–	8	–	8	ms
Refresh period L-version	$t_{REF}$	–	64	–	64	–	–	ms
Write command setup time <sup>10)</sup>	$t_{WCS}$	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time <sup>10)</sup>	$t_{CWD}$	40	–	45	–	50	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time <sup>10)</sup>	$t_{RWD}$	75	–	90	–	100	–	ns
Column address to $\overline{WE}$ delay time <sup>10)</sup>	$t_{AWD}$	50	–	60	–	65	–	ns
$\overline{CAS}$ setup time ( $\overline{CAS}$ -before- $\overline{RAS}$ cycle)	$t_{CSR}$	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time ( $\overline{CAS}$ -before- $\overline{RAS}$ cycle)	$t_{CHR}$	10	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	0	–	0	–	0	–	ns



### AC Characteristics (cont'd) <sup>4) 13)</sup>

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  10 %;  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
CAS precharge time ( $\overline{\text{CAS}}$ -before-RAS counter test cycle)	$t_{\text{CPT}}$	25	–	30	–	40	–	ns
$\overline{\text{OE}}$ access time	$t_{\text{OEA}}$	–	15	–	15	–	20	ns
RAS hold time referenced to $\overline{\text{OE}}$	$t_{\text{ROH}}$	10	–	10	–	10	–	ns
Output buffer turn-off delay time from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	15	0	20	0	20	ns
Data to $\overline{\text{CAS}}$ low delay <sup>14)</sup>	$t_{\text{DZC}}$	0	–	0	–	0	–	ns
$\overline{\text{CAS}}$ high to data delay <sup>15)</sup>	$t_{\text{DZO}}$	0	–	0	–	0	–	
$\overline{\text{OE}}$ high to data delay <sup>15)</sup>	$t_{\text{CDD}}$	15	–	20	–	20	–	ns
$\overline{\text{OE}}$ to data delay <sup>15)</sup>	$t_{\text{ODD}}$	15	–	20	–	20	–	ns

### Capacitance

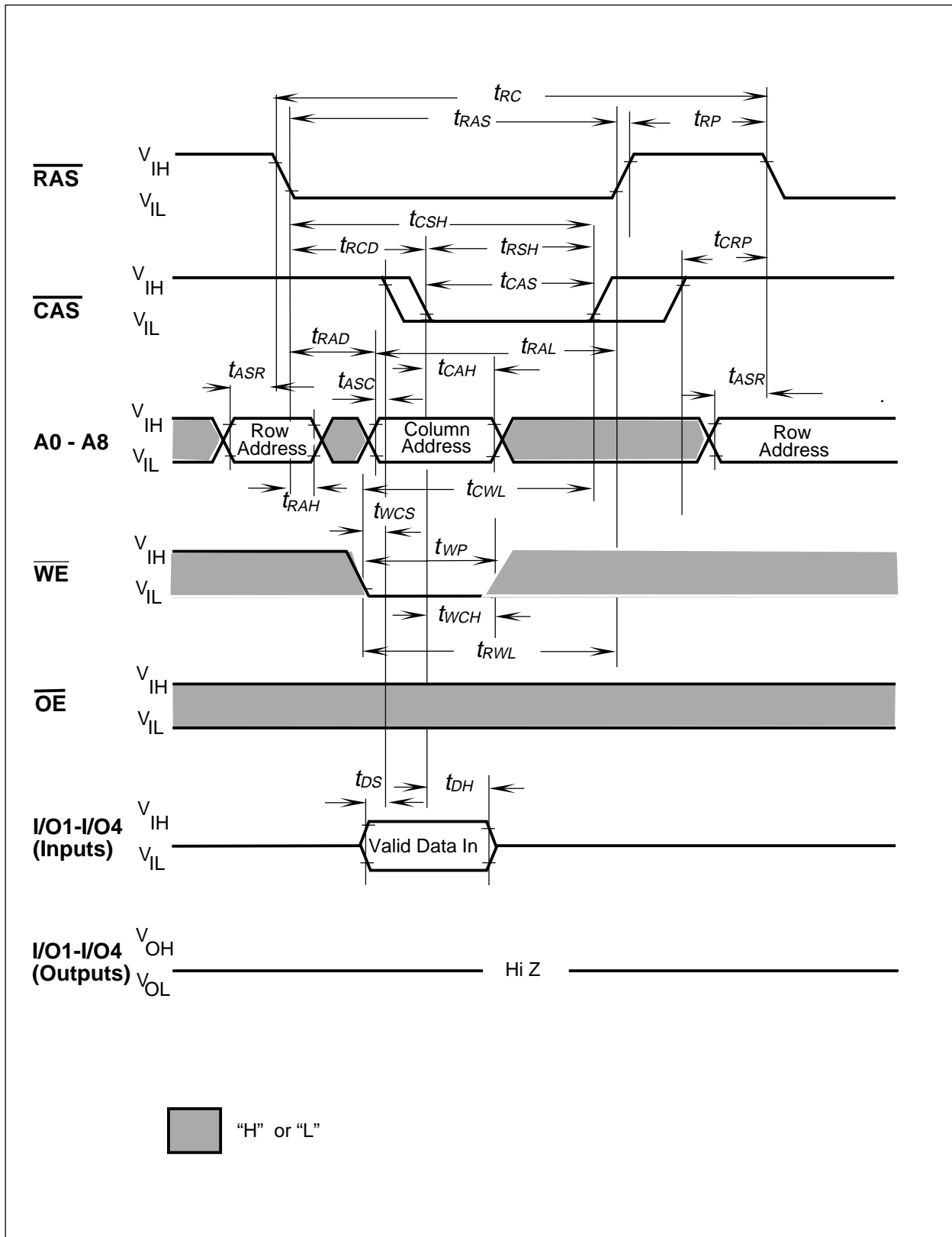
$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  10 %;  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	$C_{11}$	–	5	pF
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{12}$	–	7	pF
Output capacitance (I/O1 ... I/O4)	$C_{50}$	–	7	pF

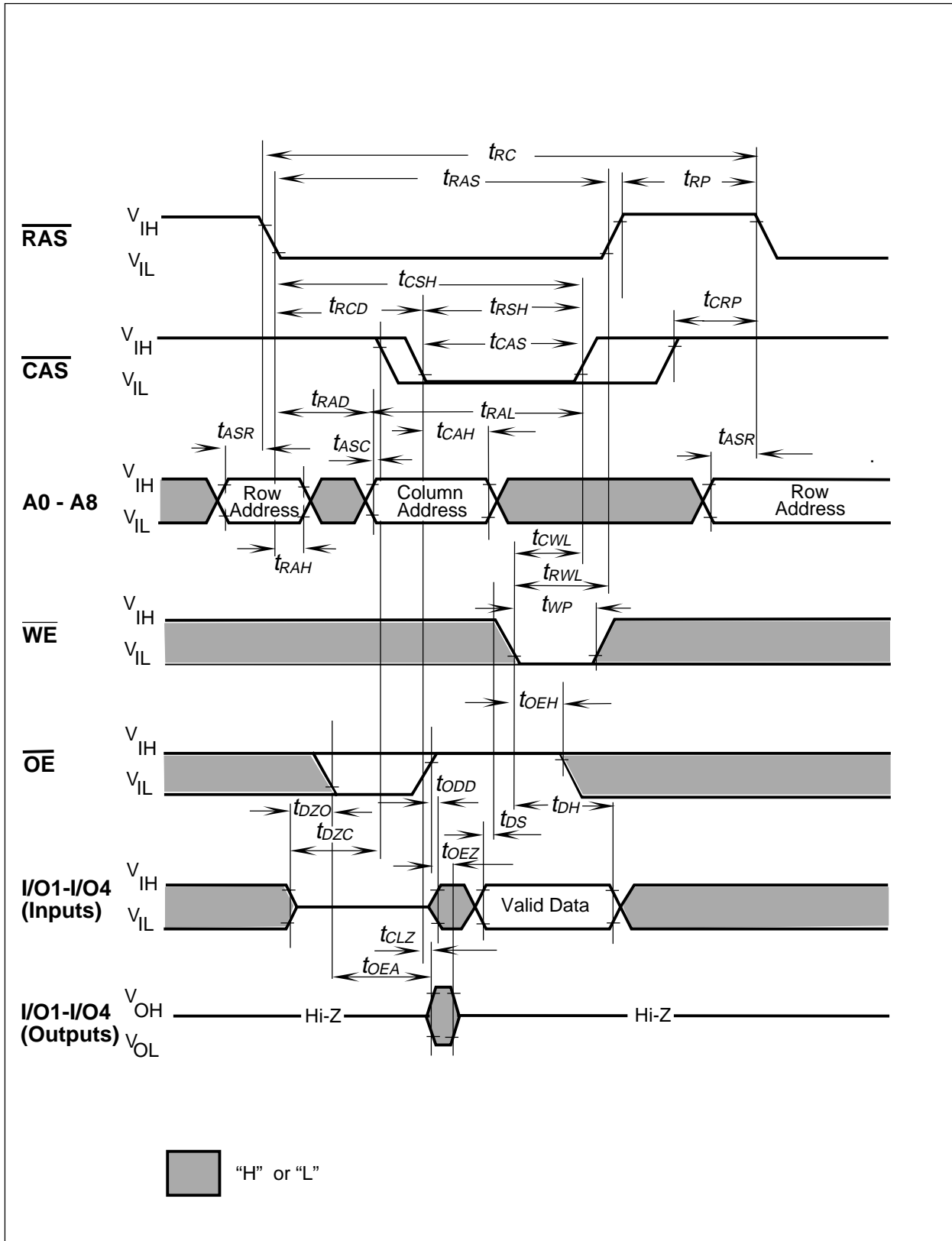
**Notes :**

- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  and  $I_{CC7}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are measured with the output open.
- 4) An initial pause of 200  $\mu$ s is required after power-up followed by 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
- 5)  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 6) Measured with a load equivalent to 2 TTL loads and 100 pF.
- 7)  $t_{OFF}$  (max.) and  $t_{OEZ}$  (max.) define the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
- 8) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 9) These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles and to the  $\overline{\text{WE}}$  leading edge in read-modify-write cycles.
- 10)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-modify-write cycle and I/O will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 11) Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met,  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
- 12) Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
- 13) AC measurements assume  $t_T = 5\text{ns}$ .
- 14) Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
- 15) Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.





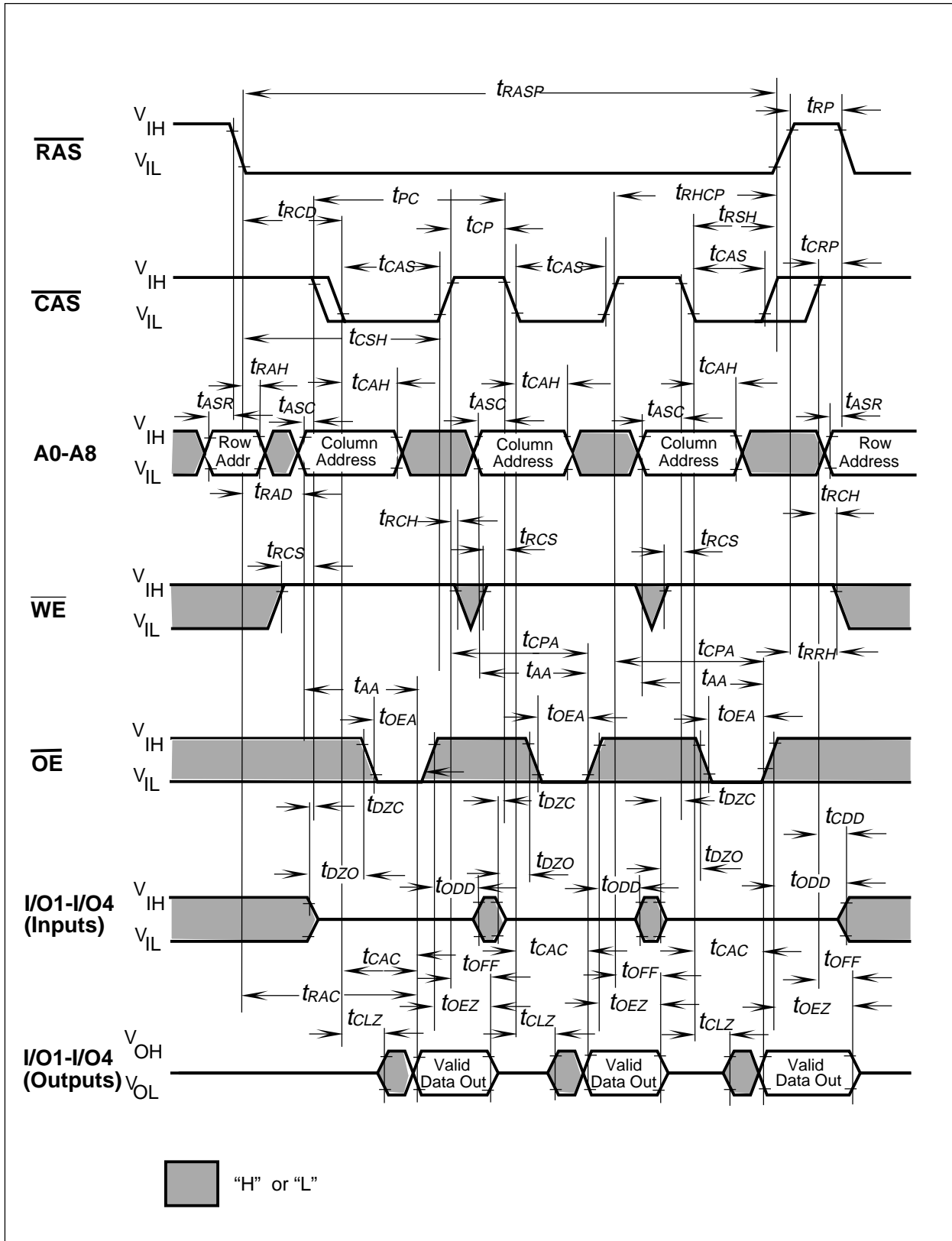
Write Cycle (Early Write)



Write Cycle ( $\overline{OE}$  Controlled Write)

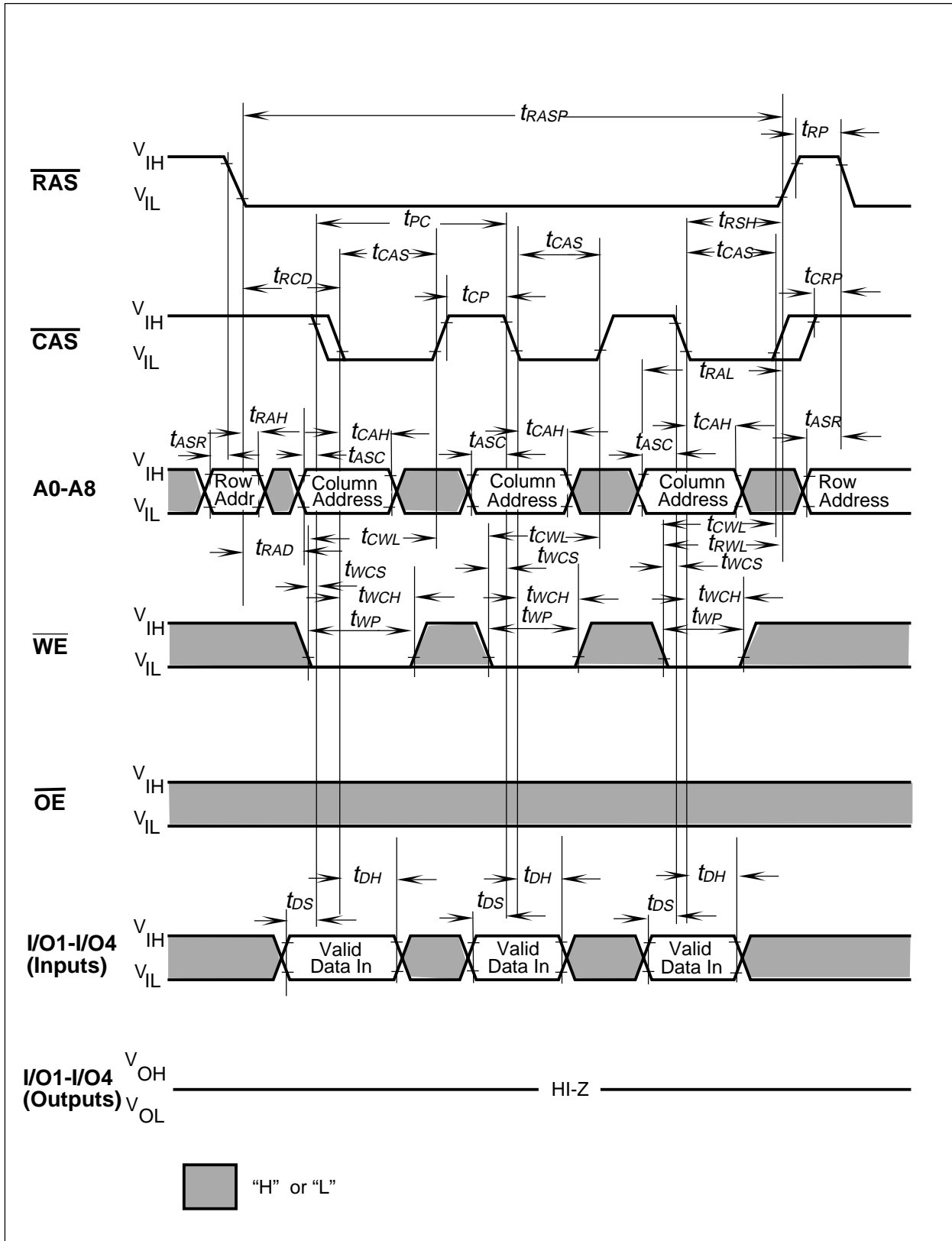




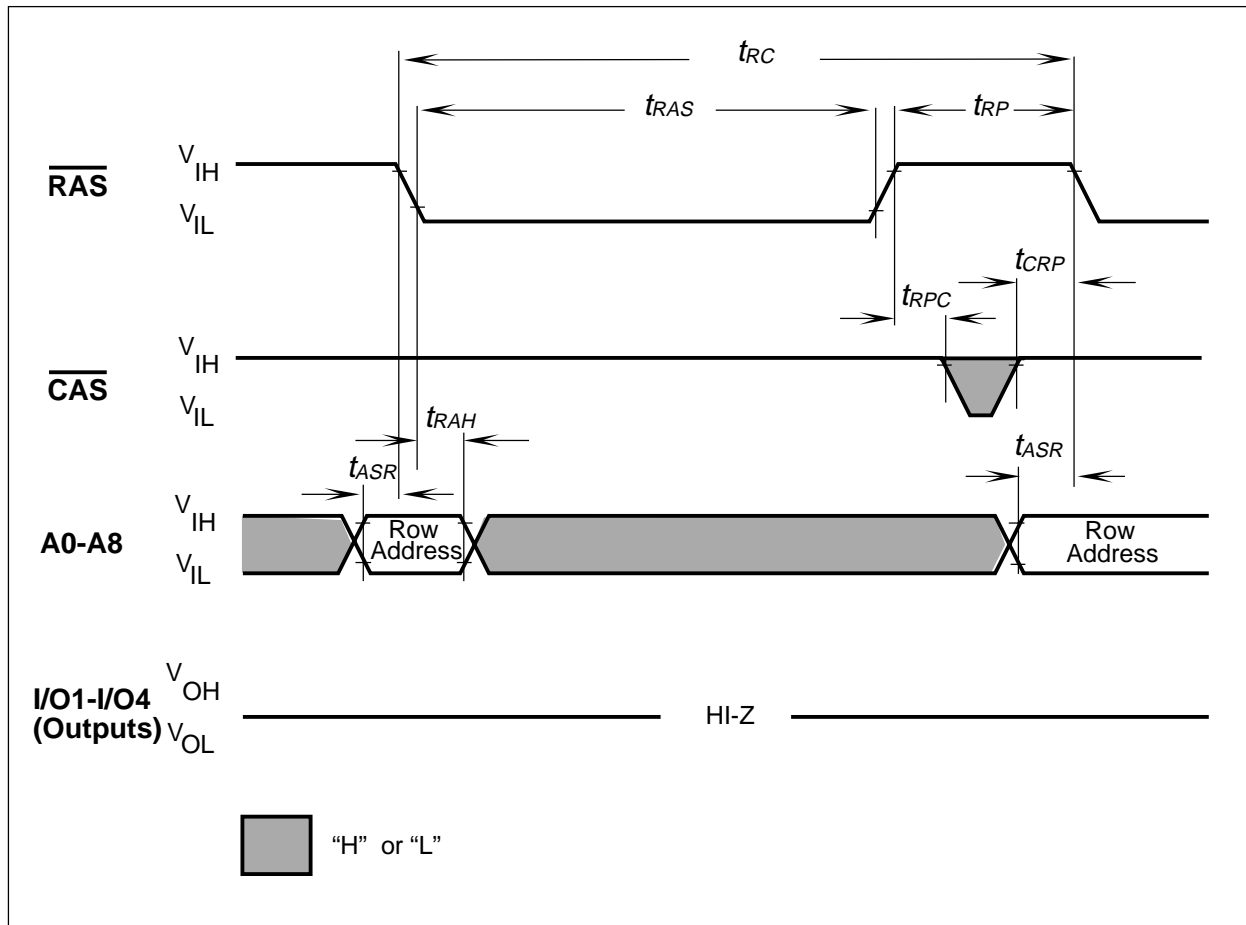


Fast Page Mode Read Cycle

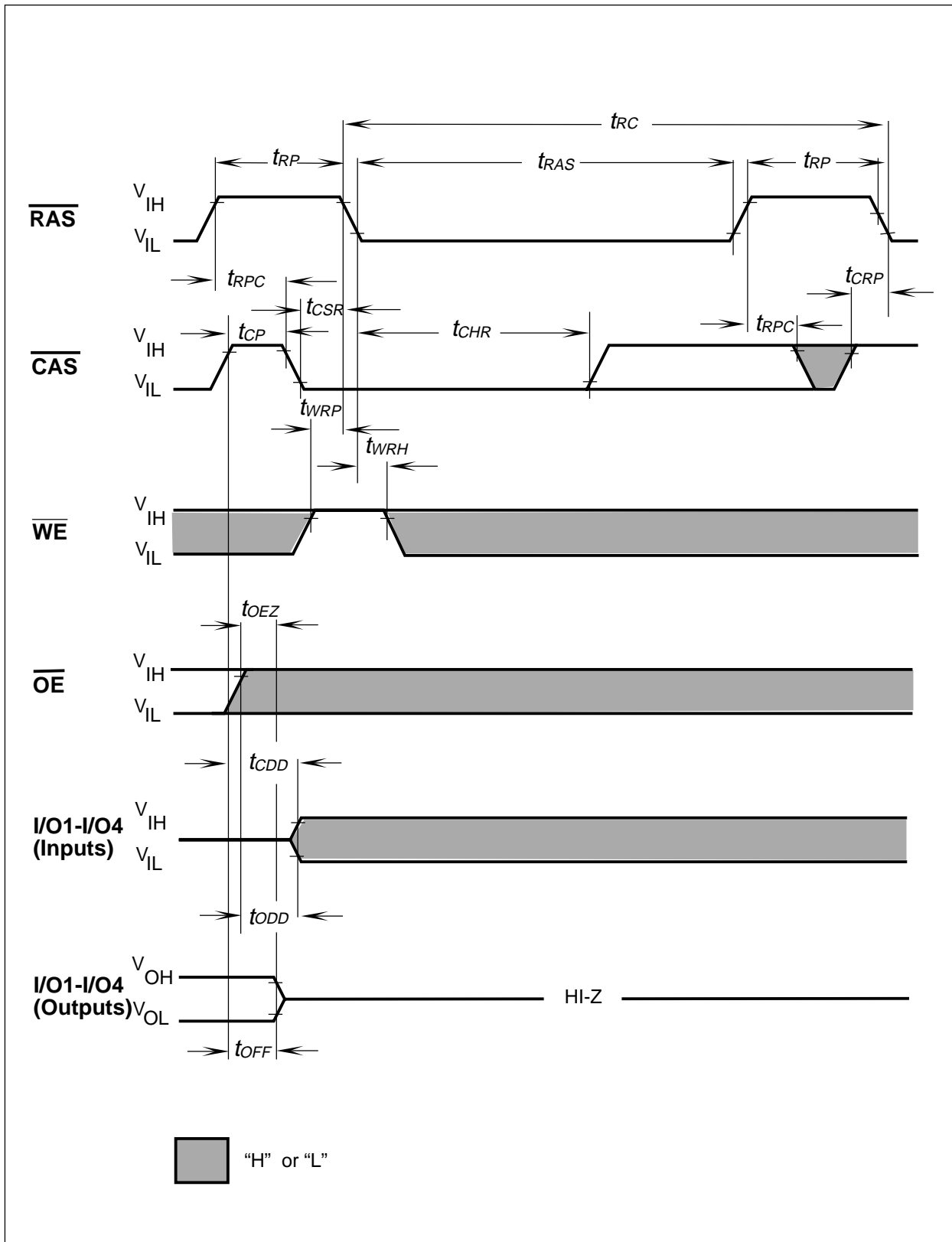




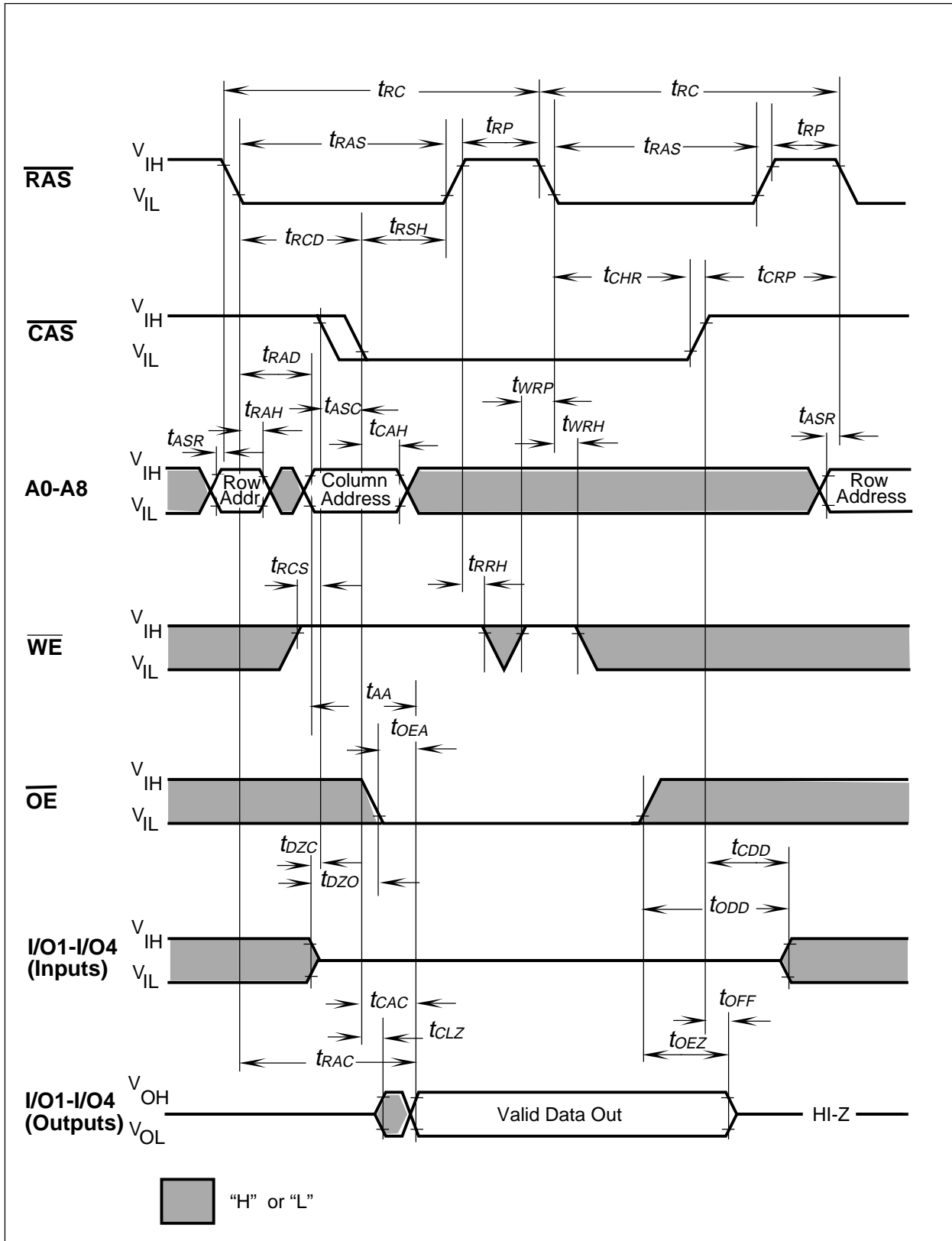
Fast Page Mode Early Write Cycle



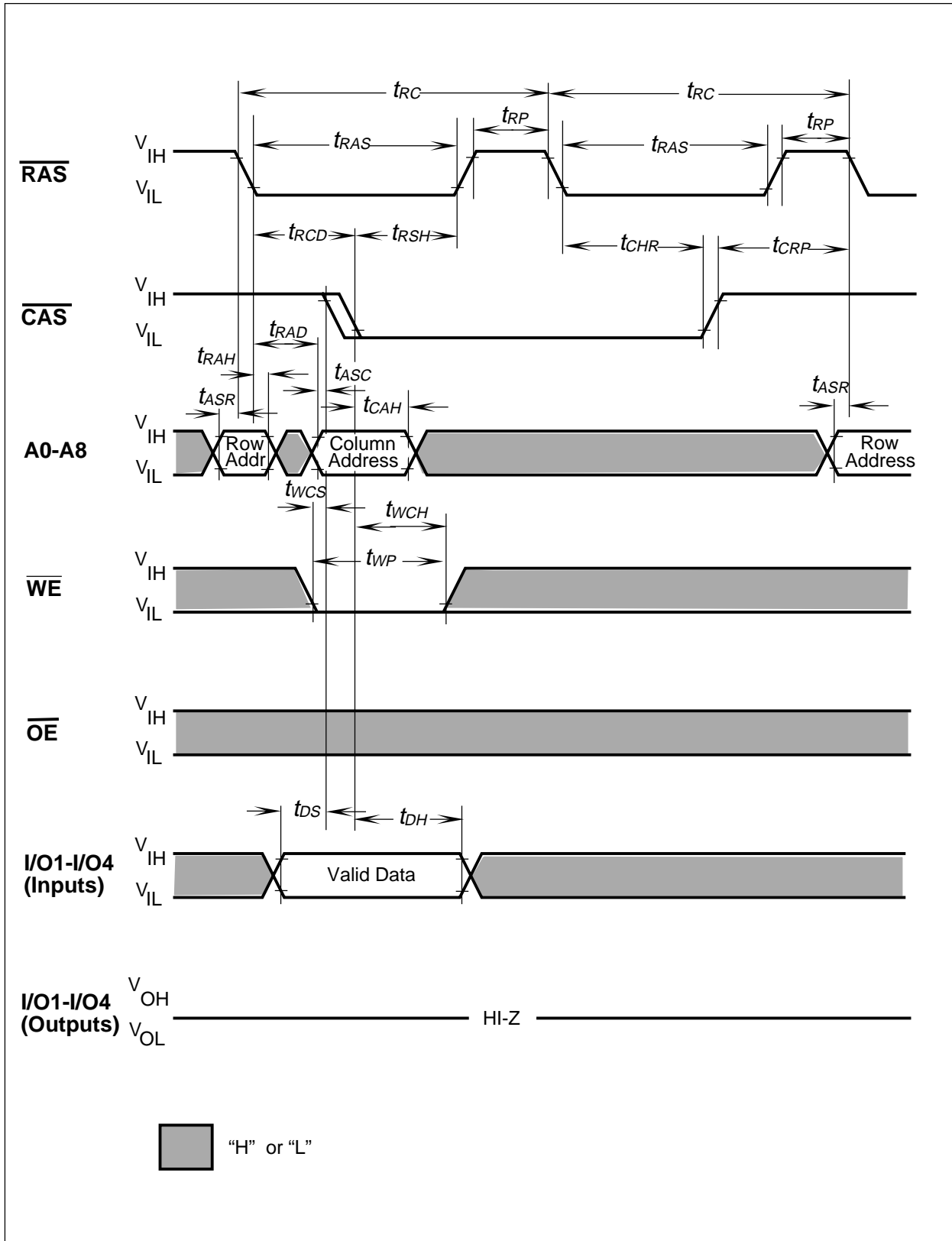
**$\overline{\text{RAS}}$ -Only Refresh Cycle**



CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)

