

## 2M x 8 - Bit Dynamic RAM 2k Refresh (Hyper Page Mode- EDO)

HYB5117805BSJ -50/-60/-70

### Advanced Information

- 2 097 152 words by 8-bit organization
- 0 to 70 °C operating temperature
- Performance:

		-50	-60	-70	
t <sub>RAC</sub>	$\overline{RAS}$ access time	50	60	70	ns
t <sub>CAC</sub>	$\overline{CAS}$ access time	13	15	20	ns
t <sub>AA</sub>	Access time from address	25	30	35	ns
t <sub>RC</sub>	Read/Write cycle time	84	104	124	ns
t <sub>HPC</sub>	Hyper page mode (EDO) cycle time	20	25	30	ns

- Single + 5 V (± 10 %) supply
- Low power dissipation  
max. 660 mW active (-50 version)  
max. 605 mW active (-60 version)  
max. 550 mW active (-70 version)  
11 mW standby (TTL)  
5.5. mW standby (MOS)
- Read, write, read-modify-write,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, hidden refresh, self refresh and test mode
- Hyper page mode (EDO) capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles / 32 ms (2k-Refresh)
- Plastic Package: P-SOJ-28-3 400 mil

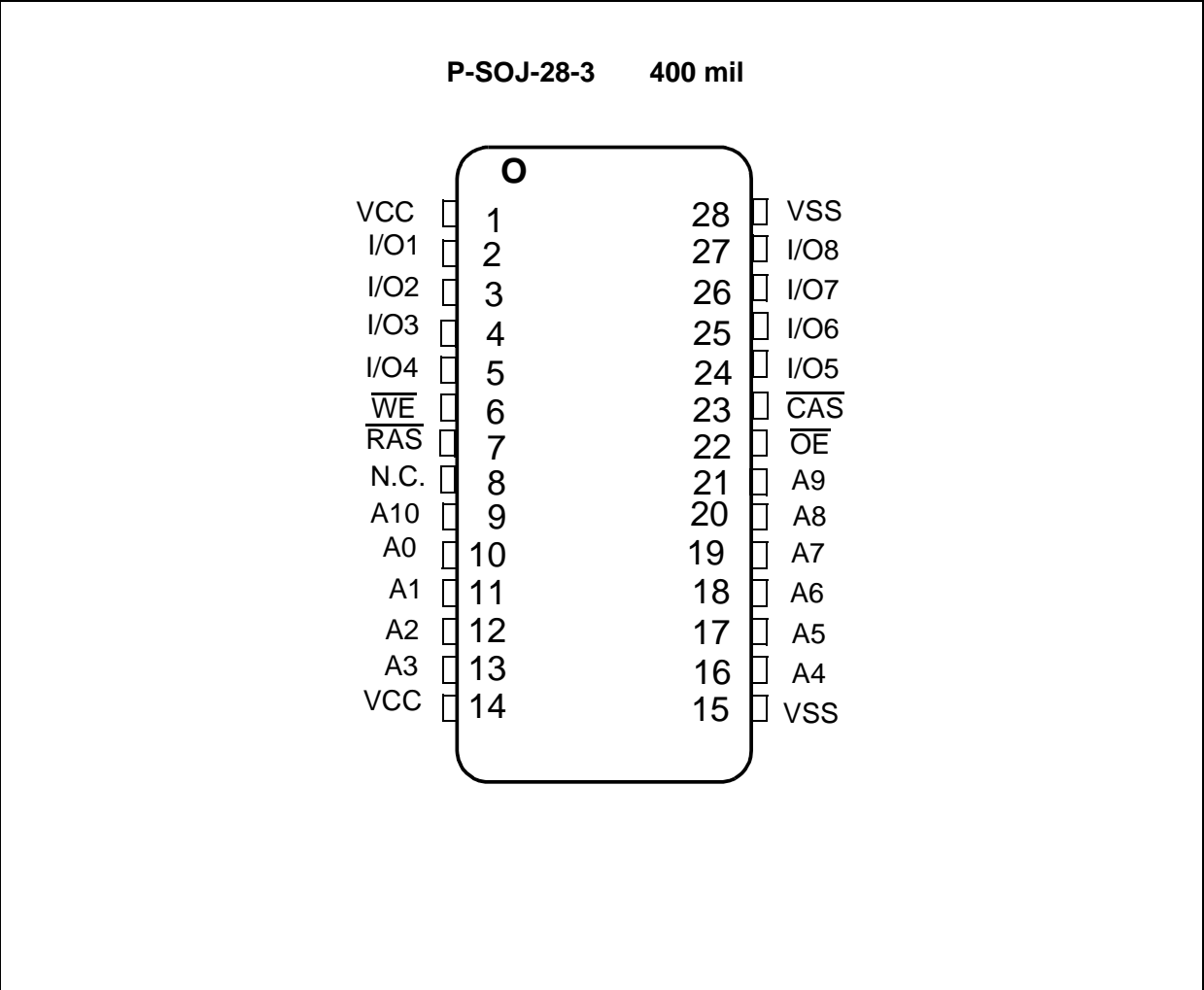
The HYB 5117805BSJ is a 16 MBit dynamic RAM organized as 2 097 152 words by 8-bits. The HYB 5117805BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5117805BSJ to be packaged in a standard SOJ 28 plastic package with 400 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V ( $\pm 10\%$ ) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

### Ordering Information

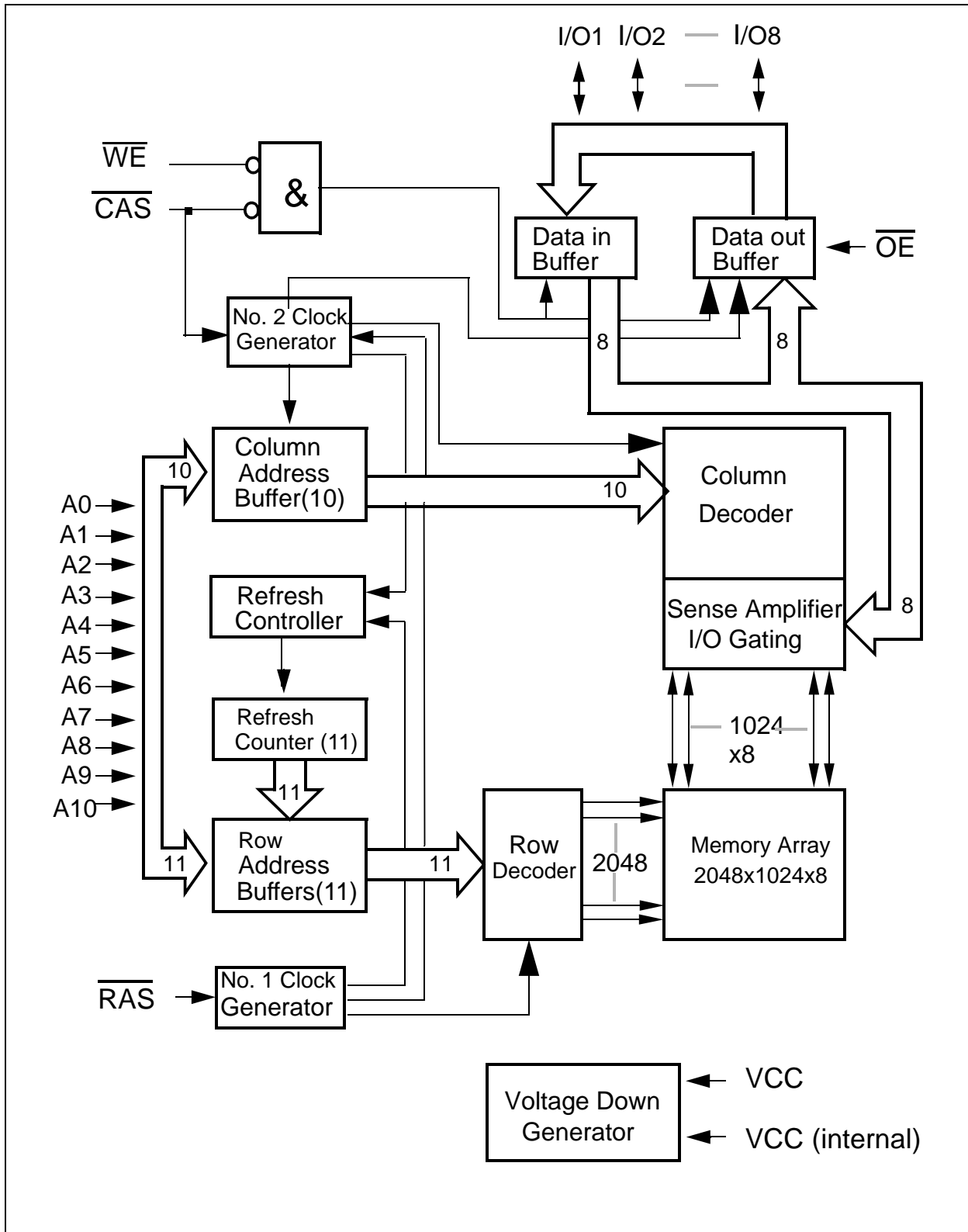
Type	Ordering Code	Package	Descriptions
HYB 5117805BJ-50	Q67100-Q1104	P-SOJ-28-3 400 mil	DRAM (access time 50 ns)
HYB 5117805BJ-60	Q67100-Q1105	P-SOJ-28-3 400 mil	DRAM (access time 60 ns)
HYB 5117805BJ-70	Q67100-Q1106	P-SOJ-28-3 400 mil	DRAM (access time 70 ns)

### Pin Names

A0-A10	Row Address Inputs
A0-A9	Column Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$V_{\text{CC}}$	Power Supply (+ 5 V)
$V_{\text{SS}}$	Ground (0 V)
N.C.	not connected



Pin Configuration



**Block Diagram**

### Absolute Maximum Ratings

Operating temperature range .....	0 to 70 °C
Storage temperature range.....	– 55 to 150 °C
Input/output voltage .....	-0.5 to min (V <sub>CC</sub> +0.5,7.0) V
Power supply voltage.....	-1.0V to 7.0 V
Power dissipation.....	1.0 W
Data out current (short circuit) .....	50 mA

### Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to 70 °C,  $V_{SS} = 0$  V,  $V_{CC} = 5$  V  $\pm$  10 %;  $t_T = 2$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.4	$V_{CC}+0.5$	V	1)
Input low voltage	$V_{IL}$	– 0.5	0.8	V	1)
Output high voltage ( $I_{OUT} = -5$ mA)	$V_{OH}$	2.4	–	V	1)
Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{OL}$	–	0.4	V	1)
Input leakage current ( $0$ V $\leq V_{IH} \leq V_{CC} + 0.3$ V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	$\mu$ A	1)
Output leakage current (DO is disabled, $0$ V $\leq V_{OUT} \leq V_{CC} + 0.3$ V)	$I_{O(L)}$	– 10	10	$\mu$ A	1)
Average $V_{CC}$ supply current: <div style="margin-left: 20px;">-50 ns version</div> <div style="margin-left: 20px;">-60 ns version</div> <div style="margin-left: 20px;">-70 ns version</div> ( $\overline{RAS}$ , $\overline{CAS}$ , address cycling: $t_{RC} = t_{RC}$ min.)	$I_{CC1}$	–	120 110 100	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$	–	2	mA	–
Average $V_{CC}$ supply current, during $\overline{RAS}$ -only refresh cycles: <div style="margin-left: 20px;">-50 ns version</div> <div style="margin-left: 20px;">-60 ns version</div> <div style="margin-left: 20px;">-70 ns version</div> ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = t_{RC}$ min.)	$I_{CC3}$	–	120 110 100	mA mA mA	2) 4) 2) 4) 2) 4)

### DC Characteristics

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 5$  V  $\pm$  10 %;  $t_T = 2$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current, during hyper page mode: -50 ns version -60 ns version -70 ns version ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: $t_{PC} = t_{PC}$ min.)	$I_{CC4}$	–	70 55 45	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	$I_{CC5}$	–	1	mA	1)
Average $V_{CC}$ supply current, during $\overline{CAS}$ -before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ( $\overline{RAS}$ , $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ min.)	$I_{CC6}$	–	120 110 100	mA mA mA	2) 4) 2) 4) 2) 4)
Average Self Refresh Current  (CBR cycle with $t_{RAS} > TRASS_{min.}$ , $\overline{CAS}$ held low, $\overline{WE} = V_{CC} - 0.2$ V, Address and Din = $V_{CC} - 0.2$ V or 0.2V)	$I_{CC7}$	–	1	mA	

### Capacitance

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
I/O capacitance (I/O1-I/O8)	$C_{I0}$	–	7	pF

### AC Characteristics <sup>5)6)</sup>

16E

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

#### **common parameters**

Random read or write cycle time	$t_{RC}$	84	–	104	–	124	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	30	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	8	10k	10	10k	12	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	8	–	10	–	12	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	12	37	14	45	14	53	ns	
$\overline{RAS}$ to column address delay	$t_{RAD}$	10	25	12	30	12	35	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	13		15	–	17	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	40		50	–	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	1	50	1	50	ns	7
Refresh period	$t_{REF}$	–	32	–	32	–	32	ms	

#### **Read Cycle**

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	–	17	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	$t_{OEA}$	–	13	–	15	–	17	ns	
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	35	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	$t_{RRH}$	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	$t_{CLZ}$	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	0	17	ns	12
Output turn-off delay from $\overline{OE}$	$t_{OEZ}$	0	13	0	15	0	17	ns	12

### AC Characteristics (cont'd) 5)6)

16E

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 5 \text{ V} \pm 10 \%, t_T = 2 \text{ ns}$ 

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Data to $\overline{\text{CAS}}$ low delay	$t_{DZC}$	0	–	0	–	0	–	ns	13
Data to $\overline{\text{OE}}$ low delay	$t_{DZO}$	0	–	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	$t_{CDD}$	10	–	13	–	15	–	ns	14
$\overline{\text{OE}}$ high to data delay	$t_{ODD}$	10	–	13	–	15	–	ns	14

### Write Cycle

Write command hold time	$t_{WCH}$	8	–	10	–	10	–	ns	
Write command pulse width	$t_{WCP}$	8	–	10	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	$t_{RWL}$	13	–	15	–	17	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{CWL}$	13	–	15	–	17	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	0	–	ns	16
Data hold time	$t_{DH}$	8	–	10	–	12	–	ns	16

### Read-modify-Write Cycle

Read-write cycle time	$t_{RWC}$	113	–	138	–	162	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{RWD}$	64	–	77	–	89	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{CWD}$	27	–	32	–	36	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	$t_{AWD}$	39	–	47	–	54	–	ns	15
$\overline{\text{OE}}$ command hold time	$t_{OEH}$	10	–	13	–	15	–	ns	

### Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	$t_{HPC}$	20	–	25	–	30	–	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	8	–	10	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{CPA}$	–	27	–	32	–	37	ns	7
Output data hold time	$t_{COH}$	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width in EDO mode	$t_{RAS}$	50	200k	60	200k	70	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	$t_{RHPC}$	27	–	32	–	37	–	ns	



### AC Characteristics (cont'd) 5)6)

16E

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 5 \text{ V} \pm 10 \%, t_T = 2 \text{ ns}$ 

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

#### Hyper Page Mode (EDO) Read-modify-Write Cycle

Hyper page mode (EDO) read-write cycle time	$t_{PRWC}$	58	–	68	–	77	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	$t_{CPWD}$	41	–	49	–	56	–	ns	

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

$\overline{\text{CAS}}$ setup time	$t_{CSR}$	10	–	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	$t_{CHR}$	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{RPC}$	5	–	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{WRP}$	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	$t_{WRH}$	10	–	10	–	10	–	ns	

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

$\overline{\text{CAS}}$ precharge time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle)	$t_{CPT}$	35	–	40	–	40	–	ns	
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#### Self Refresh Cycle

$\overline{\text{RAS}}$ pulse width	$t_{RASS}$	100k	–	100k	–	100k	–	ns	17
$\overline{\text{RAS}}$ precharge time	$t_{RPS}$	95	–	110	–	130	–	ns	17
$\overline{\text{CAS}}$ hold time	$t_{CHS}$	-50	–	-50	–	-50	–	ns	17

#### Test Mode

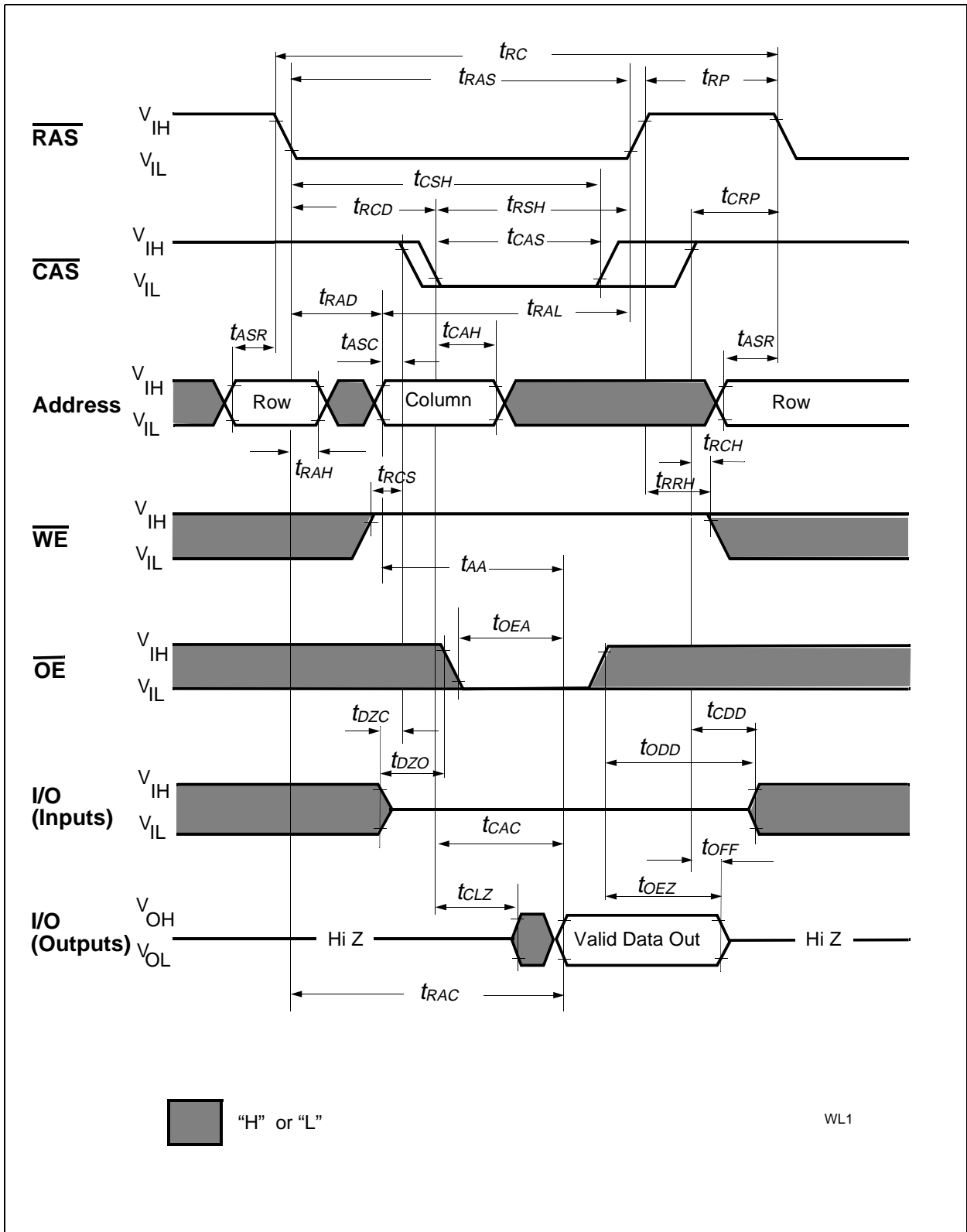
Write command setup time	$t_{WTS}$	10	–	10	–	10	–	ns	
Write command hold time	$t_{WTH}$	10	–	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	$t_{CHRT}$	30	–	30	–	30	–	ns	

**Notes:**

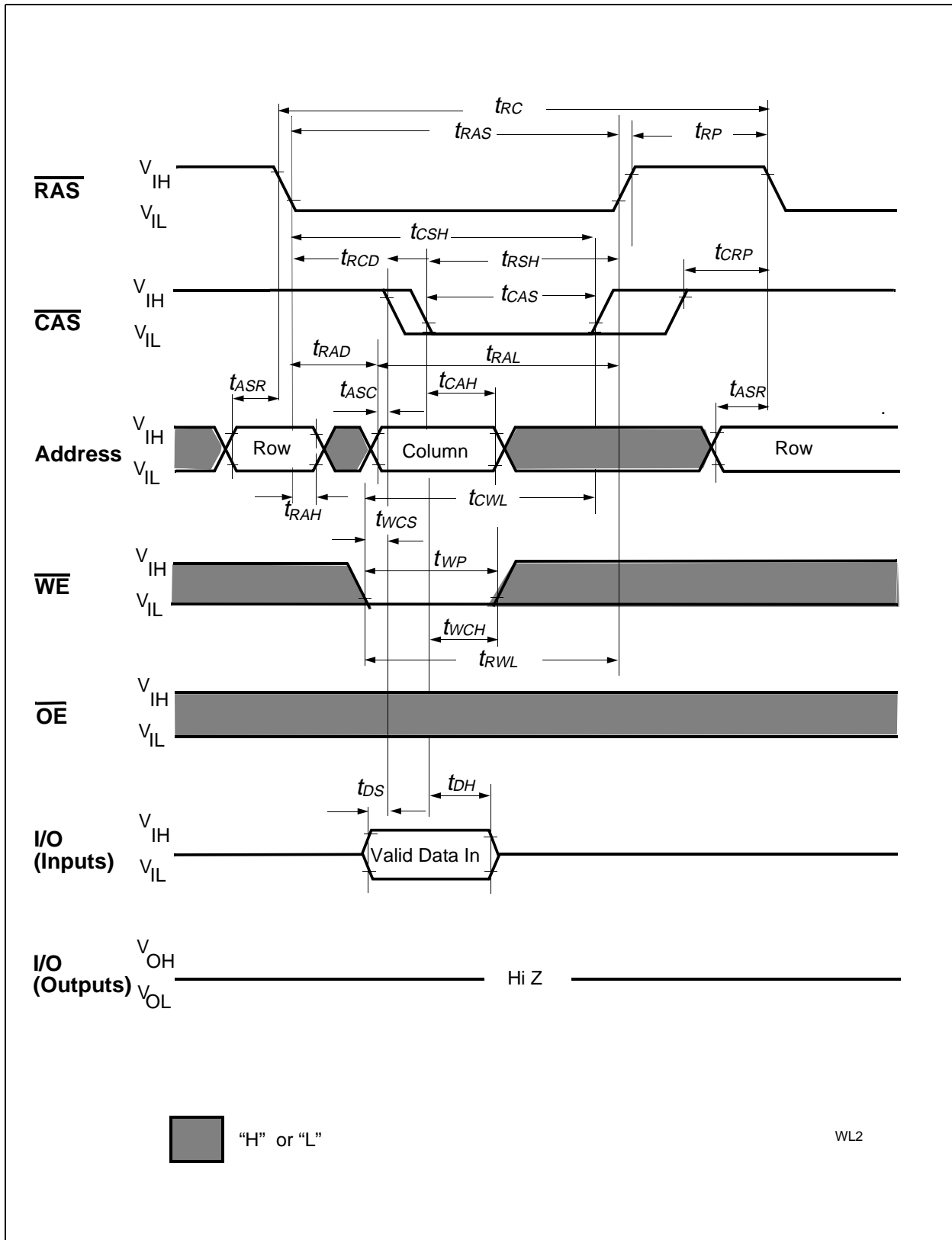
- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while  $RAS = \overline{Vil}$ . In case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle
- 5) An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 2$  ns.
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with the specified current load and 100 pF at  $V_{ol} = 0.8$  V and  $V_{oh} = 2.0$  V. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ ,  $t_{OEA}$ .  $t_{CAC}$  is measured from tristate.
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{AA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$ ,  $t_{OEZ (max.)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.  $t_{OFF}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.
- 13) Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
- 14) Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
- 15)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD (min.)}$ ,  $t_{CWD} > t_{CWD (min.)}$  and  $t_{AWD} > t_{AWD (min.)}$ , the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
 

If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

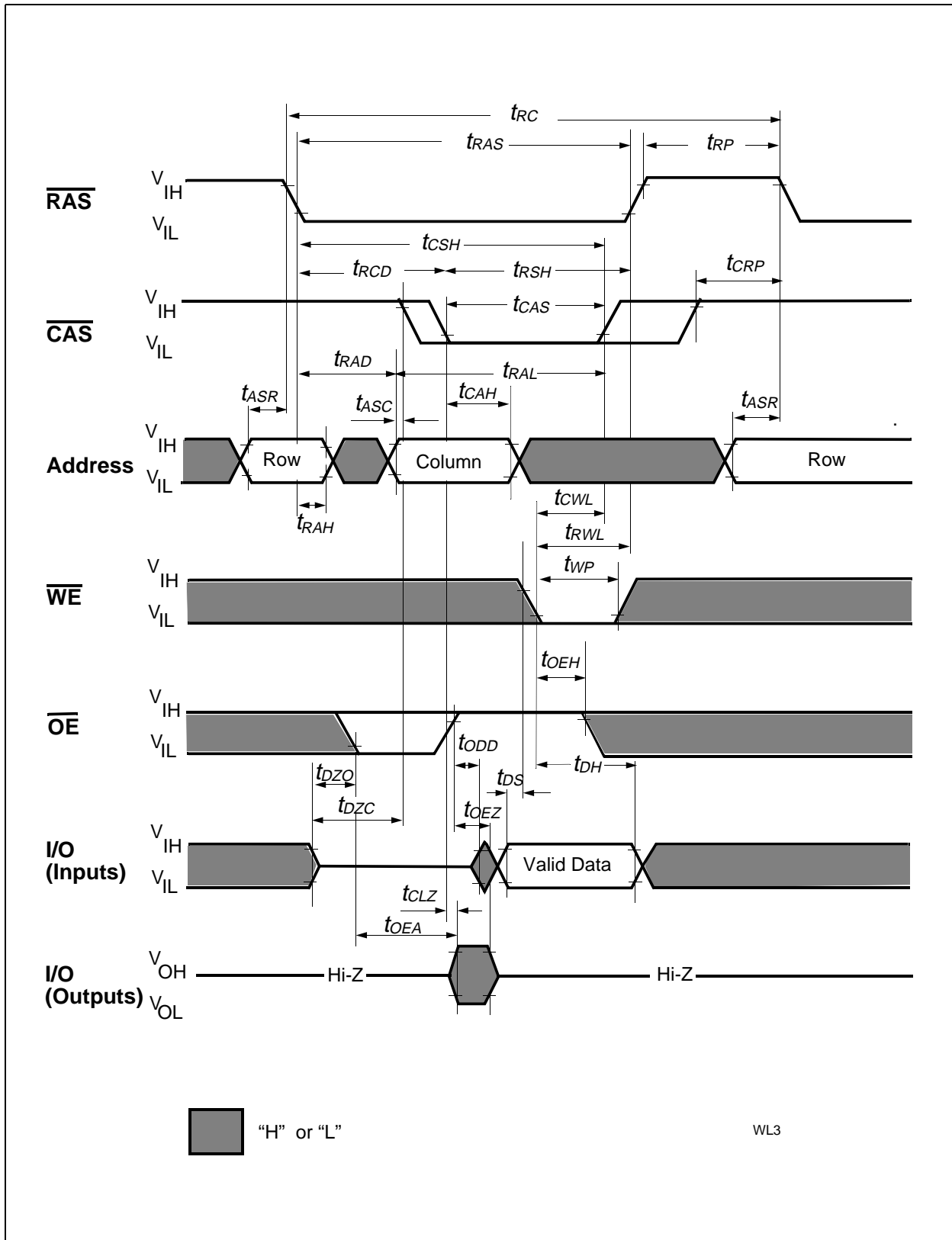
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh



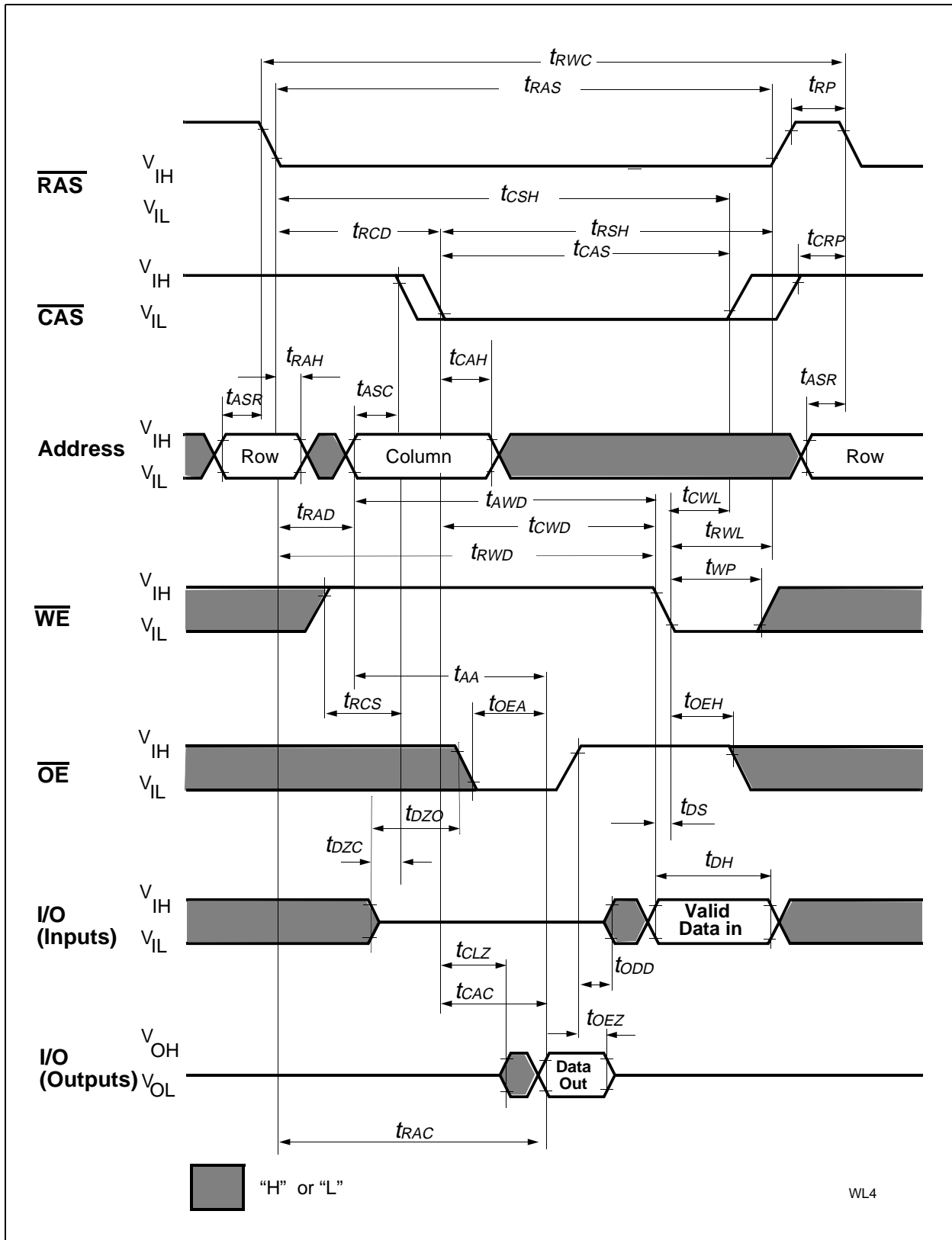
Read Cycle



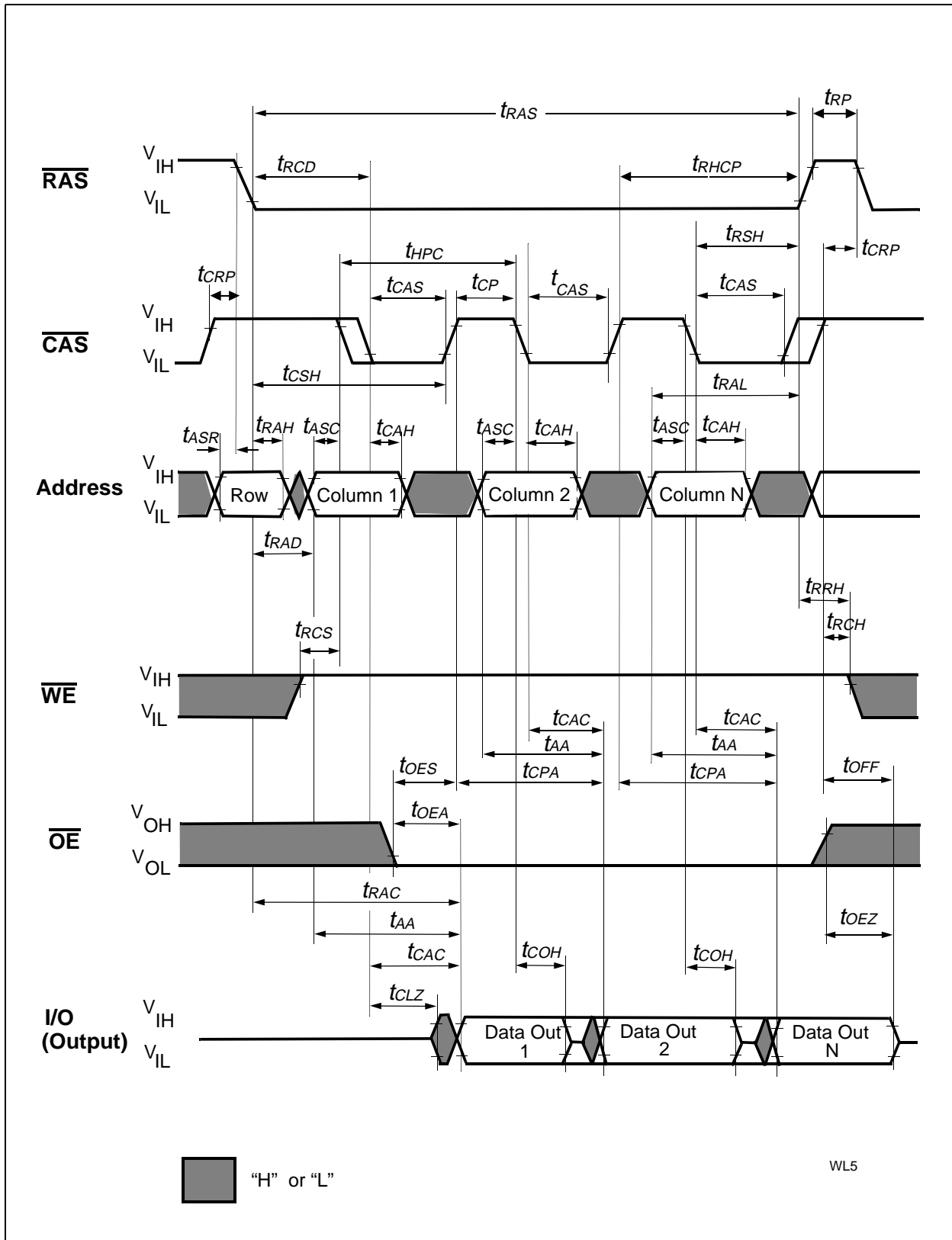
Write Cycle (Early Write)



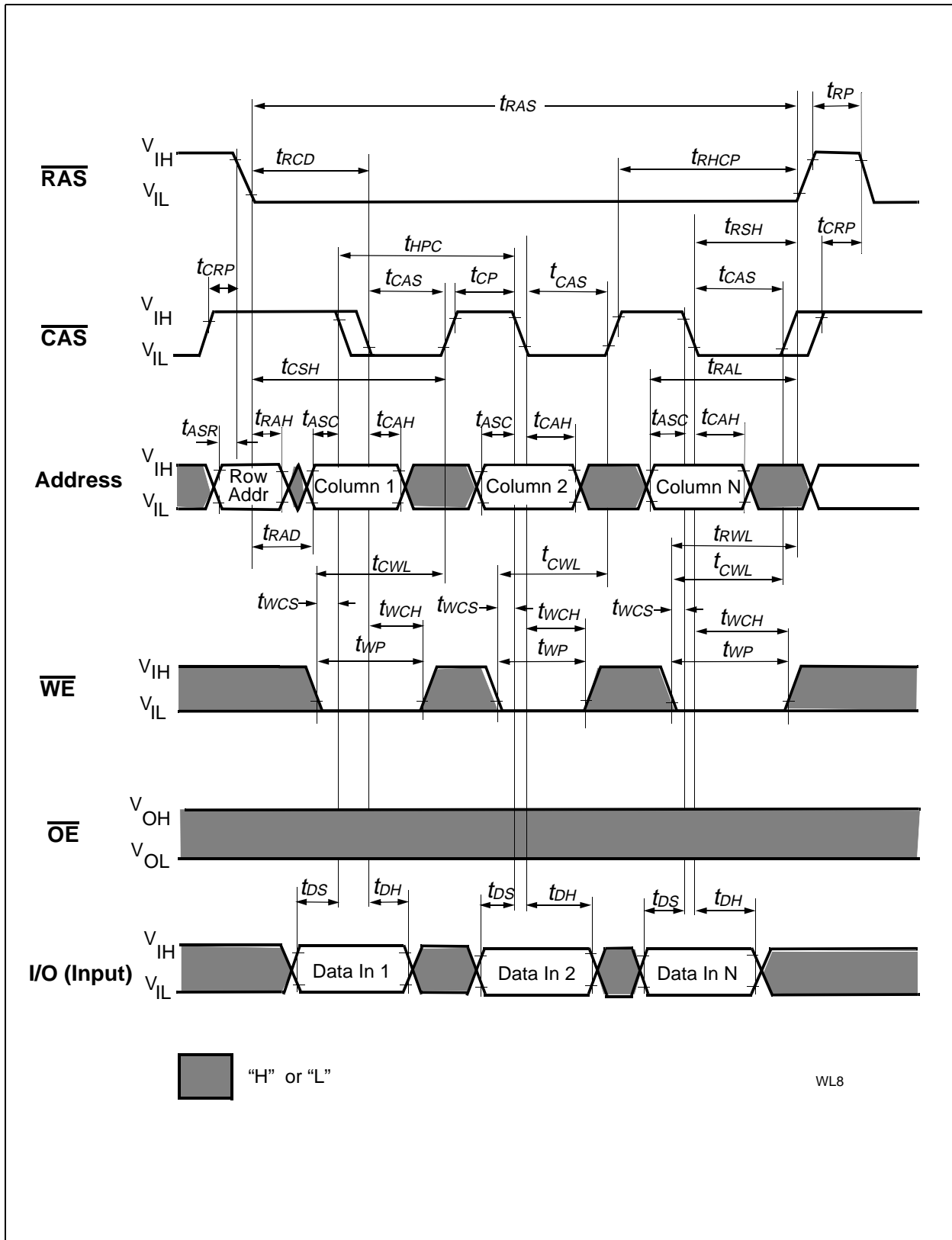
Write Cycle ( $\overline{OE}$  Controlled Write)



**Read-Write (Read-Modify-Write) Cycle**



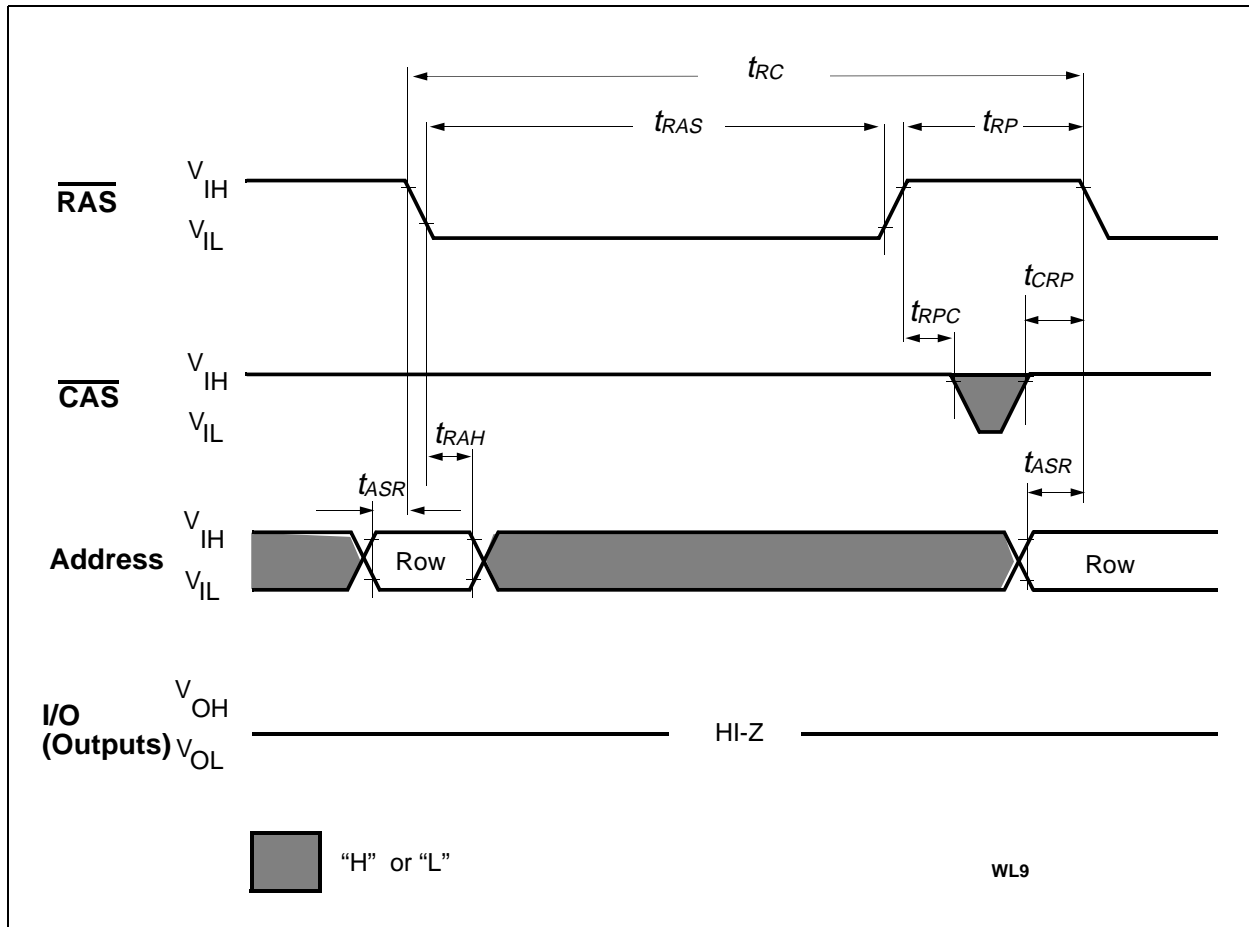
Hyper Page Mode (EDO) Read Cycle



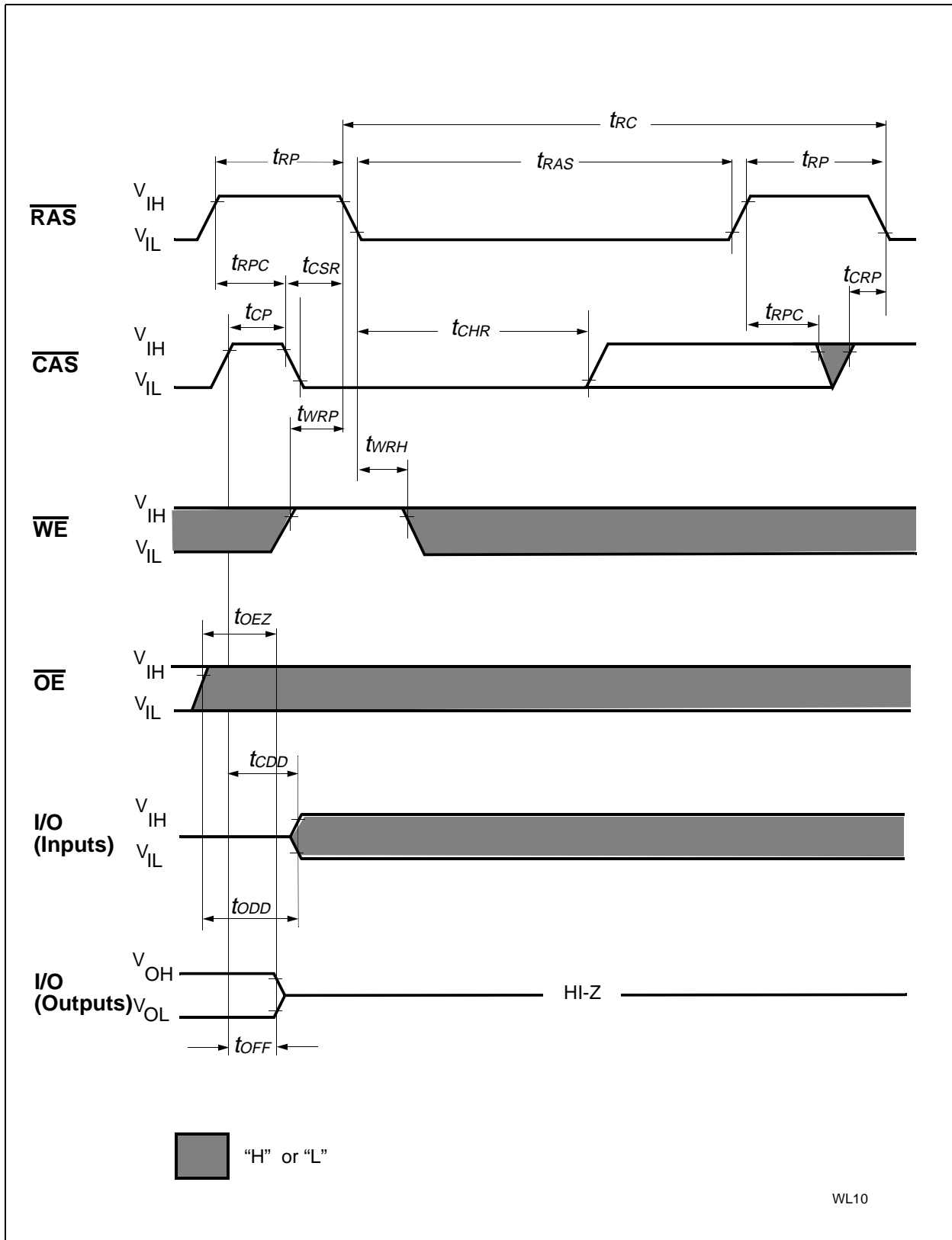
Hyper Page Mode (EDO) Early Write Cycle



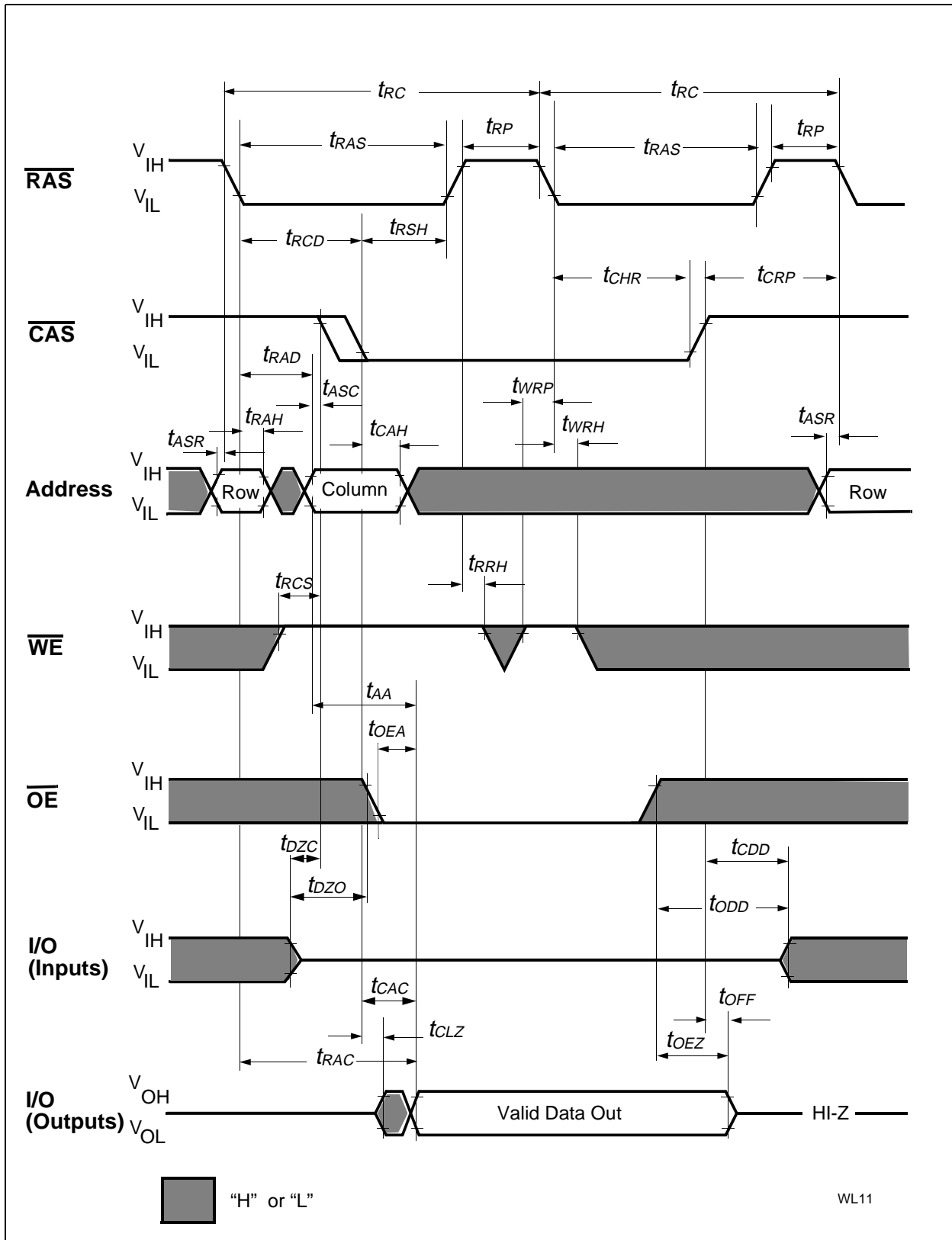




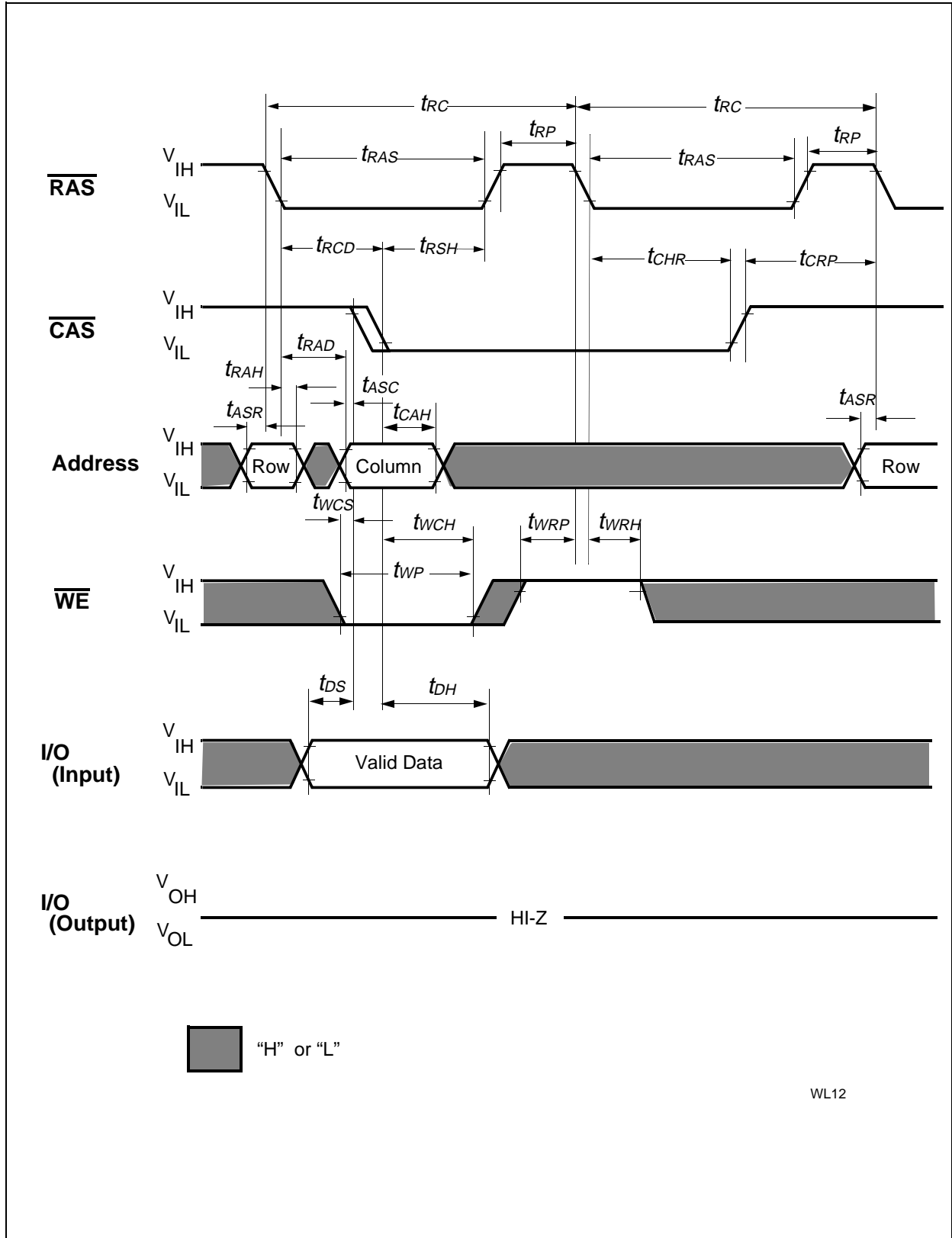
$\overline{\text{RAS}}$ -Only Refresh Cycle



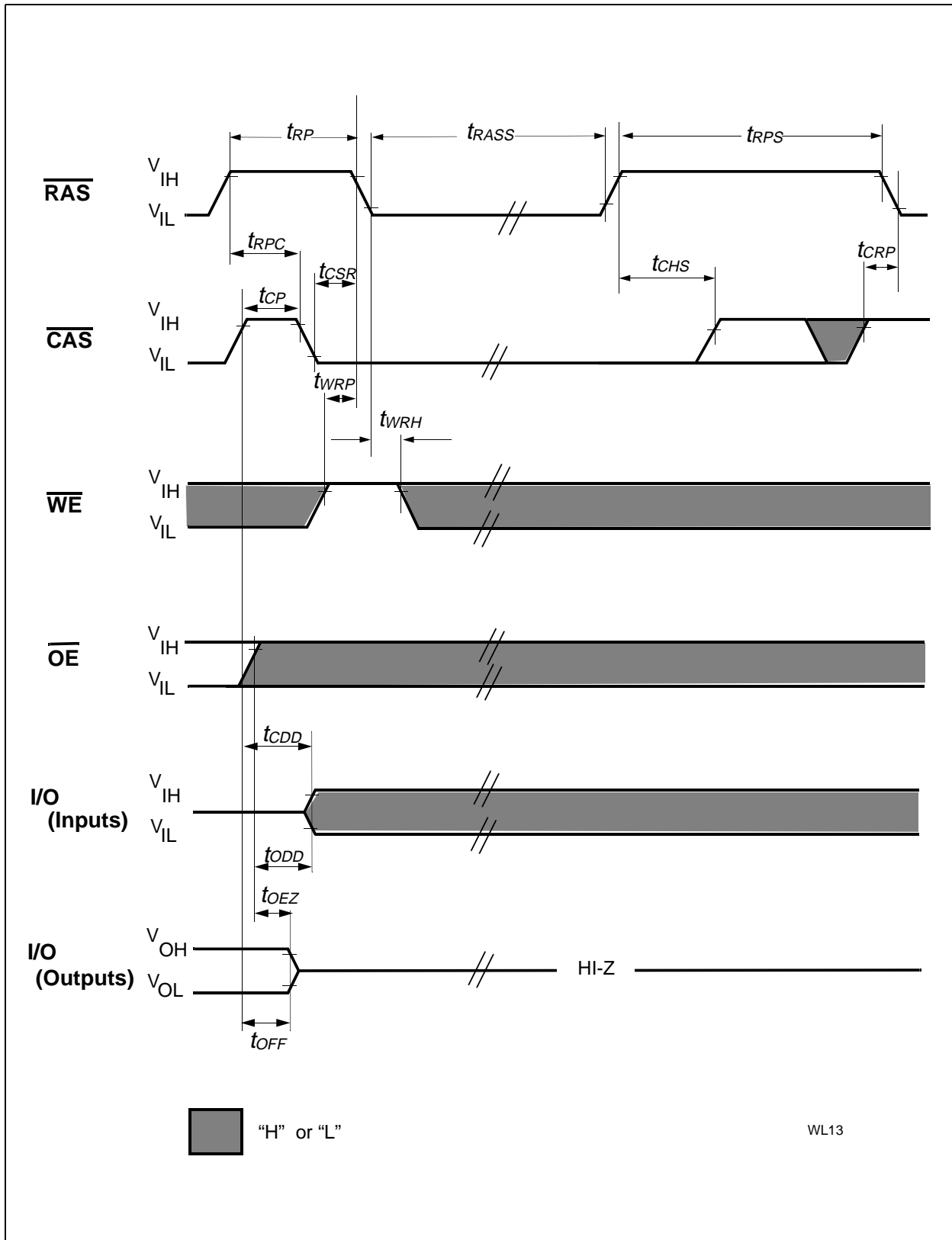
**CAS-Before-RAS Refresh Cycle**



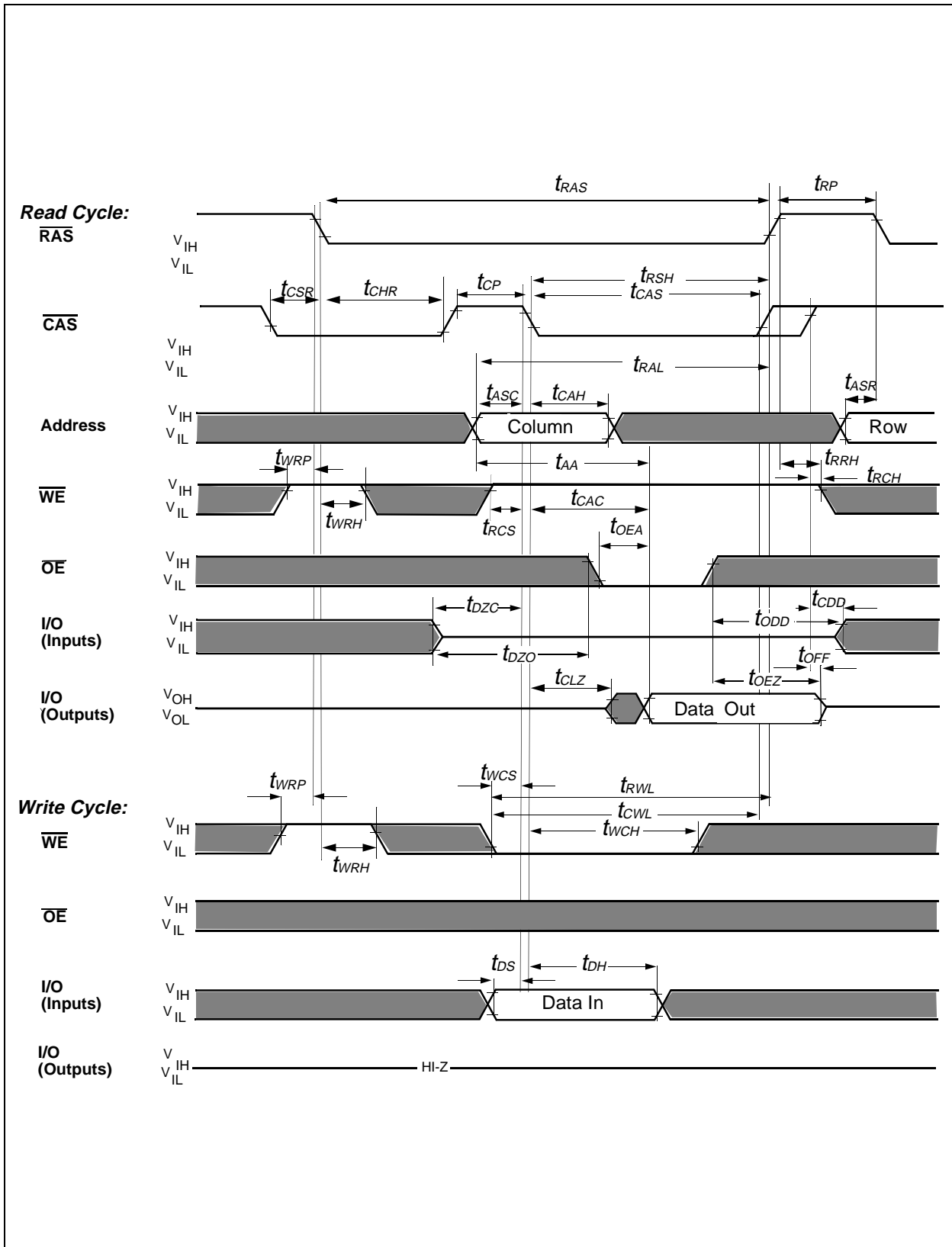
Hidden Refresh Cycle (Read) Cycle



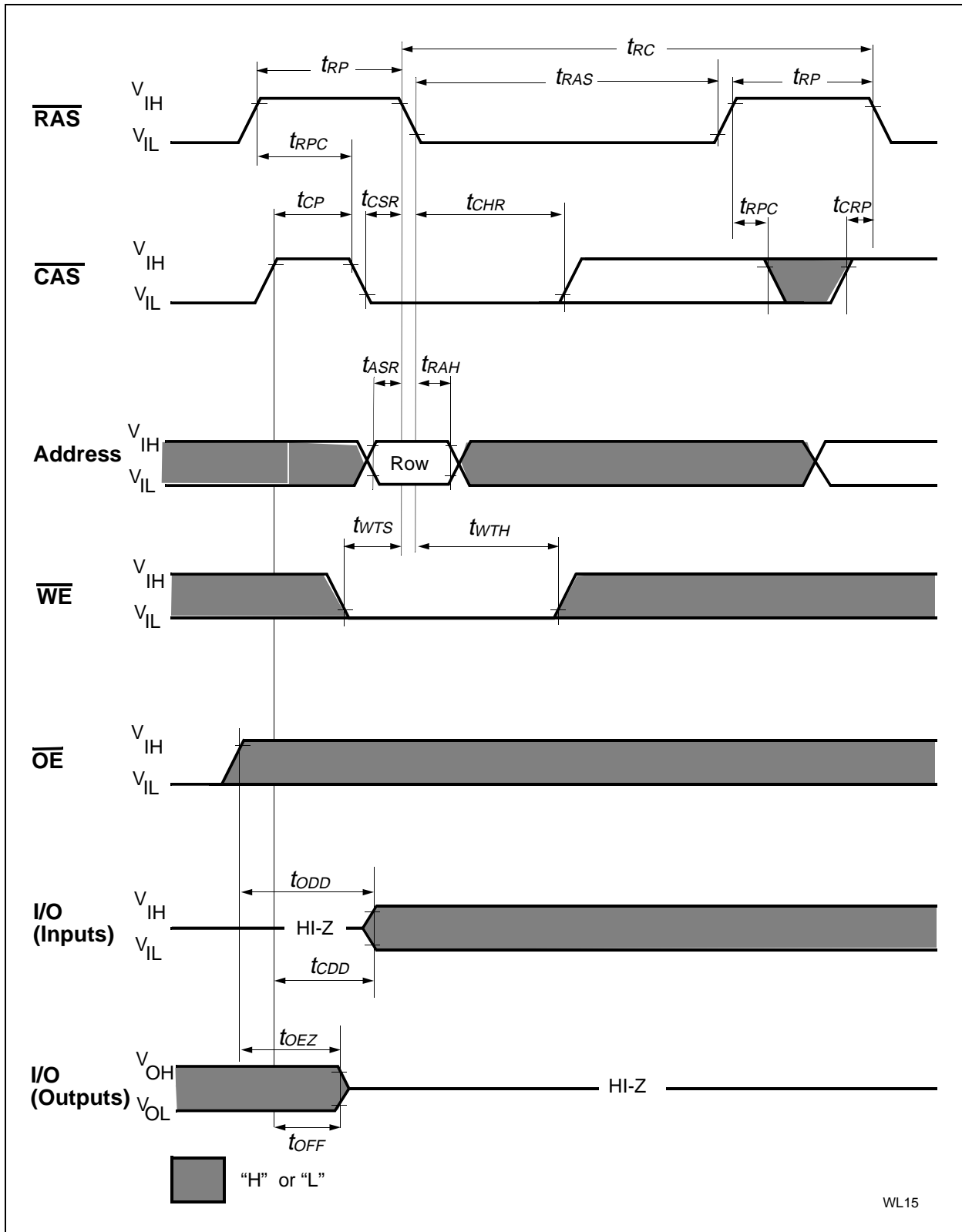
Hidden Refresh Early Write Cycle



Self Refresh



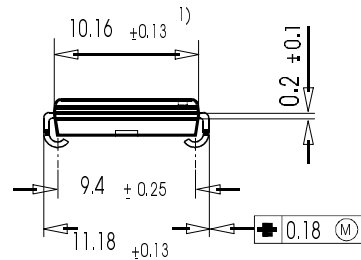
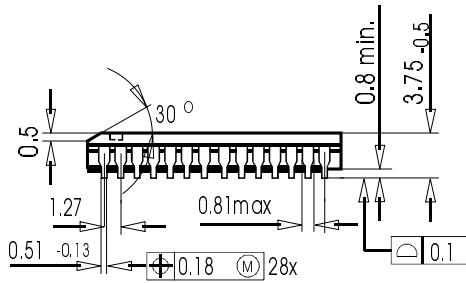
### $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle



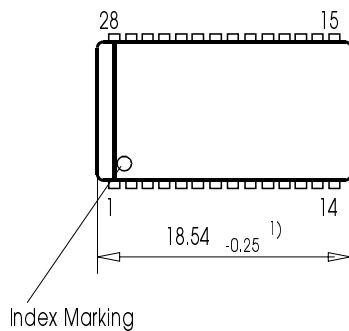
Test Mode Entry



### Plastic Package P-SOJ-28-3 (400mil) (Small Outline J-lead, SMD)



GPJ05699



Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

### Package Outline