SIEMENS

1M × 4-Bit Dynamic RAM — HYB 314400BJ-50/-60

Advanced Information

- 1 048 576 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode Operation
- Performance:

		-50	-60	
t_{RAC}	$\overline{RAS}$ access time	50	60	ns
t_{CAC}	$\overline{CAS}$ access time	13	15	ns
t_{AA}	Access time from address	25	30	ns
t_{RC}	Read/Write cycle time	95	110	ns
t_{PC}	Fast page mode cycle time	35	40	ns

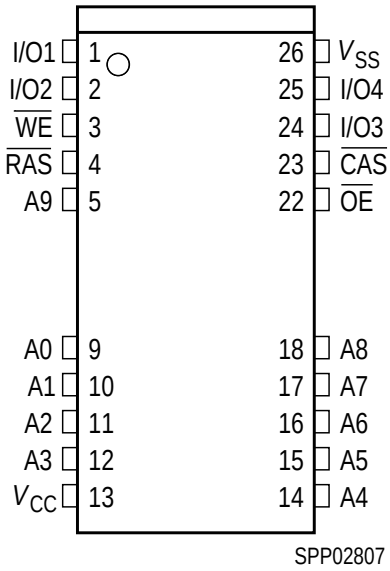
- Fast access and cycle time
  Single + 3.3 V (± 0.3 V) supply with a built-in VBB generator
- Low power dissipation
  max. 252 mW active (-50 version)
  max. 216 mW active (-60 version)
- Standby power dissipation:
  7.2 mW max. standby (LVTTL)
  3.6 mW max. standby (LVCMOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh and test mode capability
- All inputs and outputs LVTTL-compatible
- 1024 refresh cycles / 16 ms
- Plastic Packages: P-SOJ-26/20-2 with 300 mil width

The HYB 314400BJ is the new generation dynamic RAM organized as 1 048 576 words by 4-bit. The HYB 314400BJ utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 314400BJ to be packed in a standard plastic P-SOJ-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 3.3 V (± 0.3 V) power supply, direct interfacing with high performance logic device families.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 314400BJ-50	on request	P-SOJ-26/20-2 300 mil	3.3 V DRAM (access time 50 ns)
HYB 314400BJ-60	on request	P-SOJ-26/20-2 300 mil	3.3 V DRAM (access time 60 ns)

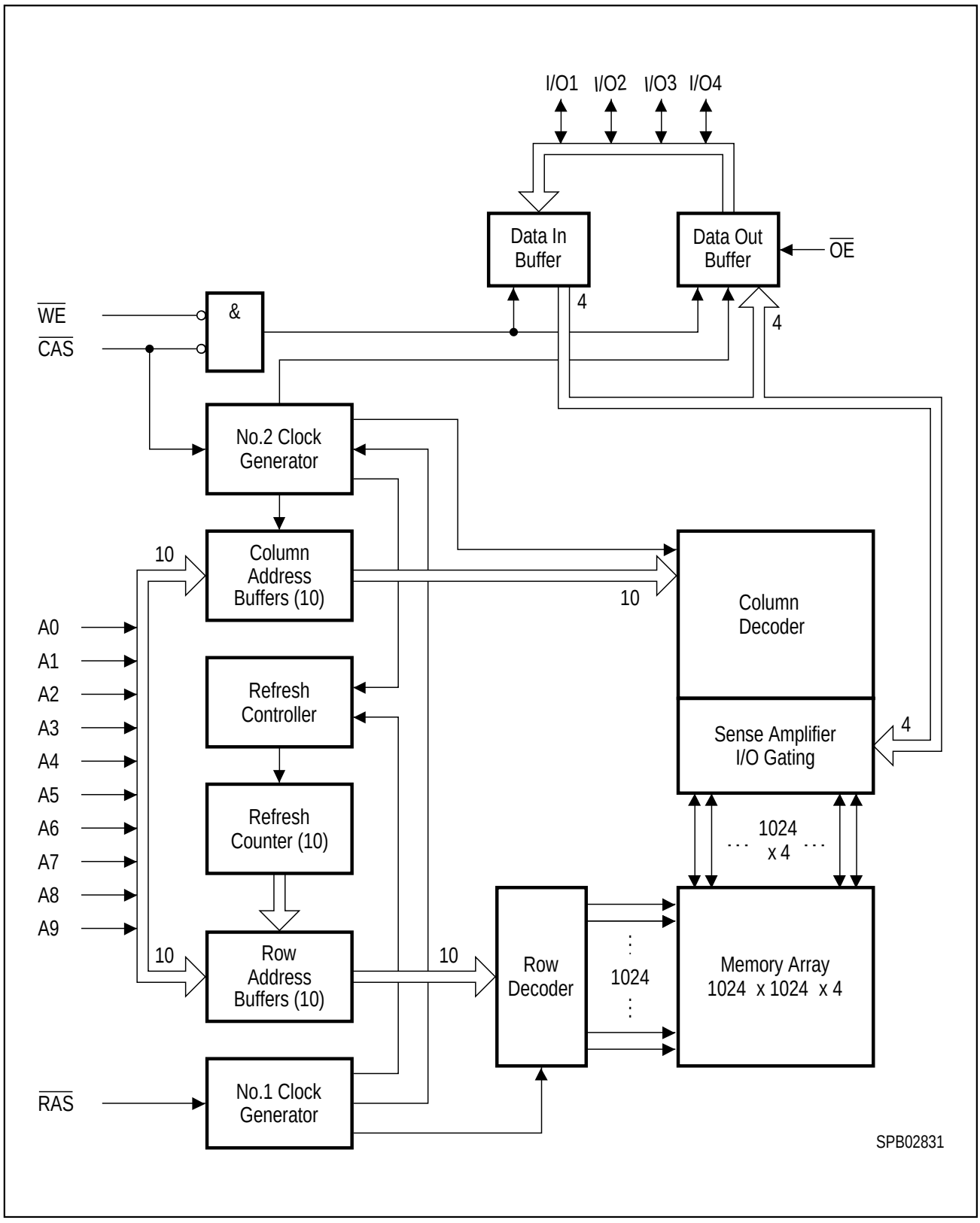
P-SOJ-26/20-2



Pin Configuration

Pin Names

A0 - A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 - I/O4	Data Input/Output
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	No Connection



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range..... – 55 to + 150 °C
Input/output voltage ..... – 1 to min (V_{CC} + 0.5, 4.6) V
Power Supply voltage ..... – 1 to + 4.6 V
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	[1]
Input low voltage	V_{IL}	– 1.0	0.8	V	[1]
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	[1]
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	[1]
CMOS Output high voltage (I_{OUT} = – 100 µA)	V_{OH}	V_{CC} – 0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 µA)	V_{OL}	–	0.2	V	
Input leakage current, any input (0 V < V_{IN} < V_{CC} + 0.3 V, all other input = 0 V)	$I_{I(L)}$	– 10	10	µA	[1]
Output leakage current (DO is disabled, 0 < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	[1]
Average V_{CC} supply current -50 version -60 version	I_{CC1}	 – –	 70 60	mA	[2, 3, 4]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{IH})	I_{CC2}	–	2	mA	
Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles -50 version -60 version	I_{CC3}	 – –	 70 60	mA	[2, 4]
Average V_{CC} supply current during fast page mode operation -50 version -60 version	I_{CC4}	 – –	 50 45	mA	[2, 3, 4]

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	µA	[1]
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode	I_{CC6}			mA	[2, 4]
-50 version		–	70		
-60 version		–	60		

Capacitance

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
Output capacitance (IO1 to IO4)	C_{IO}	–	7	pF

AC Characteristics [5, 6]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Common Parameters							
Random read or write cycle time	t_{RC}	95	–	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10k	15	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45		
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	–	16	–	16	ms	
Read Cycle							
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8, 10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	12

AC Characteristics (cont'd) [5, 6]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	ns	[13]
$\overline{CAS}$ high to data delay	t_{CDD}	13	–	15	–	ns	[14]
$\overline{OE}$ high to data delay	t_{ODD}	13	–	15	–	ns	[14]
Write Cycle							
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	[15]
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	[16]
Data hold time	t_{DH}	10	–	10	–	ns	[16]
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	ns	[13]
Read-Modify-Write Cycle							
Read-write cycle time	t_{RWC}	131	–	150	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	68	–	80	–	ns	[15]
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	31	–	35	–	ns	[15]
Column address to $\overline{WE}$ delay time	t_{AWD}	43	–	50	–	ns	[15]
$\overline{OE}$ command hold time	t_{OEH}	13	–	15	–	ns	
Fast Page Mode Cycle							
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	30	–	35	ns	[7]
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	30	–	35	–	ns	
Fast Page Mode Read-Modify-Write Cycle							
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	48	–	55	–	ns	

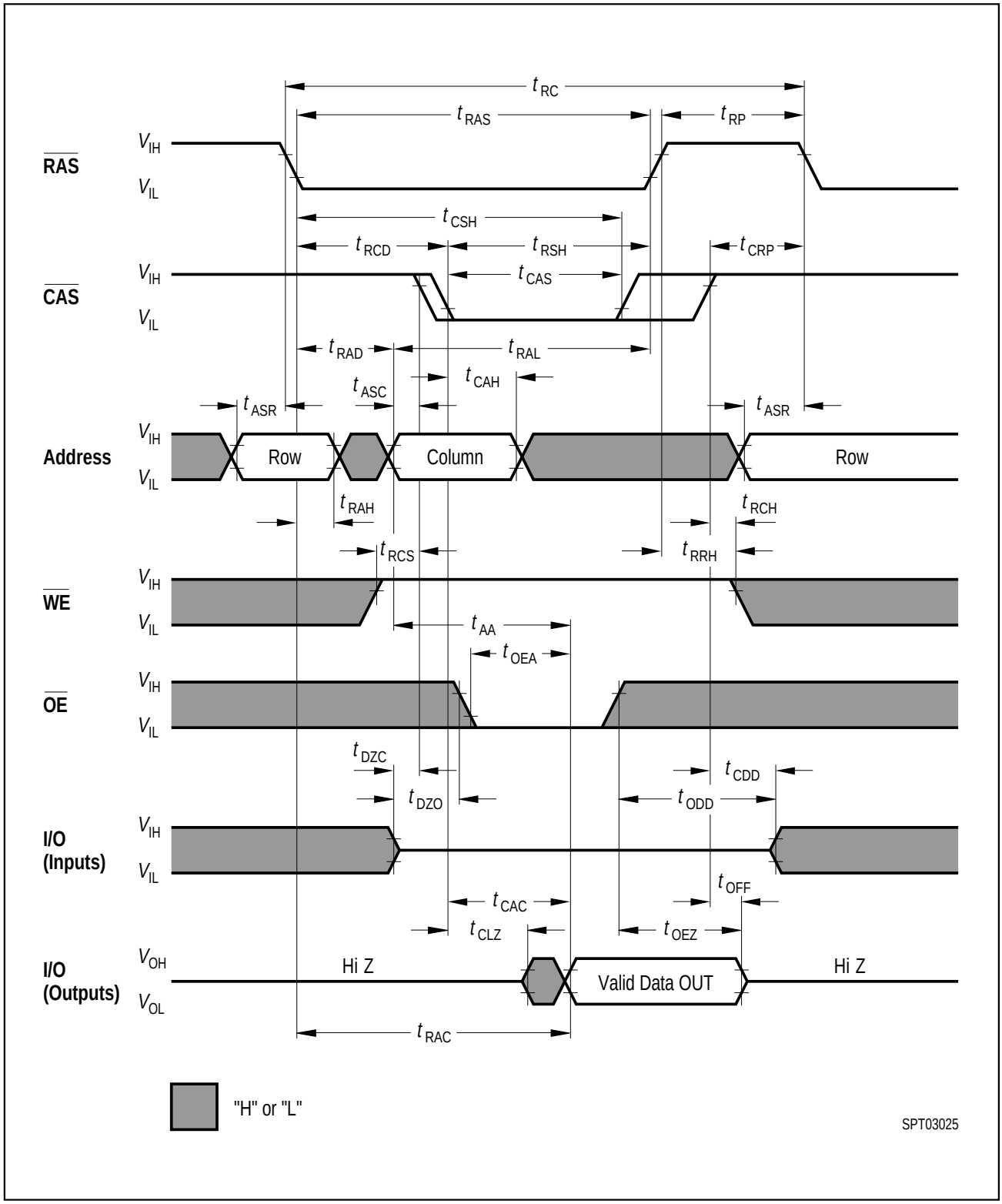
AC Characteristics (cont'd) [5, 6]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

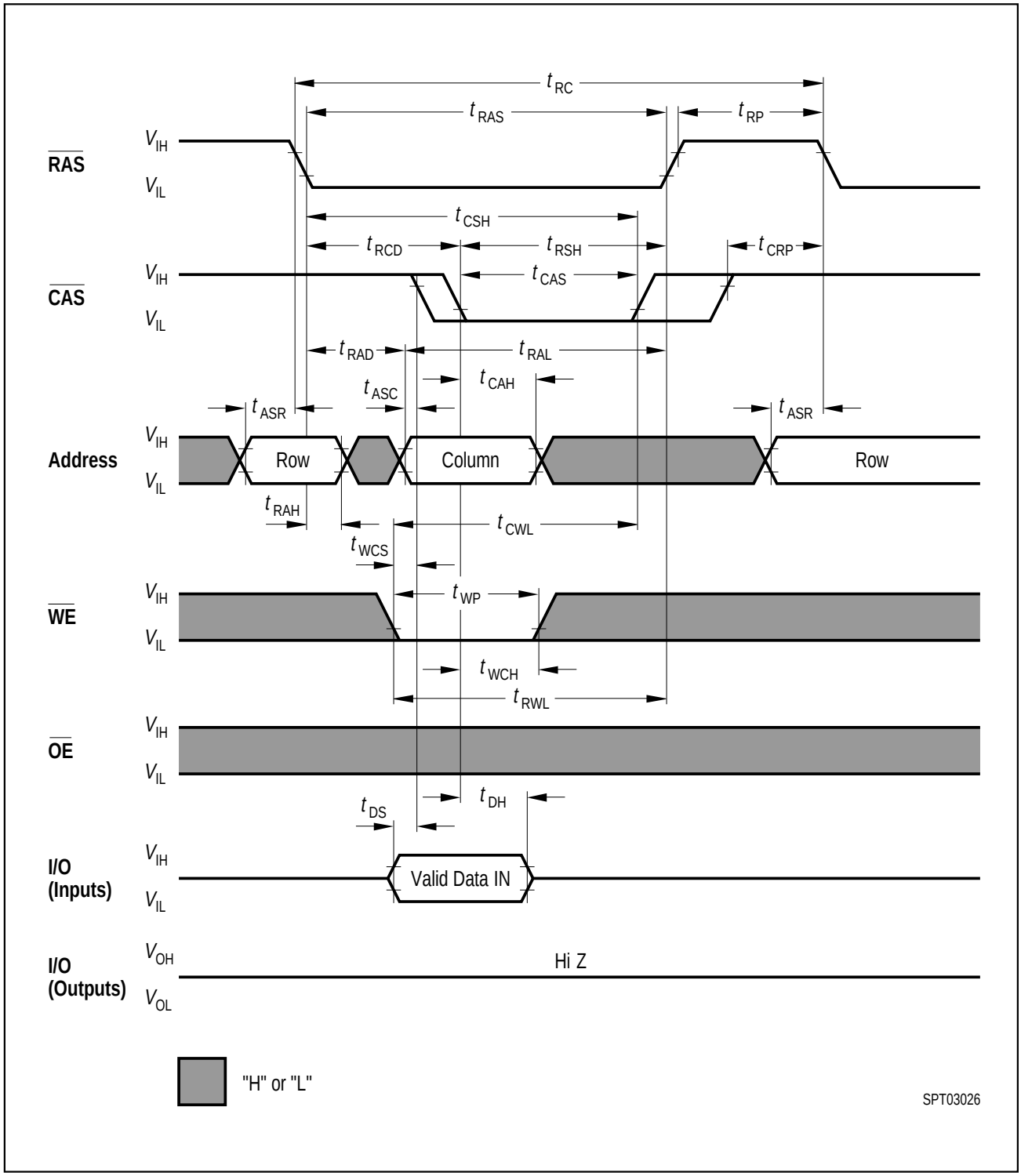
Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle							
$\overline{\text{CAS}}$ setup time	t_{CSR}	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	t_{CHR}	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	t_{WRH}	10	–	10	–	ns	
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Cycle							
$\overline{\text{CAS}}$ precharge time	t_{CPT}	35	–	40	–	ns	
Test Mode							
Write command setup time	t_{WTS}	10	–	10	–	ns	
Write command hold time	t_{WTH}	10	–	10	–	ns	

Notes

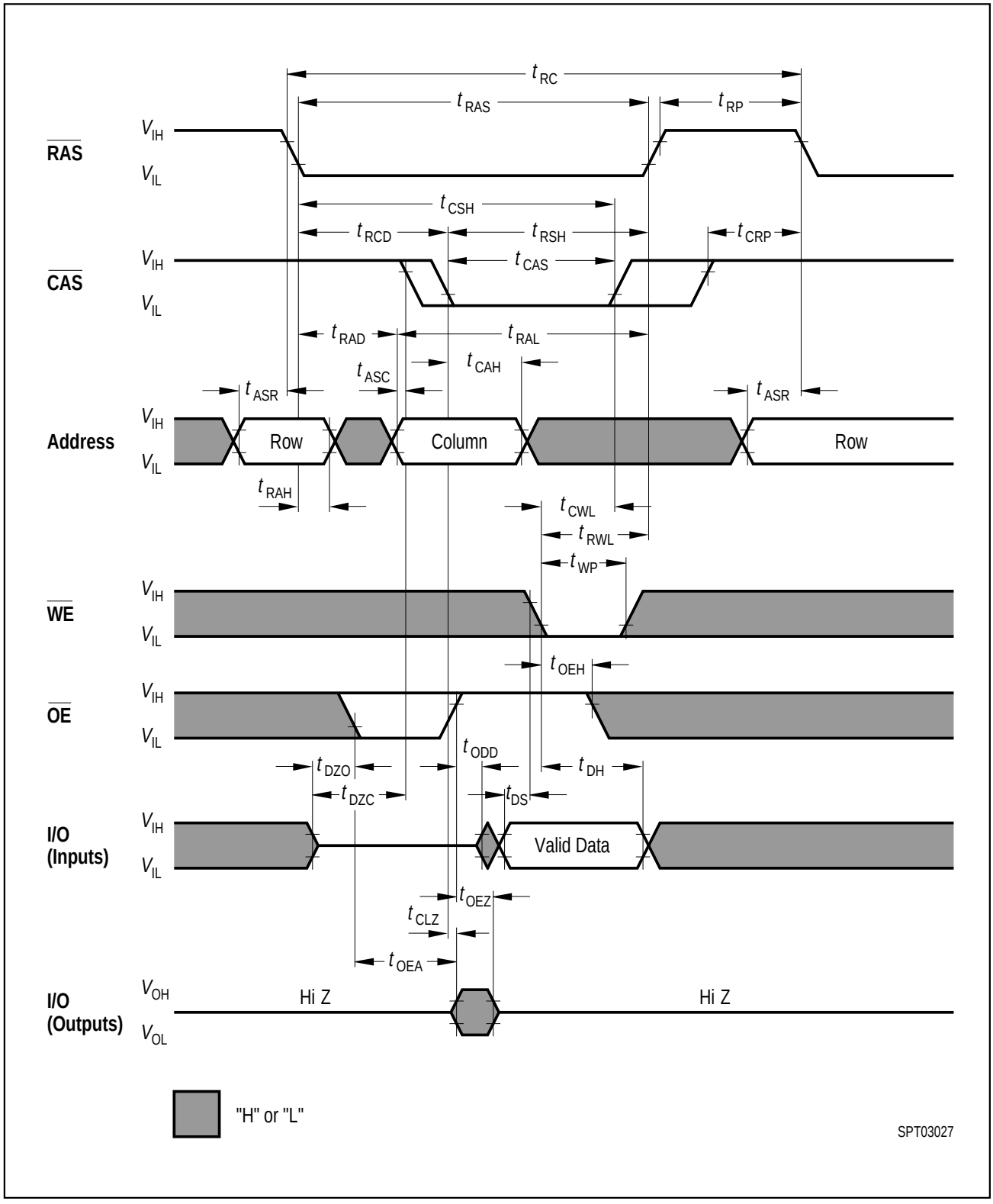
1. All voltages are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).
5. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 100 pF and at V_{OH} = 2.0 V (I_{OH} = – 2 mA), V_{OL} = 0.8 V (I_{OL} = 2 mA).
9. Operation within the $t_{RCD\ (MAX.)}$ limit ensures that $t_{RAC\ (MAX.)}$ can be met. $t_{RCD\ (MAX.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (MAX.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD\ (MAX.)}$ limit ensures that $t_{RAC\ (MAX.)}$ can be met. $t_{RAD\ (MAX.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (MAX.)}$ limit, then access time is controlled by t_{AA}.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
13. Either t_{DZC} or t_{DZO} must be satisfied.
14. Either t_{CDD} or t_{ODD} must be satisfied.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (MIN.)}$, $t_{CWD} > t_{CWD\ (MIN.)}$, $t_{AWD} > t_{AWD\ (MIN.)}$ and $t_{CPWD} > t_{CPWD\ (MIN.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAH
tASC
tASR
tASR
Address
Row
Column
Row
tRAH
tRCH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tOFF
tCAC
tCLZ
tOEZ
VOH
VOL
I/O
(Outputs)
Hi Z
Valid Data OUT
Hi Z
tRAC
"H" or "L"
SPT03025

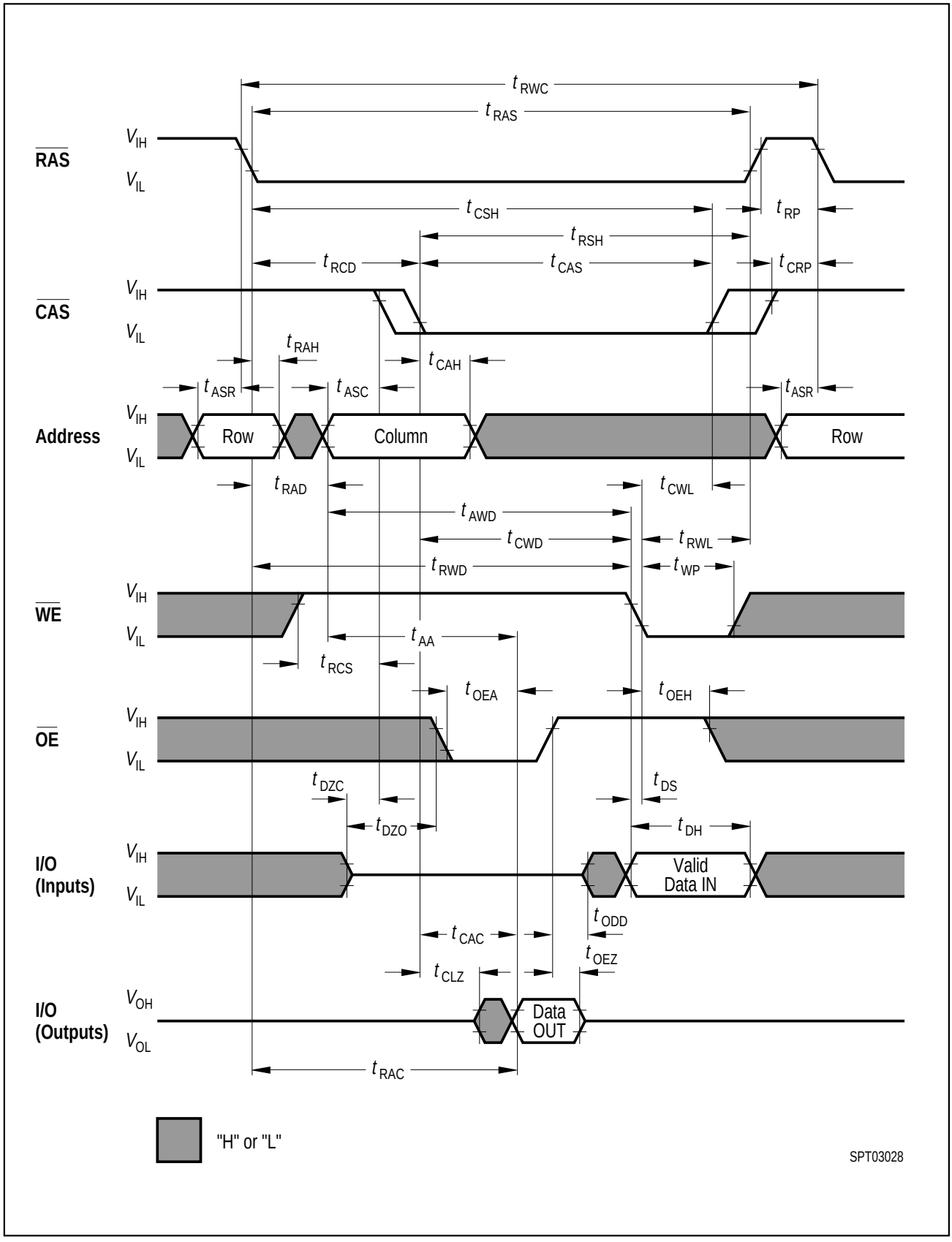
Read Cycle



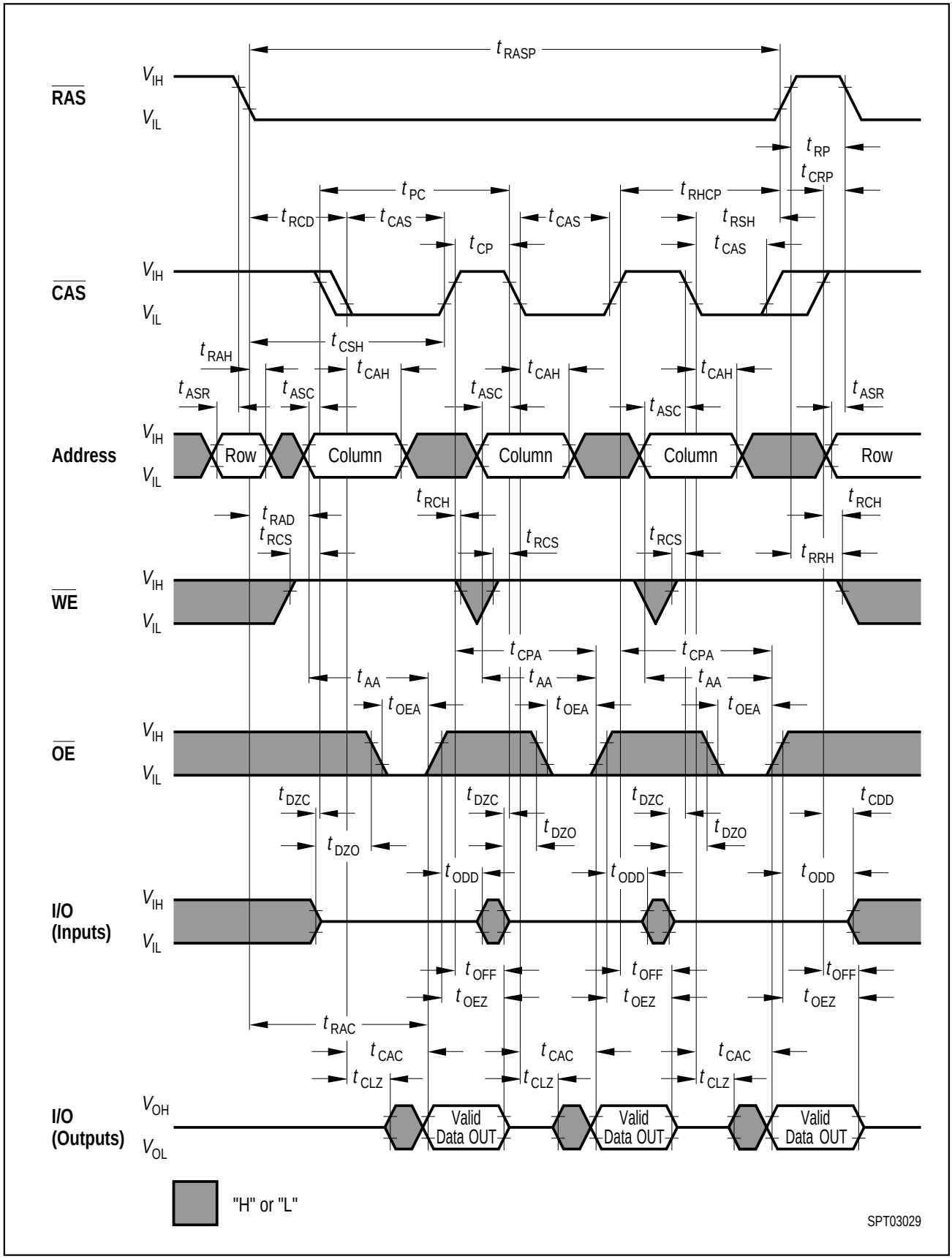
Write Cycle (Early Write)



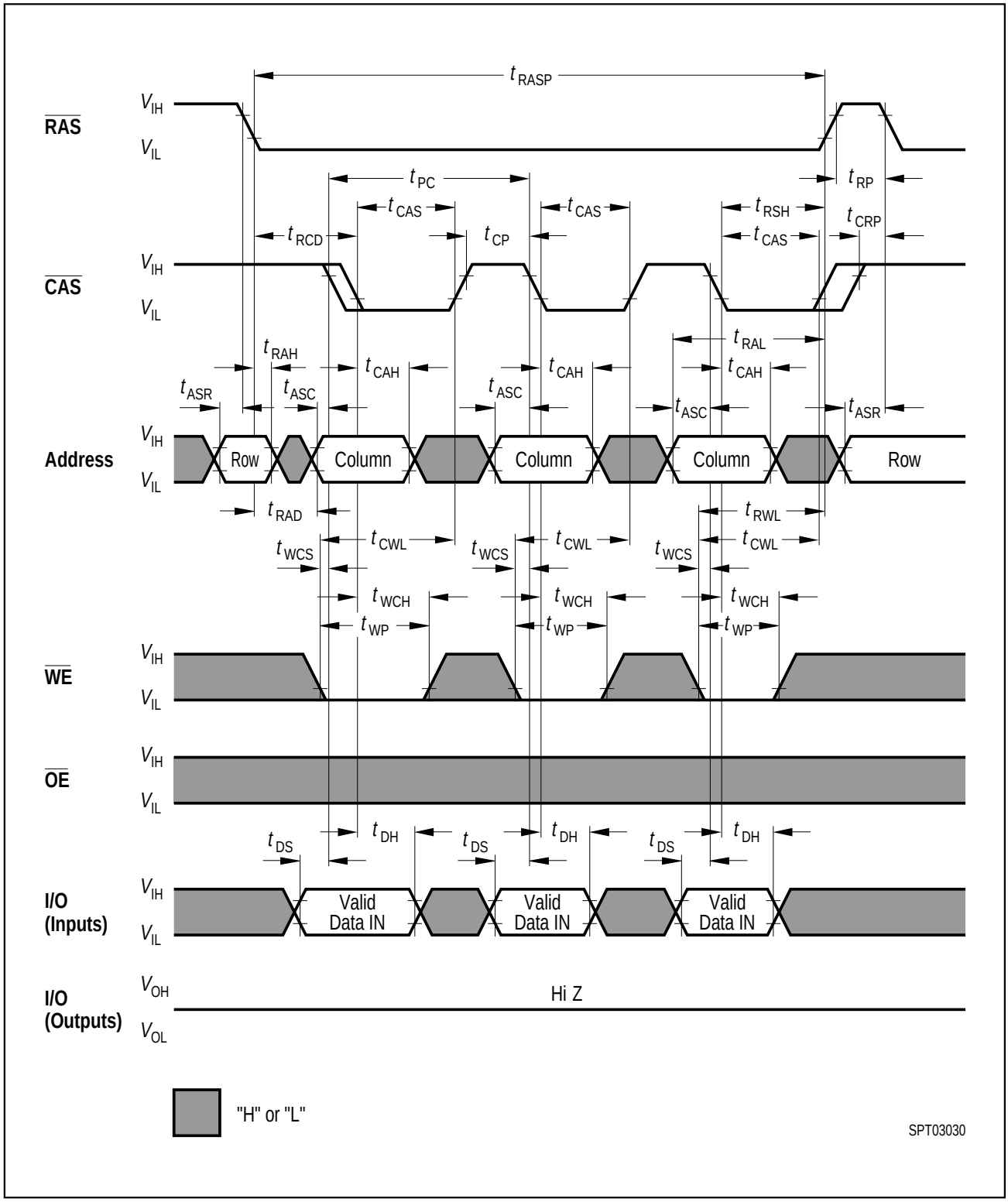
Write Cycle (OE Controlled Write)



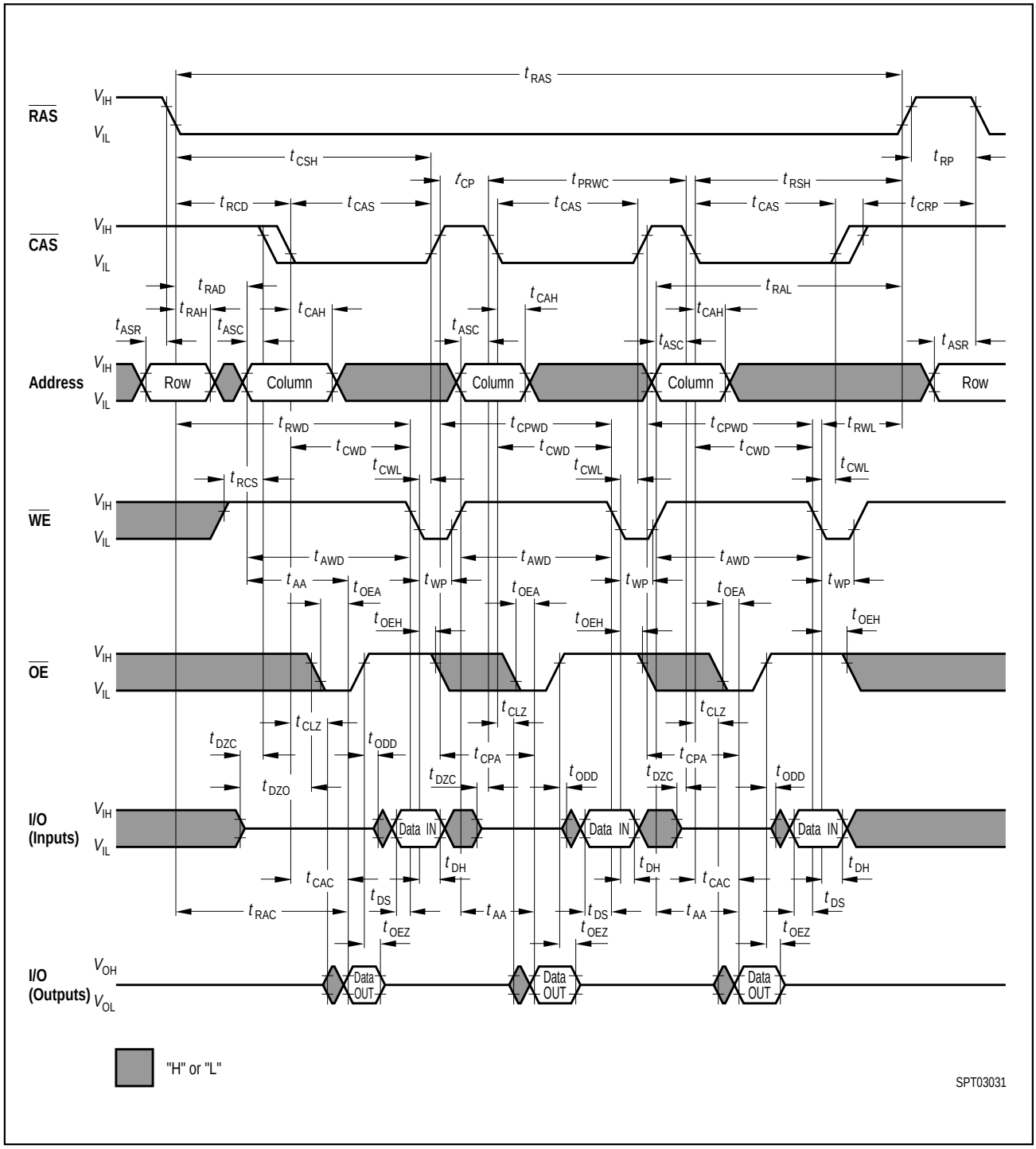
Read-Write (Read-Modify-Write) Cycle



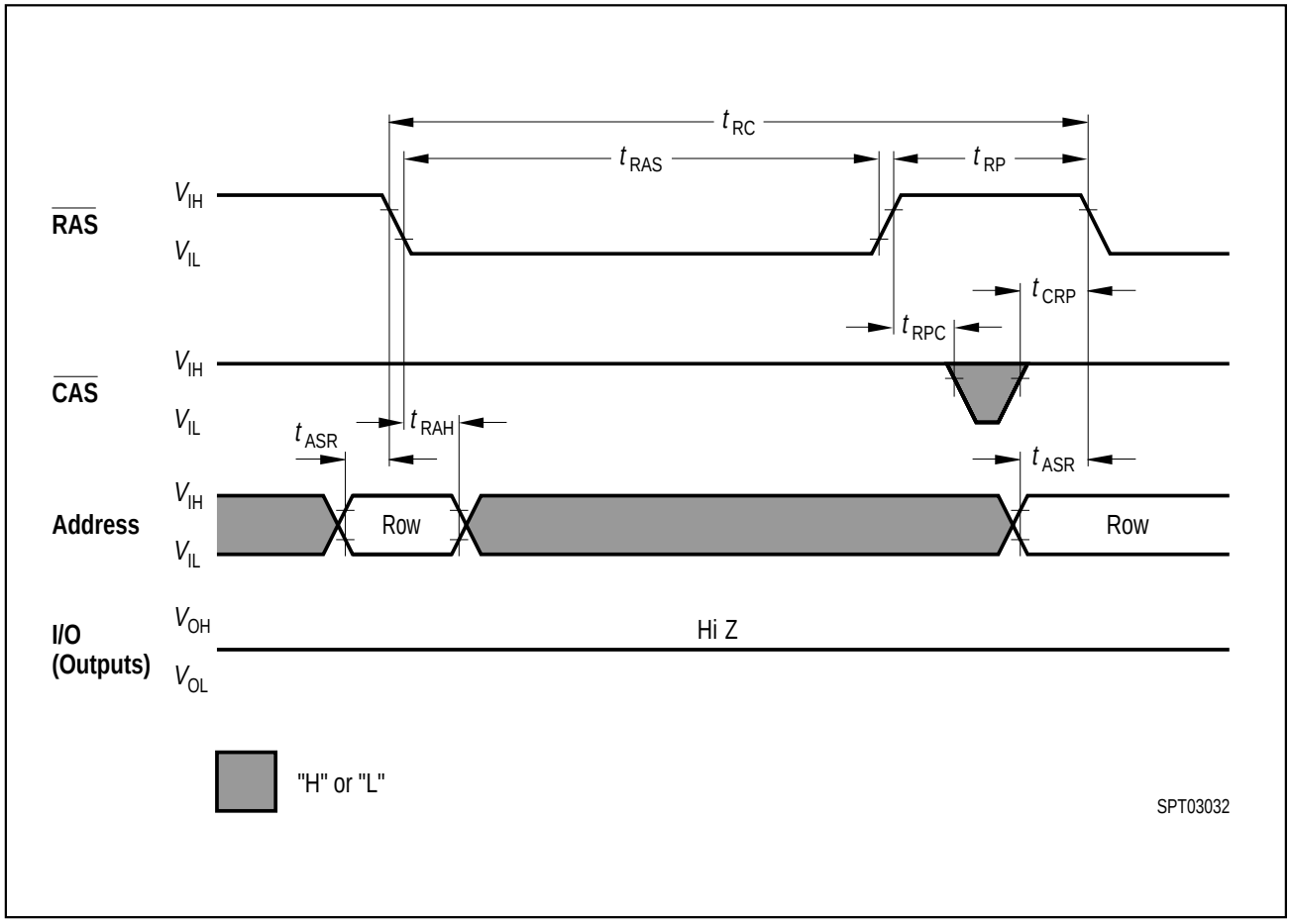
Fast Page Mode Read Cycle



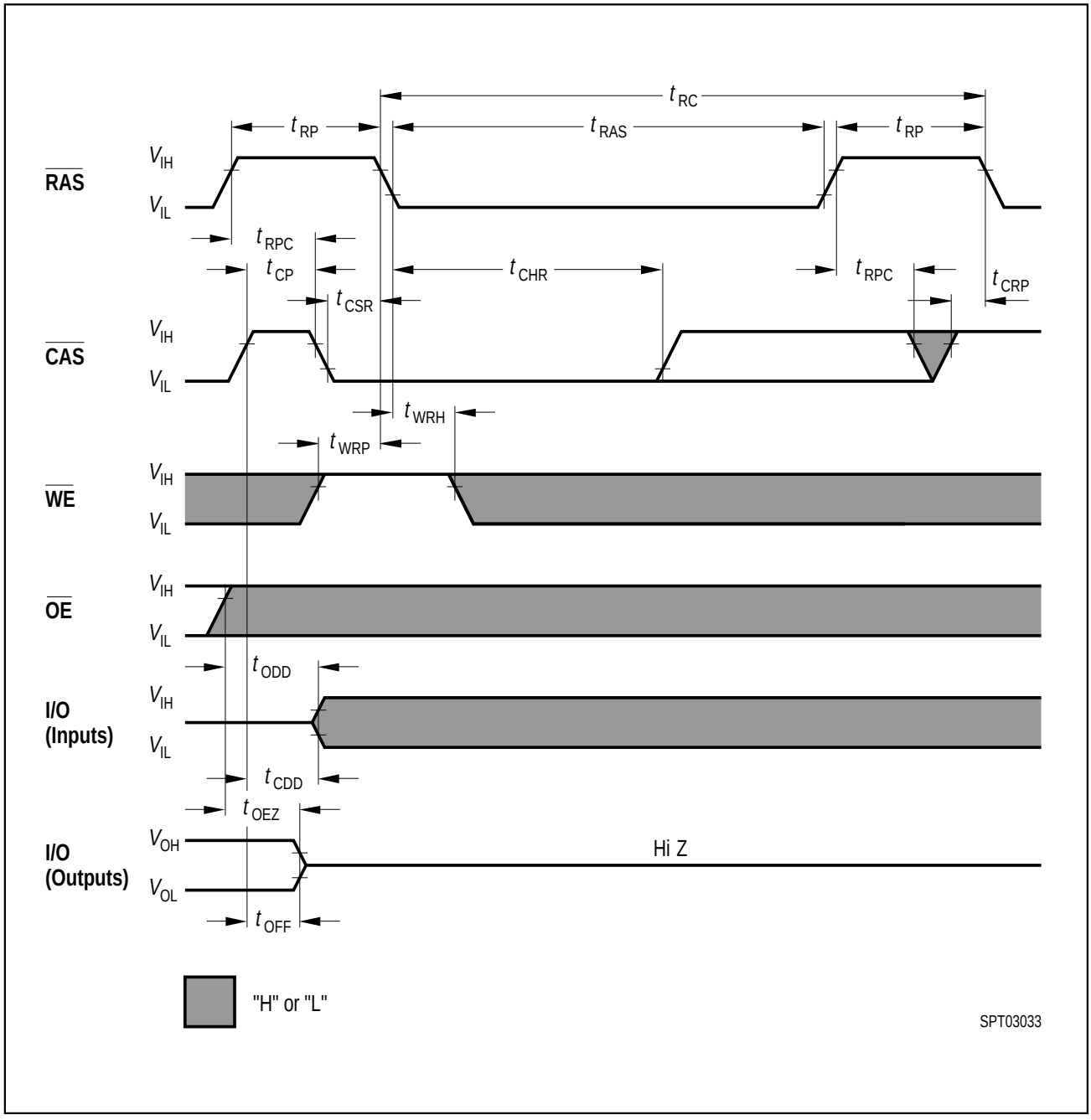
Fast Page Mode Early Write Cycle



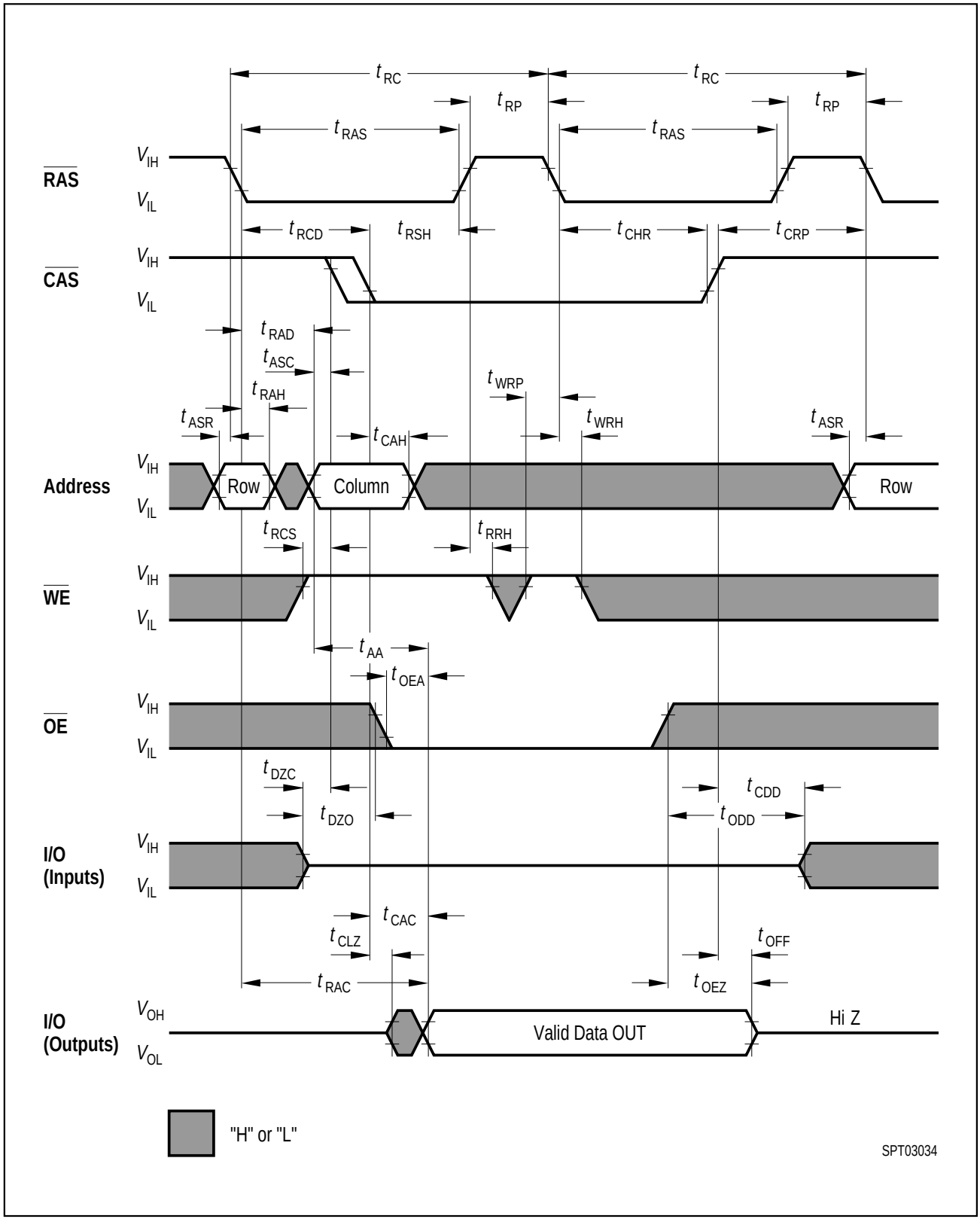
Fast Page Mode Read-Modify-Write Cycle



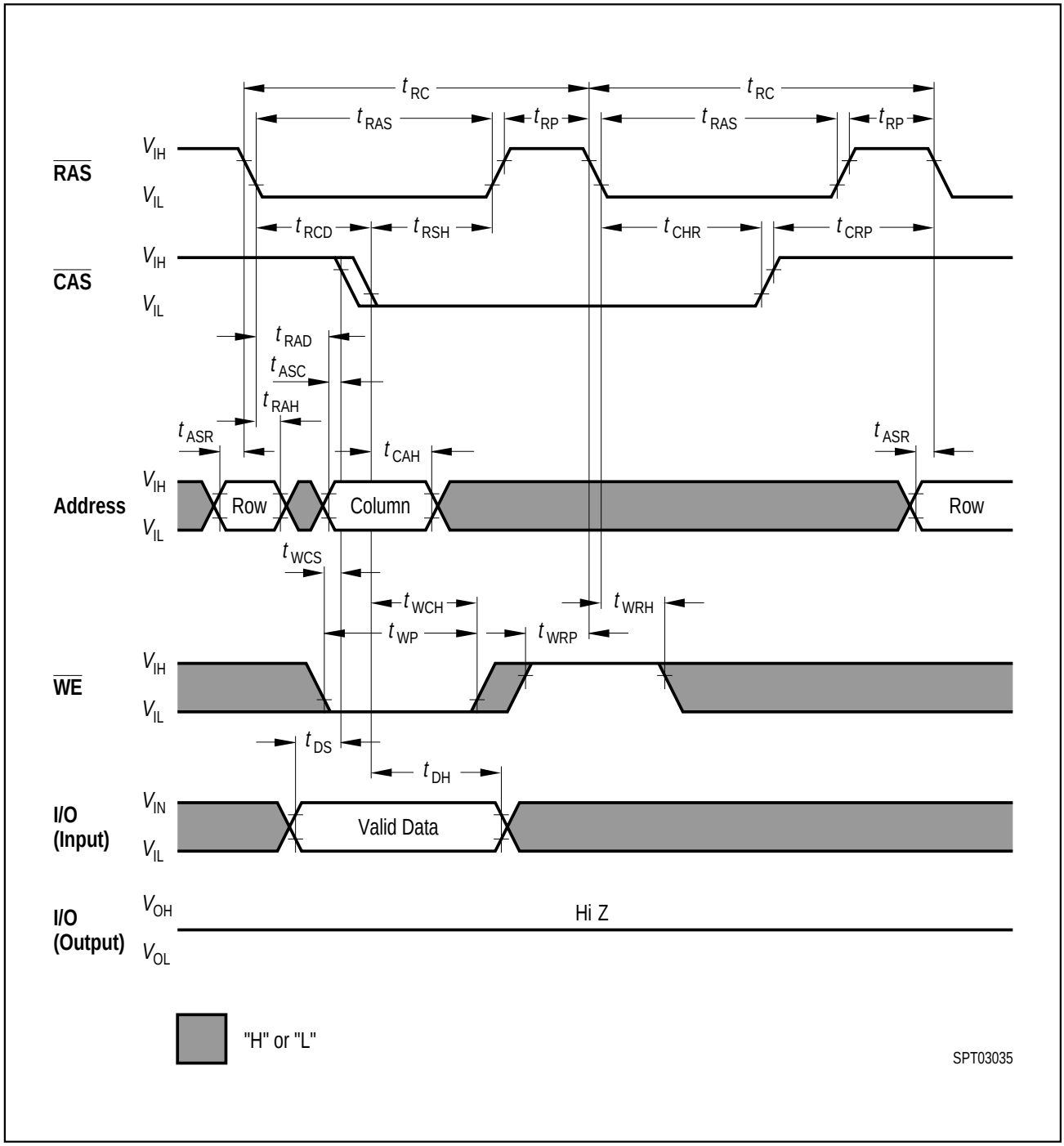
RAS-Only Refresh Cycle



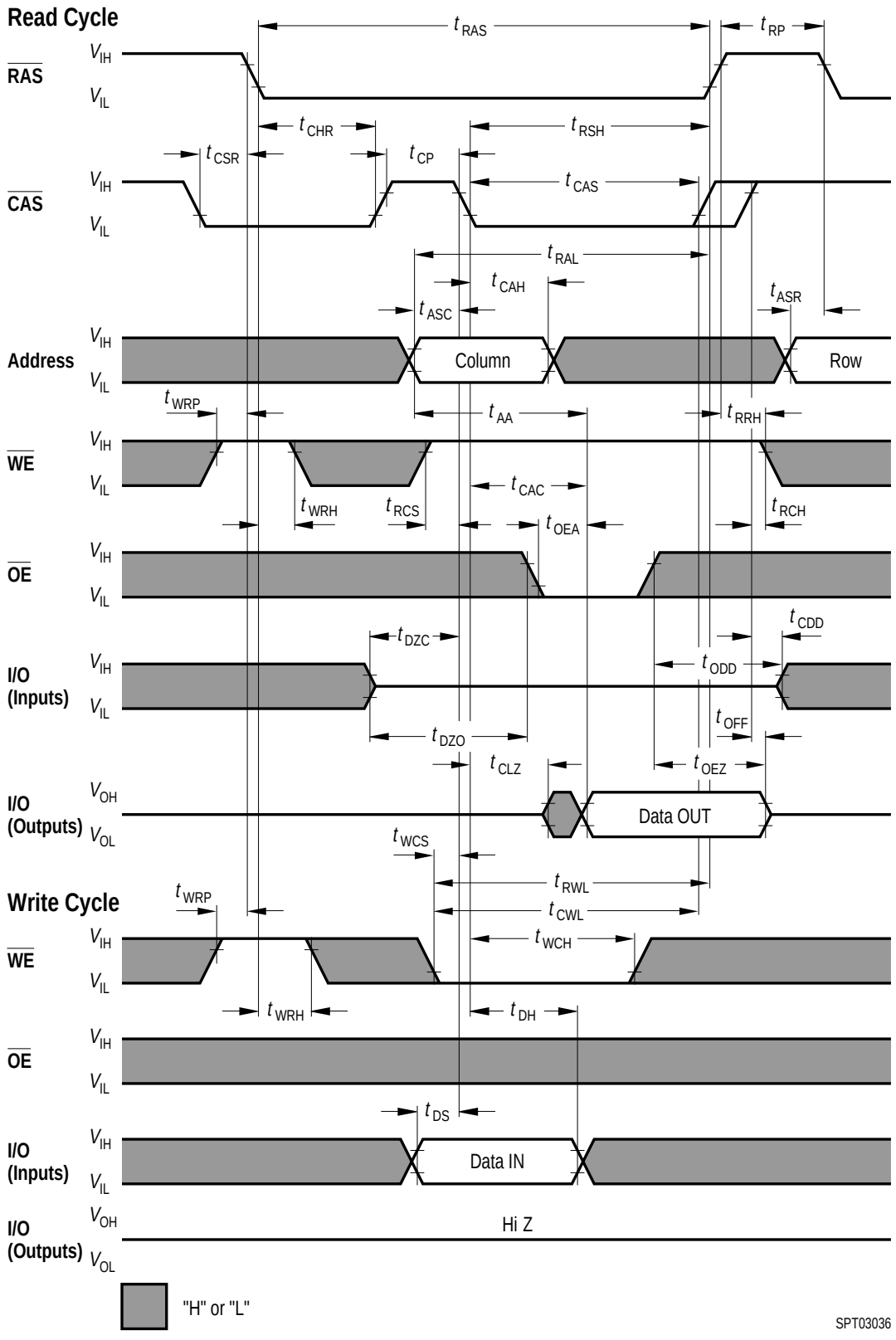
CAS-Before-RAS Refresh Cycle



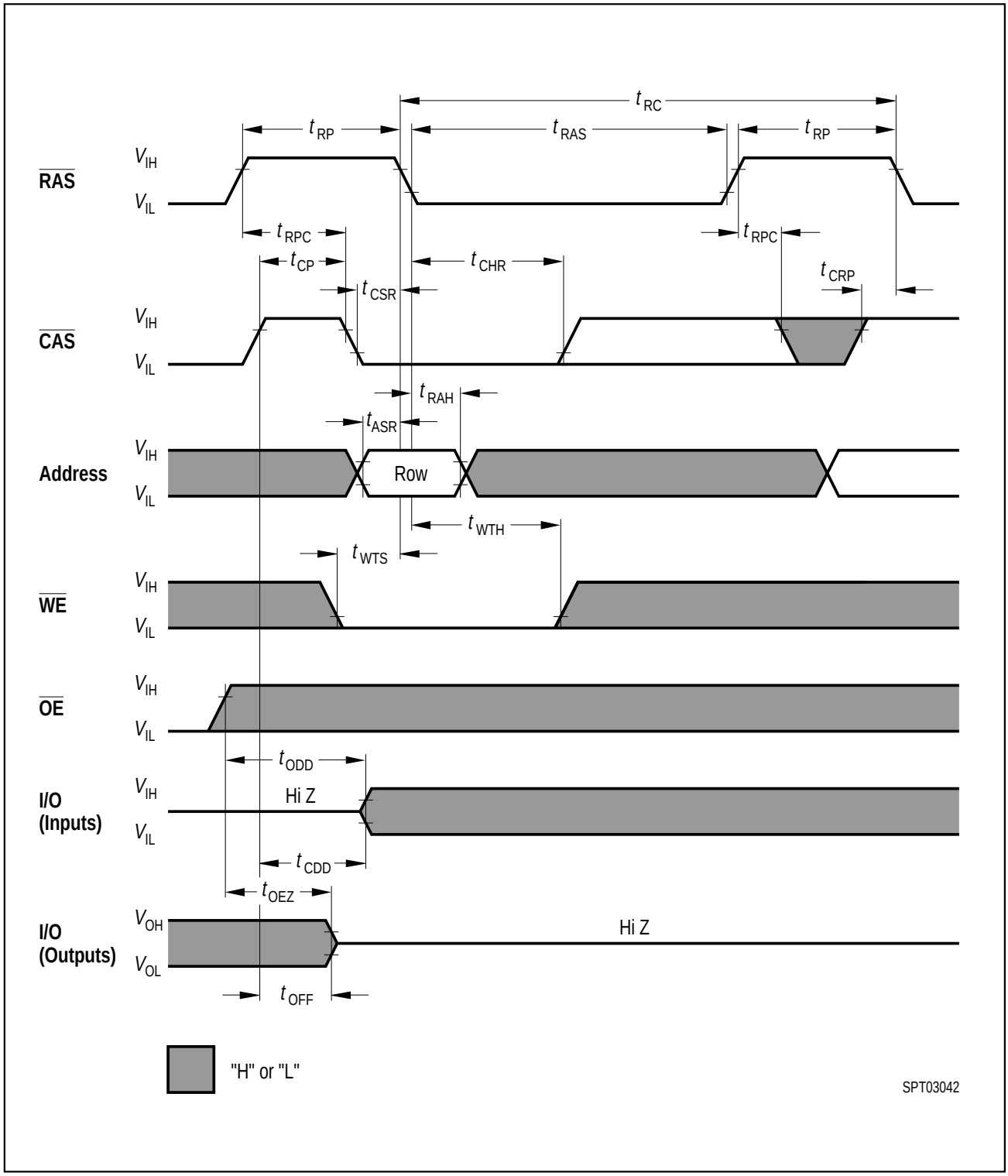
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

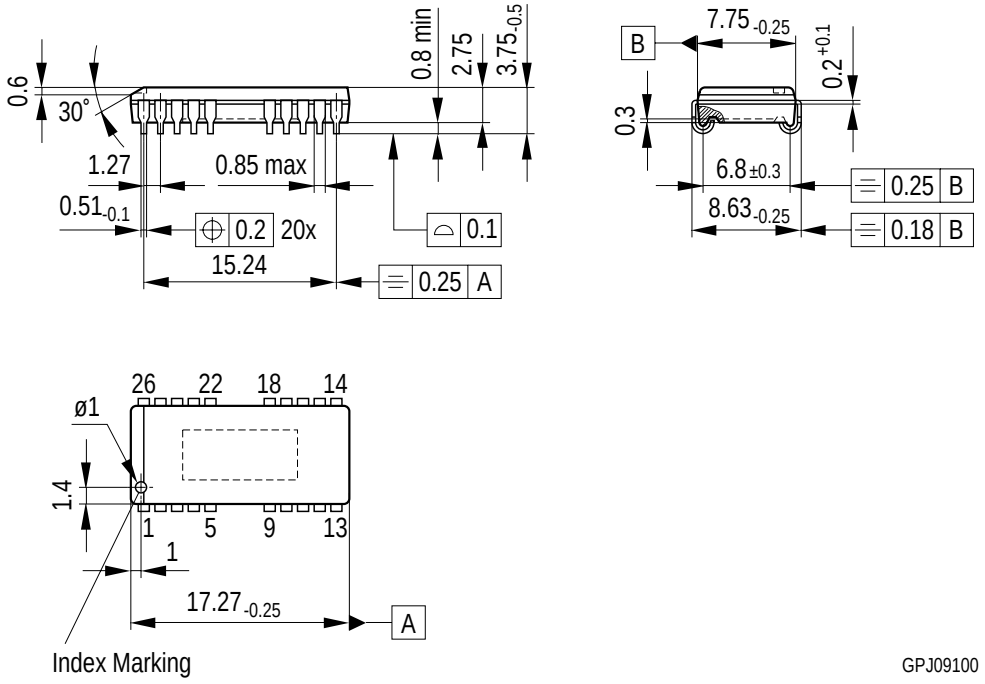
As the HYB 314400BJ is organized internally as 512k × 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note that in the 1M × 4 version the test time is reduced by 1/2 for a linear test pattern.

In a test mode “write” the data from each I/O1 pin is written into eight bits simultaneously (all “1” or all “0”).The I/O2 - I/O4 inputs are not used for writing in test mode. In test mode “read” each I/O output is used for indicating the test mode result. If the internal eight bits are equal, the I/O would indicate a “1”. If they were not equal, the I/O would indicate a “0”. Note that in test mode "read" I/O1-I/O3 are always driven to “ones”, i.e. all outputs will be “1” for a test mode “pass”. The WCBR cycle ($\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$) puts the device into test mode. To exit from test mode, a “$\overline{CAS}$-before-$\overline{RAS}$ refresh”, “$\overline{RAS}$-only refresh” or “Hidden refresh” can be used.

Addresses A10R, A10C and A0C are don‘t care during test mode.

Package Outlines

Plastic Package, P-SOJ-26/20-2 (SMD)
(Plastic small outline J-leaded)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm