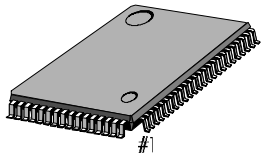
DIGITAL SIGNAL PROCESSOR

The KS9286B is a CMOS integrated circuit designed for the Digital Audio Signal Processor for Compact Disc Player. It is a monolithic IC that builts-in 16-bit Digital Analog Convertor, ESP Interface and Digital De-emphasis additional conventional DSP function.

80-QFP-1420C



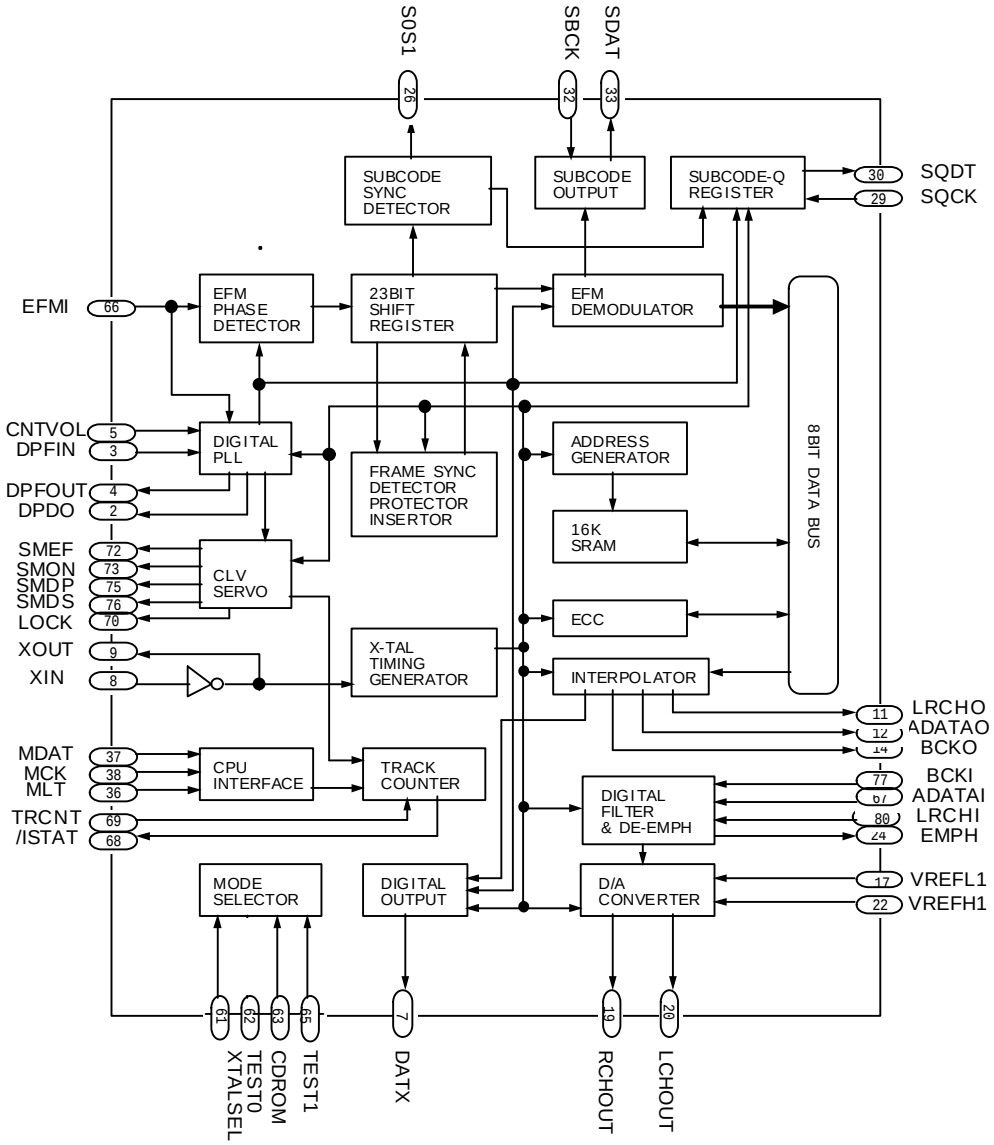
FEATURES

- EFM data demodulation
- Frame sync detection/protection/insertion
- Powerful error correction (C1: 2error, C2: 4erasure)
- Interpolation
- 8fs digital filter (51th+13th+9th)
- Subcode data serial output
- CLV servo controller
- Micom interface
- Digital audio output
- Digital de-emphasis
- ESP interface
- Built-in 16K SRAM
- Built-in Digital PLL
- Double speed play available
- Built-in 16-bit D/A converter
- Operating Voltage range
  KS9286B : 5V
  KS9286B-L : 3.4V

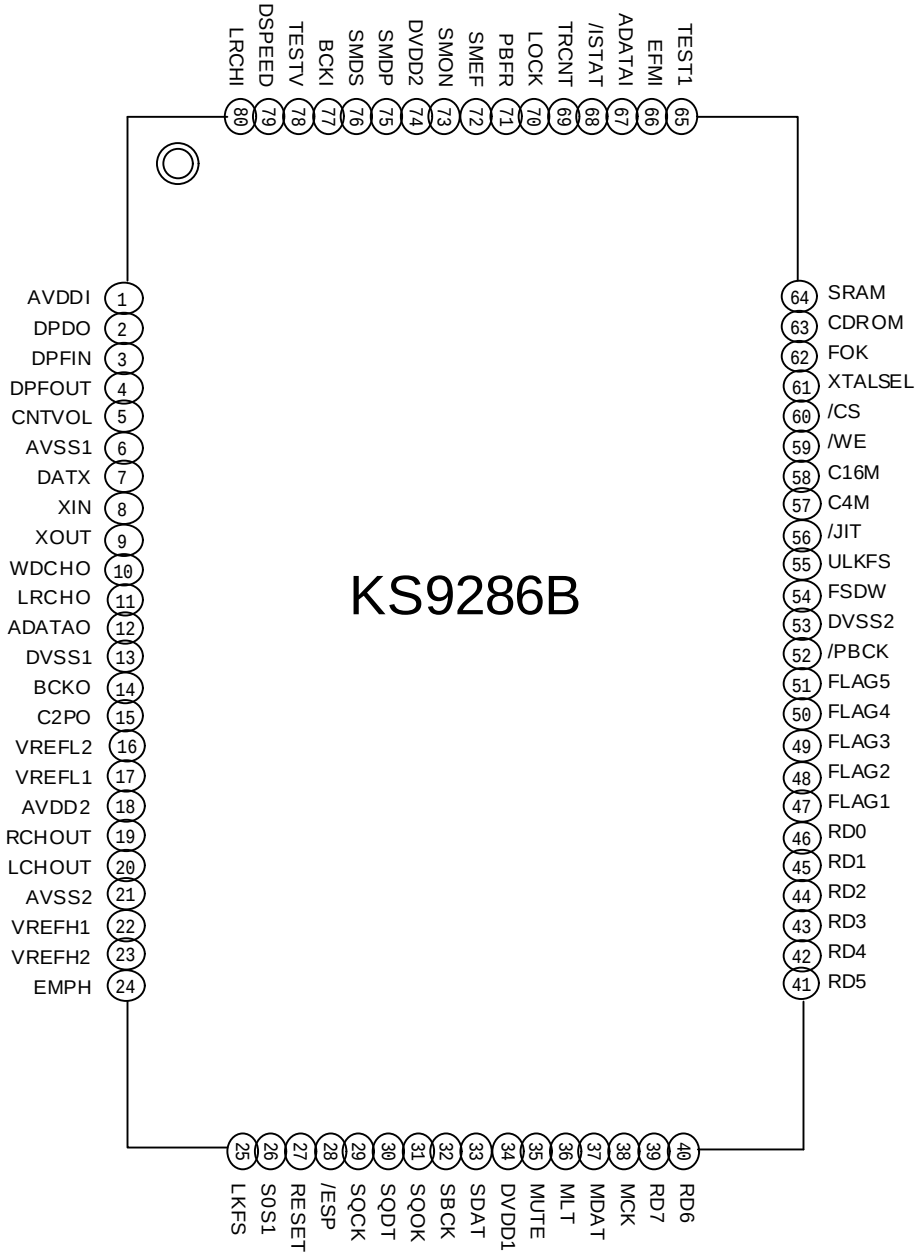
ORDERING INFORMATION

Device	Package	Tempe. Range
KS9286B	80-QFP-1420C	-20°C ~ +75°C
KS9286B-L		

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	SYMBOL	IO	DESCRIPTION
1	AVDD1	-	Analog VCC1
2	DPDO	O	Charge pump output for Digital PLL
3	DPFIN	I	Filter input for Digital PLL
4	DPFOUT	O	Filter output for Digital PLL
5	CNTVOL	I	VCO control voltage for Digital PLL
6	AVSS1	-	Analog Ground1
7	DATX	O	Digital Audio output data
8	XIN	I	X'tal oscillator input
9	XOUT	O	X'tal oscillator output
10	WDCHO	O	Word clock output of 48bit/Slot (88.2KHz)
11	LRCHO	O	Channel clock output of 48 bit/Slot (44.1KHz)
12	ADATAO	O	Serial audio data output of 48 bit/Slot (MSB first)
13	DVSS1	-	Digital Ground1
14	BCKO	O	Audio data bit clock output of 48 bit/Slot (2.1168MHz)
15	C2PO	O	C2 Pointer for output audio data
16	VREFL2	I	Input terminal2 of reference voltage "L" (Floating)
17	VREFL1	I	Input terminal1 of reference voltage "L" (GND connection)
18	AVDD2	-	Analog VCC2
19	RCHOUT	O	Right-Channel audio output through D/A converter
20	LCHOUT	O	Left-Channel audio output through D/A converter
21	AVSS2	-	Analog ground2
22	VREFH1	I	Input terminal1 of reference voltage "H" (VDD connection)
23	VREFH2	I	Input terminal2 of reference voltage "H" (Floating)
24	EMPH	O	H: Emphasis ON, L: Emphasis OFF
25	LKFS	O	The Lock Status output of frame sync
26	S0S1	O	Output of subcode sync signal(S0+S1)
27	RESET	I	System reset at "L"
28	/ESP	I	ESP function ON/OFF control ("L": ESP function ON, "H": ESP function OFF)
29	SQCK	I	Clock for output Subcode-Q data

PIN DESCRIPTION (continued)

PIN NO	SYMBOL	IO	DESCRIPTION
30	SQDT	O	Serial output of Subcode-Q data
31	SQOK	O	The CRC (Cycle Redundancy Check) check result signal output of Subcode-Q
32	SBCK	I	Clock for output subcode data
33	SDAT	O	Subcode serial data output
34	DVDD1	-	Digital VDD1
35	MUTE	I	Mute control input ("H": Mute ON)
36	MLT	I	Latch Signal Input from Micom (Schmit Trigger)
37	MDAT	I	Serial data input from Micom (Schmit Trigger)
38	MCK	I	Serial clock input from Micom (Schmit Trigger)
39	RD7	I/O	SRAM data I/O port 8 (MSB)
40	RD6	I/O	SRAM data I/O port 7
41	RD5	I/O	SRAM data I/O port 6
42	RD4	I/O	SRAM data I/O port 5
43	RD3	I/O	SRAM data I/O port 4
44	RD2	I/O	SRAM data I/O port 3
45	RD1	I/O	SRAM data I/O port 2
46	RD0	I/O	SRAM data I/O port 1 (LSB)
47	FLAG1	I/O	Monitoring output for error correction (RA0)
48	FLAG2	I/O	Monitoring output for error correction (RA1)
49	FLAG3	I/O	Monitoring output for error correction (RA2)
50	FLAG4	I/O	Monitoring output for error correction (RA3)
51	FLAG5	I/O	Monitoring output for error correction (RA4)
52	/PBCK	I/O	Output of VCO/2 (4.3218MHz) (RA5)
53	DVSS2	I/O	Digital ground 2
54	FSDW	I/O	Window or unprotected frame sync (RA6)
55	ULKFS	I/O	Frame sync protection state (RA7)
56	/JIT	I/O	Display of either RAM overflow or underflow for $\pm$ 4 frame jitter margin (RA8)
57	C4M	I/O	Only monitoring signal (4.2336MHz) (RA9)
58	C16M	I/O	16.9344MHz signal output(RA10)
59	/WE	I/O	Terminal for test
60	/CS	I/O	Terminal for test

PIN DESCRIPTION (continued)

PIN NO	SYMBOL	IO	DESCRIPTION
61	XTALSEL	I	Mode Selection1 (H: 33.8688MHz, L: 16.9344MHz)
62	FOK	I	SERVO FOK Signal input terminal
63	CDROM	I	Mode Selection2 (H: CD-ROM, L: CDP)
64	SRAM	I	TEST input terminal (GND connection)
65	TEST1	I	TEST input terminal (GND connection)
66	EFMI	I	EFM signal input
67	ADATAI	I	Serial audio data input of 48 bit/Slot (MSB first)
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking counter input signal
70	LOCK	O	Output signal of LKFS condition sampled PBFR/16 (if LKFS is "H", LOCK is "H", if LKFS is sampled "L" at least 8 times by PBFR/16, LOCK is "L".)
71	PBFR	O	Write frame clock (Lock: 7.35KHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spindle servo
74	DVDD2	-	Digital VDD2
75	SMDP	O	Spindle Motor drive (Rough control in the SPEED mode, Phase control in the PHASE mode)
76	SMDS	O	Spindle Motor drive (Velocity control in the PHASE mode)
77	BCKI	I	Audio data bit clock input of 48 bit/Slot (2.1168MHz)
78	TESTV	I	TEST input terminal (GND connection)
79	DSPEED	I	TEST input terminal (VDD connection)
80	LRCHI	I	Channel clock input of 48 bit/Slot (44.1KHz)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VI	-0.3 ~ 7.0	V
Output Voltage	VO	-0.3 ~ 7.0	V
Operating Temperature	TOPR	-20 ~ 75	^{o}C
Storage Temperature	TSTG	-40 ~ 125	^{o}C

ELECTRICAL CHARACTERISTIC

1. DC Characteristic
(Vcc=5V, Vss=0V, Ta=25^{o}C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
'H' INPUT VOLTAGE1	VIH(1)	(Note1)	0.7VDD	-	-	V
'L' INPUT VOLTAGE1	VIL(1)	(Note1)	-	-	0.3VDD	V
'H' INPUT VOLTAGE2	VIH(2)	(Note2)	0.8VDD	-	-	V
'L' INPUT VOLTAGE2	VIL(2)	(Note2)	-	-	0.2VDD	V
'H' OUTPUT VOLTAGE1	VOH(1)	IOH=-1mA (Note3)	VDD-0.5	-	VDD	V
'L' OUTPUT VOLTAGE1	VOL(1)	IOL=1mA (Note3)	0	-	0.4	V
'H' OUTPUT VOLTAGE2	VOH(2)	IOH=-1mA (Note4)	VDD-0.5	-	VDD	V
'L' OUTPUT VOLTAGE2	VOL(2)	IOL=2mA (Note4)	0	-	0.4	V
INPUT LEAK CURRENT	ILKG	VI=0~VDD (Note5)	-5	-	5	uA
THREE STATE OUTPUT LEAK CURRENT	IO(LKG)	VO=0~VDD (Note6)	-5	-	5	uA

(Note1) Related pins : XTALSEL, TEST0, CDROM, SRAM, TEST1, EFMI, ADATAI, BCKI, DSPEED & LRCHI

(Note2) Related pins : All bi-direction pins & RESET, MLT, MCK, MDAT, MUTE, TRCNT

(Note3) Related pins : All output pins except (Note4) and OSCILATOR, DPFOUT

(Note4) Related pins : /ISTAT

(Note5) Related pins : XIN

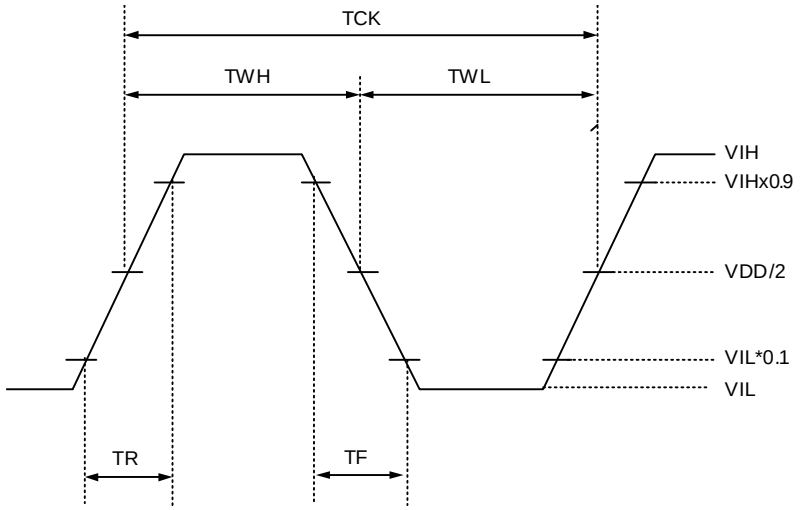
(Note6) Related pins : SMEF, SMDP, SMDS & DPDO

2. AC CHARACTERISTIC

A. XIN (When the pulse is input)

(Vcc=5V, Vss=0V, Ta=25°C, unless otherwise specified)

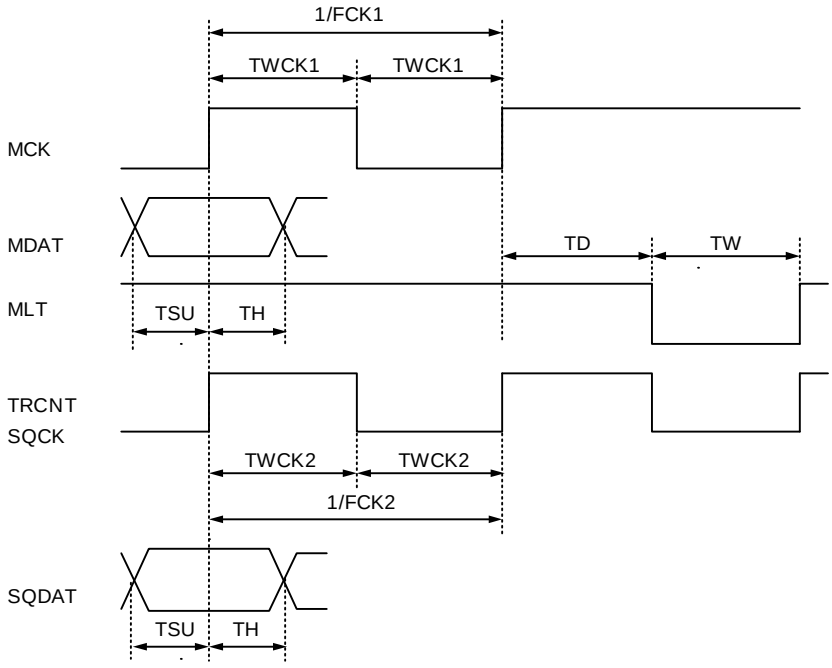
Characteristic	Symbol	Min	Typ	Max	UNIT
'H' LEVEL PULSE WIDTH	TWH	13	-	-	ns
'L' LEVEL PULSE WIDTH	TWL	13	-	-	ns
PULSE FREQUENCY	TCK	26	-	-	ns
INPUT 'H' LEVEL	VIH	VDD-1.0	-	-	V
INPUT 'L' LEVEL	VIL	-	-	0.8	V
RISING & FALLING TIME	TR,TF	-	-	8	ns



B. MCK, MDAT, MLT & TRCNT

(Vcc=5V, Vss=0V, Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
CLOCK FREQUENCY	FCK1	-	-	1	MHz
CLOCK PULE WIDTH	TW	300	-	-	ns
SETUP TIME	TSU	300	-	-	ns
HOLD TIME	TH	300	-	-	ns
DELAY TIME	TD	300	-	-	ns
LATCH PULSE WIDTH	TWCK1	300	-	-	ns
TRCNT, SQCK FREQUENCY	FCK2	-	-	1	MHz
TRCNT, SQCK PULSE WIDTH	TWCK2	300	-	-	ns



SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

1. Micom Interface

The data inputted from Micom is inputted to MDAT and transfered by MCK, and the inputted signal is loaded to control register by means of MLT. The timing chart is as follows.

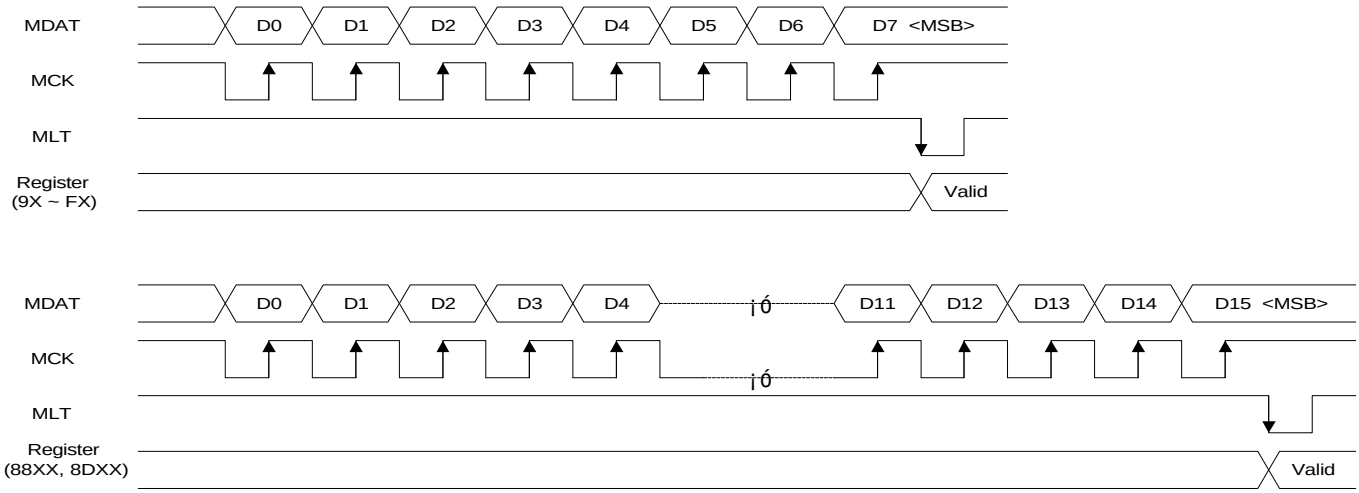


Fig.1. Micom data input timing chart

CONTROL REGSTER	COMMENT	ADDRESS D7~D4	DATA				/ISTAT PIN
			D3	D2	D1	D0	
CNTL-Z	DATA CONTROL	9X	ZCMT	-	NCLV	CRCQ	S0S1
CNTL-S	FRAME SYNC PROTECTION ATTENUATION CONTROL	AX	FSEM	FSEL	WSEL	ATTM	LKFS
CNTL-L	TRACKING COUNTER LOWER 4 BITS	BX	TRC3	TRC2	TRC1	TRC0	/COMPLETE
CNTL-U	TRACKING COUNTER UPPER 4 BITS	CX	TRC7	TRC6	TRC5	TRC4	/COUNT
CNTL-W	CLV CONTROL	DX	-	WB	WP	GAIN	FOK
CNTL-C	CLV-MODE	EX	CM3	CM2	CM1	CM0	/(Pw ≥ 64)
CNTL-D	DOUBLE-SPEED	FX	0	0	DS1	DS2	TRCNT

CONTROL REGSTER	COMMENT	ADDRESS D15~D8	DATA								/ISTAT PIN
			D7	D6	D5	D4	D3	D2	D1	D0	
CNTL-F	FUNCTION CONTROL	88XX	-	-	DEEM	ERA_ OFF	-	-	-	-	Hi-Z
CNTL-H	ESP,MONITOR PIN CONTROL	8DXX	-	-	-	-	-	-	ESP_ ON	DUMB	Hi-Z

Table 1. Control register & data

* Send the 9X, AX, DX, FX command when output the S0S1, LKFS, FOK, TRCNT signal to /ISTAT pin also just send MDAT, MCK except MLT

1) CNTL-Z REGISTER

It is a register to control zero cross mute of audio data, phase terminal control, phase servo control and having or not of CRCF in data SQDT.

		DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is OFF	Zero cross mute is ON
-	D2	-	-
NCLV	D1	The phase servo is acted by frame sync	The phase servo is controlled by base counter
CRCQ	D0	SQDT outputs except for SQOK	SQDT=CRCF when S0S1='H'

Table 2. CNTL-Z register & data

2) CNTL-S REGISTER

It is a register to control frame sync protection and attenuation.

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	± 3
1	± 7

ATTM	MUTE	dB
0	0	0
0	1	- ∞
1	0	-12
1	1	-12

Table 3. CNTL-S register & data

3) CNTL-L, U REGISTER

After the counter of track that must be counted is inputted from Micom, the data is loaded to tracking counter by CNTL-L, U register.

4) CNTL-W REGISTER

It is a register to control CLV-Servo.

		DATA=0	DATA=1	COMMENT
-	D3	-	-	-
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed or Hspeed-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period control during speed-mode
GAIN	D0	-12dB	0dB	SMDP gain control during speed or Hspeed-mode

Table 4. CNTL-W register & data

5) CNTL-C REGISTER

It is a register to control CLV-Mode.

MODE	D7~D4	D3~D0	SMDP	SMSD	SMEF	SMON
FORWARD	1110	1000	H	Hi-Z	L	H
REVERSE		1010	L	Hi-Z	L	H
SPEED		1110	SPEED-MODE	Hi-Z	L	H
HSPEED		1100	HSPEED-MODE	Hi-Z	L	H
PHASE		1111	PHASE-MODE	PHASE-MODE	Hi-Z	H
XPHSP		0110	SPEED or PHASE-MODE	Hi-Z or PHASE-MODE	L, Hi-Z	H
VPHSP		0101	SPEED or PHASE-MODE	Hi-Z or PHASE-MODE	L, Hi-Z	H
STOP		0000	L	Hi-Z	L	lL

Table 5. CNTL-C register & data

6) CNTL-D REGISTER

It is a register to control normal speed mode and double speed mode.

MODE	D7~D4	D3~D0	COMMENT
NORMAL	1111	0000	Normal Speed
DOUBLE		0011	Double Speed

Table 6. CNTL-D register & data

7) CNTL-F REGISTER

It is a register to control De-emphasis and ECC Erasure correction.

		DATA = 0	DATA = 1
DEEM	D5	Internal De-emphasis Filter operation OFF	Internal De-emphasis Filter operation ON
ERA_OFF	D4	ECC Erasure correction ON	ECC Erasure correction OFF

Table 6. CNTL-F register & data

8) CNTL-H RESISTER

It isa resister to control ESP interface and Monitor pin

		DATA = 0	DATA = 1
ESP_ON	D1	ESP Interface Disable	ESP Interface Enable
DUMB	D0	Monitor Pin Output Enable	Monitor Pin Output Disable

Note) Monitor pin : FLAG1 ~ FLAG5, /PBCK, FSDW, ULKFS, C16M, PBFR

Table 7. CNTL-H register & data

2. Tracking Counter Block

This block is used to improve the Track-jump characteristics.

The numbers of tracks that are to be jumped (inputted from Micom) are loaded into either register CNTL-L or CNTL-U at the rising edge of MLT. When the address is set in CNTL-L, the signal /COMPLETE is output in /ISTAT Pin, and when the address is set in CNTL-U, the signal /COUNT is output.

The following is timing chart of tracking counter block.

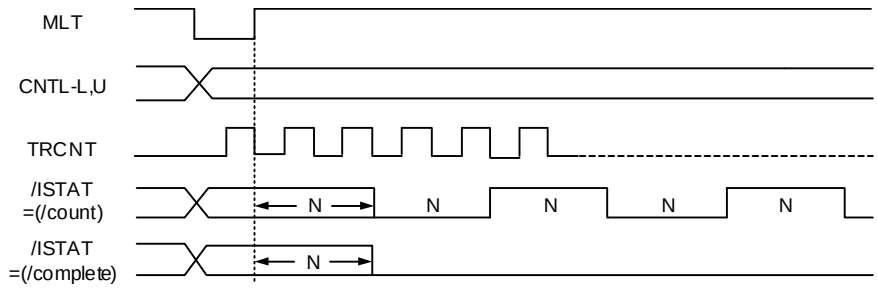


Fig.2. Tracking counter timing chart

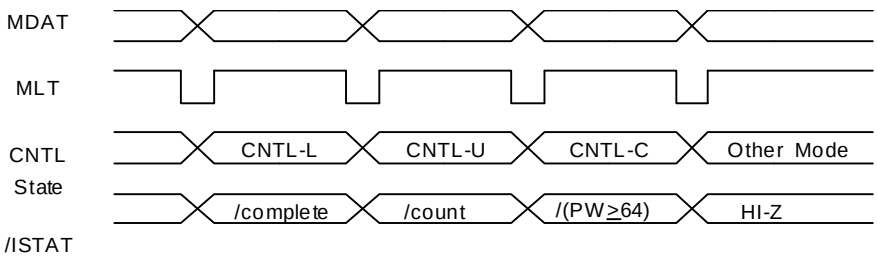


Fig.3. /ISTAT output signal according to CNTL Register

3. EFM DEMODULATION BLOCK

The EFM block consists of EFM demodulator circuit which demodulates EFM data obtained from a disc, EFM phase detector circuit and control signal generator circuit etc.

1) EFM Demodulator

The modulated 14-bit data is demodulated to 8-bit data through the demodulator circuit.

There are two kinds of demodulated data, one is subcode data and the other is audio data, and the subcode data is inputted into subcode block and the audio data is written into built-in 16K SRAM and performed error correction.

2) Frame SYNC Detector, Protector and Inserter

A. Frame SYNC Detector

The data consists of frame unit, that is, it consists of frame SYNC, subcode data, audio data and redundancy data etc.

The frame SYNC is detected in order to maintain the synchronization.

B. Frame SYNC Protector and Inserter

Occasionally, the frame sync is omitted or detected in the place where it does not exist by the effect of error or jitter on a disc. In these case, it is need to protect or insert frame SYNC signal.

The window is made by using the WSEL of CNTL-S register to protect the frame SYNC, and it's width is determined by WSEL. If the frame SYNC is inputted to the window, it is true data and if it isn't inputted, it is ignored.

If the frame SYNC is not detected in the frame SYNC protection window, one is inserted from the internal counter block.

When continuous inserting of frame SYNC, the appointed number of frame according to the FSEM and FSEL of CNTL-S register is achieved, the ULKFS becomes "H" and the frame SYNC protection window is ignored. At that time, the frame SYNC is received absolutely, the ULKFS signal becomes "L" and the frame SYNC in window is received.

LKFS	ULKFS	COMMENT
1	0	Corresponding with play back frame SYNC and generated frame SYNC
0	0	1) Out of corresponding with play back frame SYNC and generated frame SYNC, but PBFR SYNC is detected in the window selected by WSEL. 2) Out of corresponding with PBFR SYNC and XTFR SYNC, the SYNC is inserted because it is'nt detected in the window selected by WSEL.
0	1	1) After insertion as many as the frame decided by FSEM and FSEL of CNTL-S register as frame isn't detected in the window. 2) In the case that the PBFR SYNC is not detected continually after 1)

Table 8

4. SUBCODE BLOCK

The 14-bit subcode SYNC signal(that is S0,S1) is detected in the subcode SYNC block. After detection of S0 and passing through a frame, the S1 is detected.

The S0+S1 signal is outputted to S0S1 terminal, and the subcode data is outputted to SDAT terminal when the S0S1 signal is "H".

The subcode data among the data inputted to EFMI terminal is demodulated to 8-bit subcode data (P,Q,R,S,T,U,V,W). It is synchronized with PBFR signal and outputted to SDAT terminal by SBCK clock.

Among the eight subcode data, only Q data is selected and loaded to the eighty shift register by FBFR signal. The result of checking the CRC (Cycle Redundancy Check) of loading data is synchronized with S0S1 rising edge and outputted to SQOK terminal.

If the result of CRC checking is error, "L" is outputted to SQOK terminal, and if it is true, "H" is outputted to SQOK terminal. In case of CRCQ of CNTL-Z register being "H", the result of CRC checking is outputted to SQDT terminal during from S0S1 "H" to SQCK negative edge.

The following is the timing chart of subcode block

.

1) SQCK Using External Clock: S0S1, SQOK, SQCK, SQDT Timing Chart

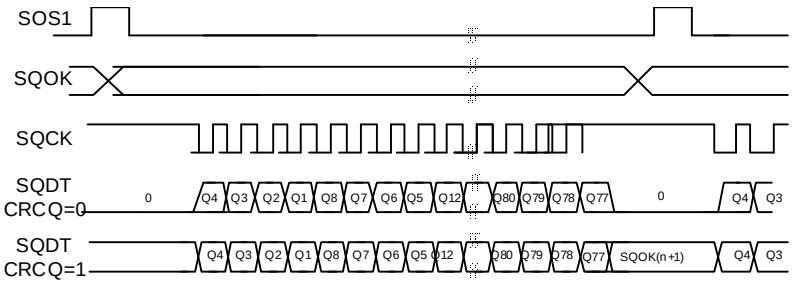
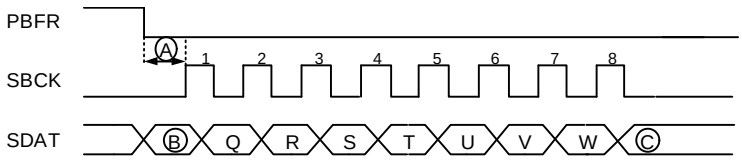


Fig.4. Subcode-Q timing chart

When the CRCQ of CNTL-Z register is "H", SQOK signal is outputted to SQDT terminal according SQCK signal, and when the CRCQ is "L", SQOK signal is not outputted to SQDT terminal.

2) SDAT, SBCK TIMING CHART



a. After PBFR becomes falling edge, SBCK becomes "L" during about 10μS.

b. If S0S1 is "L", subcode P is outputted, and if S0S1 is "H", S0S1 is outputted.

c. If the pulse inputted to the SBCK terminal is over seven, subcode data P, Q, R, S, T, U, V, W is repeated.

Fig.5. Timing chart of Subcode-Q data output

5. ECC (Error Correction Code) Block

The function of ECC block is to recover damaged data to some extent when data on a disk is damaged.

By using CIRC (Cross-interleave Reed-Solomon Code), C1(32,28: 2 Error) and C2 (28,24: 4 Erasure) error are corrected, and ECC is performed by the unit of one symbol of 8-bit.

In C1 correcting, a C1 pointer is generated, and in C2 correcting , a C2 pointer is generated. C1 & C2 pointer send error information or the data which ECC gives.

The information signal is used to deal with the error data, and the process of error correction can monitored by FLAG1, FLAG2, FLAG3, FLAG4, FLAG5 terminal.

MODE	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	REMARK
C1 No error	0	0	0	0	0	C1 correction start
C1 1 error	0	0	0	0	1	-
C1 2 error	0	0	0	1	0	-
C1 Irretrirvable error	0	1	1	1	1	C1 pointer set
C2 No error	1	0	0	0	0	C2 correction start
C2 1 error	1	0	0	0	1	-
C2 2 error	1	0	0	1	0	-
C2 3 error	1	0	0	1	1	-
C2 4 error	1	0	1	0	0	-
C2 Irretrievable error 1	1	1	1	1	0	C1 pointer copy
C2 Irretrievable error 2	1	1	1	1	1	C2 pointer set

Table 9. Error Correction monitoring flag

6. INTERPOLATOR / MUTE BLOCK

1) Interpolator

When a burst error occurs on a disc, sometimes the data can't be corrected even if the ECC process is performed.

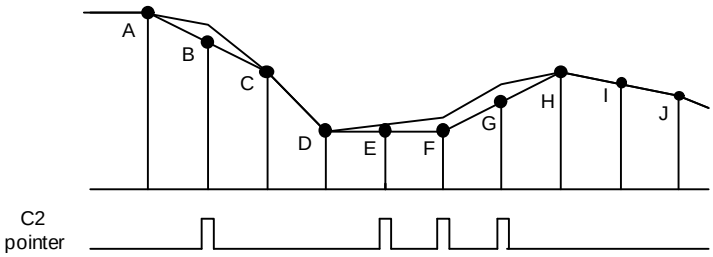
The interpolator block revises the data by using a C2 pointer outputted through the ECC block.

The data inputted to a data bus is inputted to the left and right channel respectively, in the order of C2 pointer, lower 8-bit and upper 8-bit.

In case of C2PO being "H" and the occurrence of a single error, an average interpolation method is carried out with the range of the data before and after an error happens. A pre-hold method is taken when the C2 pointer is "H" and 3 errors occur continuously.

When a check against a checked cycle LRCH is "L", R-ch data is outputted, and L-ch data is outputted when the check is "H".

The following is timing chart of interpolator block.



B = (A + C) / 2: Average Interpolation
F = E = D: Previous Data Hold
G = (F + H) / 2: Average Interpolation

Fig.6. Interpolation

2) MUTE AND ATTENUATION

By using a mute terminal and the ATTM signal of the CNTL-S register, the audio data is muted or attenuated.

A. Zero Cross Muting
The audio data is muted, after ZCMT of CNTL-S register goes to "H", and in case that mute is "H" and the upper 6 bits of audio data become all "L" or "H".

B. Muting
The audio data is muted when the ZCMT of CNTL-S rgister is "L" and MUTE terminal is "H".

C. Attenuation
The signal attenuation is occured by ATTM of CNTL-S register and MUTE signal as following.

ATTM	MUTE	Degree of Attenuation
0	0	0dB
0	1	- ∞ dB
1	0	-12dB
1	1	-12dB

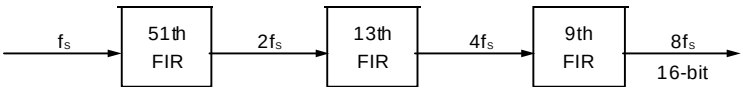
Table 10.

7. Digital Filter

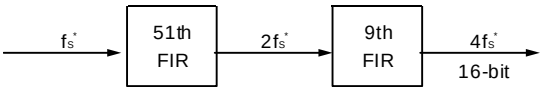
The KS9286B has a built-in FIR (Finite Impulse Response) digital filter.

This digital filter consists of 8fs over sampling filter.

1) Block Diagram



A) Normal speed play mode



B) Double speed play mode

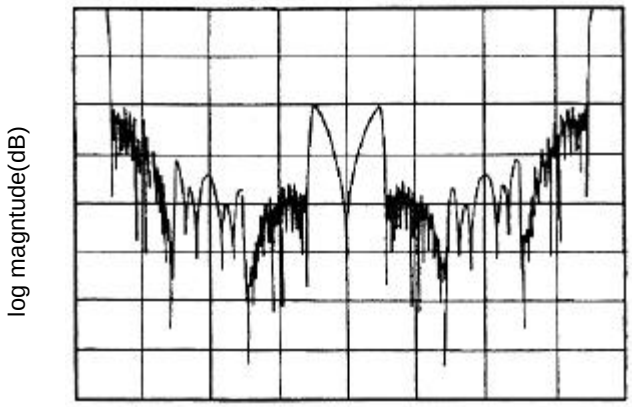
Fig.7. Digital filter block diagram

2) FILTER CHARACTERISTIC

Ripple in passband : within ± 0.5dB

Attenuation in stopband: below -42dB

(a) NORMAL SPEED



(b) DOUBLE SPEED

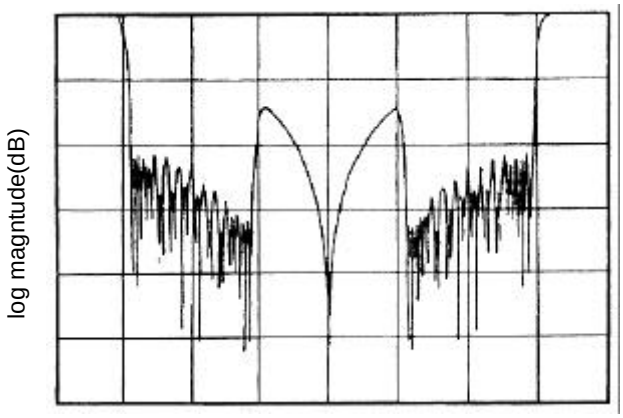
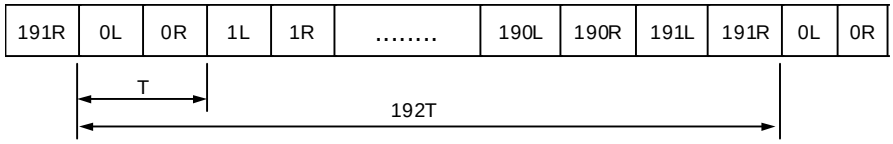


Fig.8. Filter characteristic curve

8. DIGITAL AUDIO OUTPUT BLOCK

The 2-channel, 16-bit data is connected and outputted serially to other digital system by the digital audio interface format.

1) Digital Audio Interface Format for CD



0L : L-ch format including block sync preamble
1L ~ 191L : L-ch format including L-ch sync preamble
0R ~ 191R : R-ch format including R-ch sync preamble

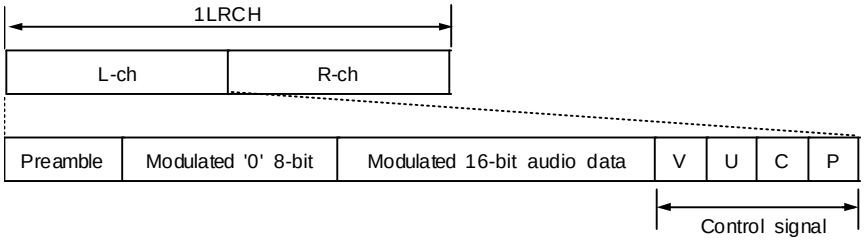
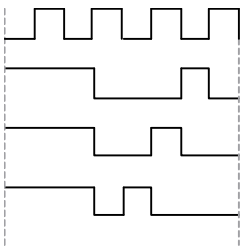


Fig.9. Digital audio output format

A. Preamble
It is used to discriminated against the block sync of data and L/R-channel of data.
Fig.10. Preamble Signal



8.4672MHz

L-ch sync (Except for Block Sync)

R-ch sync

Block sync(L-ch)

Fig.10. Preamble Signal

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B. CONTROL SIGNAL

1) Validity Bit: It is indicated that the error of 16-bit audio data exists, or doesn't. ("H": Error, "L": Valid data)

2) User Definable Bit: Subcode data output.

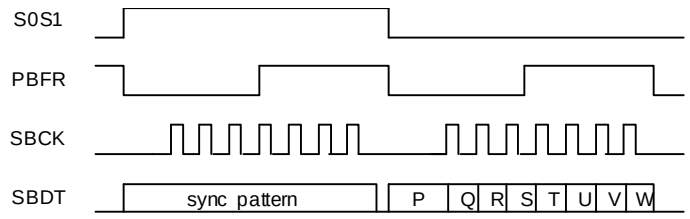


Fig.11. Timing chart of digital audio output

3) Channel Status Bit: Output a high position information of 4-bit of Subcode-Q indicating the number of channel, pre-emphasis and copy etc. Indicates the CDP category.

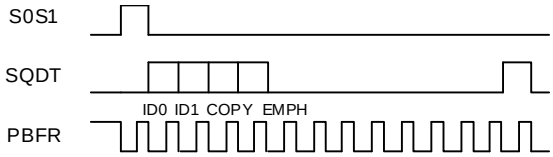


Fig.12. Timing chart of channel status data output

4) Parity Bit: Making even parity.

2) Timing Chart of Digital Audio Data Output

48 bits/slot

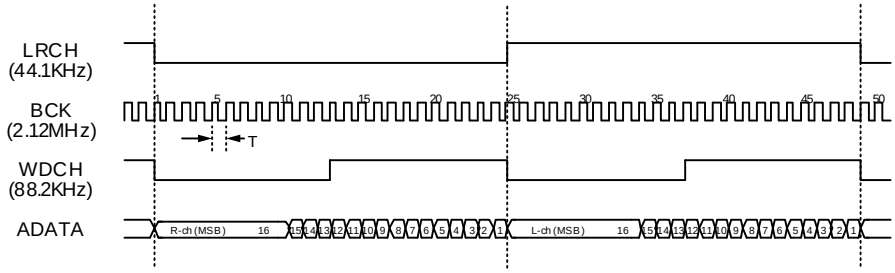


Fig.13. Timing chart of audio data output

9. CLV SERVO BLOCK

The CNTL-C register is selected to control CLV (Constant Linear Velocity) servo by the data inputted from Micom. In the CNTL-C register, the CLV servo action mode is appointed by the data inputted from Micom to control the spindle motor.

1) Forward

It is a mode of spindle motor rotates in forward direction. Output condition in forward mode is as following.

SMDP	SMSD	SMEF	SMON
H	Hi-Z	L	H

Table 11.

2) Reverse

It is a mode of spindle motor rotates in reverse direction. Output condition in reverse mode is as following.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	H

Table 12.

3) Speed-Mode

The spindle motor is controlled roughly by speed mode when track jumping or EFM phase is unlocked.

If a period of VCO is "T", the pulse width of frame sync is 22T. In case that the signal detected from EFM signal exceeds 22T by noise on the disc and etc., it must be removed, if not, the right frame sync can't be detected. In this case, the pulse width of EFM signal is detected by peak hold clock and bottom hold clock. (Peak hold clock is XTFR/2 or XTFR/4, and bottom hold clock is XTFR/16 or XTFR/32.)

The detected value is used for synchronized frame signal. If the frame signal is less than 21T, the SMDP terminal outputs "L", eaqul to 22T, outputs "Hi-Z", and more than 23T, ouputs "H".

If the gain signal of CNTL-W register is "L", the output of SMDP terminal is reduced up to -12dB, if it is "H", there is no reduction.

Output condition: SMSD="Hi-Z", SMEF="L", SMON="H".

4) Hspeed-Mode

The rough servo mode, which moves 20,000 tracks in high speed acts between the inside and outside of the CD.

The mirror domain of track which hasn't pit is duplicated with 20KHz signal to EFM. In this case, servo action is unstable because the peak value of mirror signal which is longer than orignal frame sync signal which is detected. In Hspeed mode, by using the 8.4672/256MHz signal against peak hold and XTFR/16 or XTFR/32 signal against bottom hold, the mirror component is removed, and Hspeed servo action to be stable.

The output condition is as following.

SMDP	SMSD	SMEF	SMON
-	Hi-Z	L	H

Table 13.

5) Phase-Mode

The phase mode is the mode to control the EFM phase. Phase difference between PBFR/4 and XTFR/4 is detected when NCLV of CNTL-Z register is "L",and phase difference between Read Base Counter/4 and Write Base Counter/4 detected when NCLV is "H", and the difference is outputted to SMDP(Fig.14).

If the cycle of VCO/2 signal is put as "T" and it is put as "/WP" during a "H" period of PBFR, it outputs "H" to SMSD terminal from the falling edge of PBFR to the (/WP-278T) x 32, and then, outputs "L" to the falling edge of the next PBFR (Fig.15).

6) XPHSP-Mode

The XPHSP mode is the mode used in normal operation.

The LKFS signal made from frame sync block is to sampling which period is PBFR/ 16. If the sampling is "H", the Phase mode is performed, and if the sampling is eight of "L" continously, Speed-mode is performed automatically. The selection of peak hold period in Speed-mode and selection of bottom hold period and gain in Speed/ Hspeed-mode is determined by CNTL-W register.

7) VPHSP-Mode

The VPHSP mode is the mode used for rough servo control. It uses VCO instead of X-tal in the EFM pattern test. When the range of VCO center changes, VCO is easily locked because the rotation of a spindle motor changes in the same direction.

8) Stop-Mode

The stop mode is used to stop the spindle motor.
The output condition is as following.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	L

Table 14

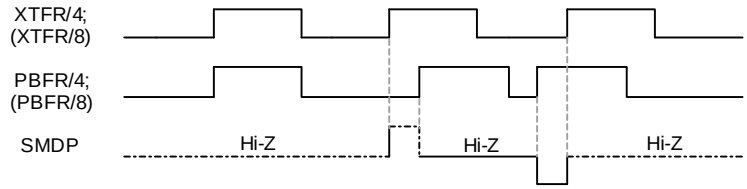
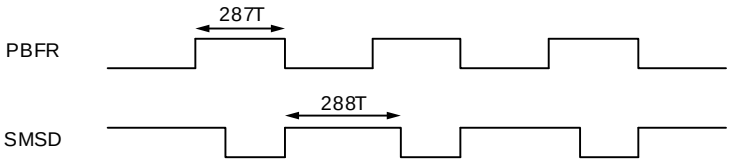
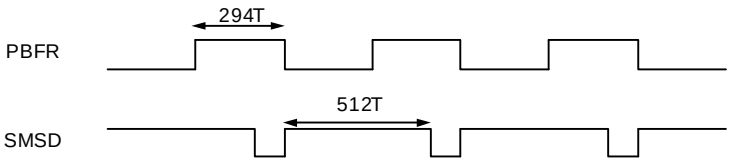


Fig.14. Timing chart of SMDP output



(A) Timing chart of SMSD when PBFR is 278T



(B) Timing chart of SMSD when PBFR is 294T

Fig.15. Timing chart of SMSD output in phase mode

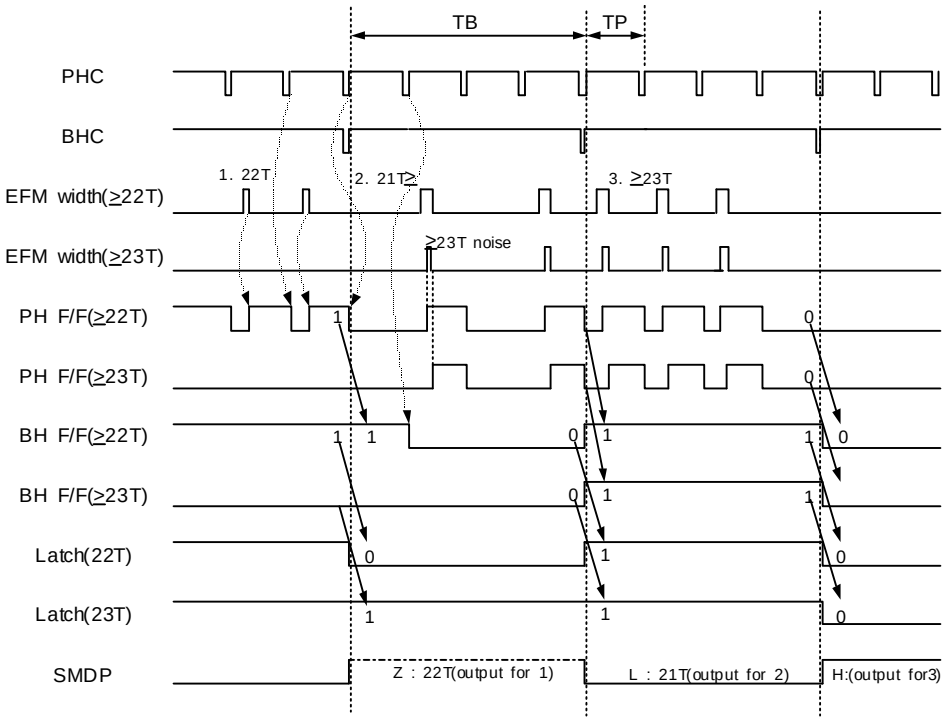


Fig.16. Timing chart of SMDP output when the gain is "H" in speed mode

10. DIGITAL PLL

This device contains Digital PLL in order to obtain the stable channel clock for demodulating EFM signal.

The block diagram of Digital PLL is as follows.

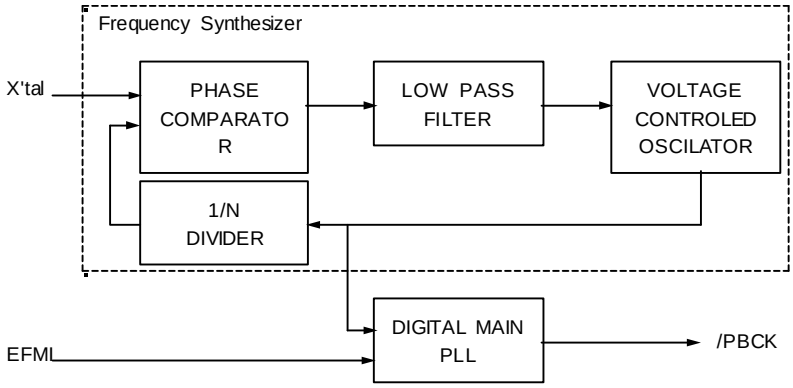


Fig.17. Digital PLL circuit diagram

11. D/A Converter (Digital to Analog Converter)

The KS9286B has a built-in 16-bit D/A converter. Digital audio data is a 2's complement serial format (MSB sirst),

1) Vref Terminal

Vref, the reference voltage across a resister-ladder, is usually recommended with VrefH1=5V, VrefL1=0V. One way of avoiding an amplitude mismatching between the Vref and OP AMP input connected to the output of D/A converter is to reduce the analog output amplitude with VrefH2=5V and VrefL2=0V (At this time about 100uF capacitor should be connected from VreH1 and VrefL1 to GND). By the effect of built-in RH and RL with this choice, the maximum analog output amplitude result in a narrow range of about 1.5 ~ 3.5V for 0dB playback.

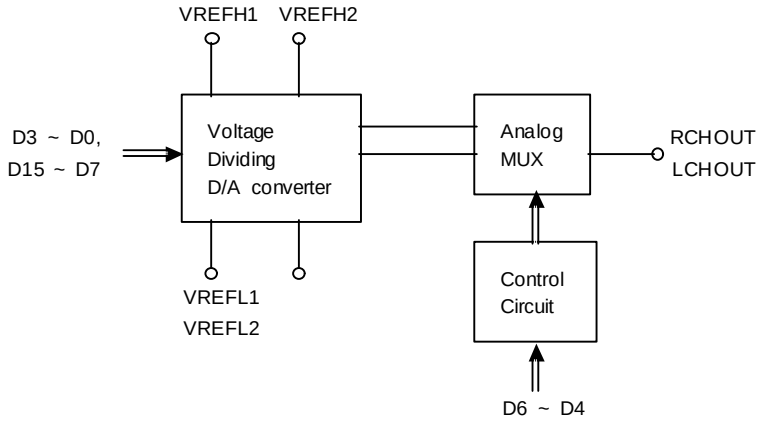


Fig.18. Vref relation circuit

2) D/A Converter Electrical Characteristic

The D/A Converter electrical characteristic built in KS9286B is as follows.

(VDD=5V, VSS=0V, Ta=25^{o}C)

Characteristics	Symbol	Test Conditon	MIN	TYP	MAX	Unit
Total Harmonic Distortion	THD	Data=1kHz, 0dB			0.08	%
Signal to Noise Ratio	S/N	VDD=4.5V Data=1kHz, 0dB		92		dB
Cross-Talk	CT	Data=1kHz, 0dB		-85		dB

Table 15

12. Digital De-Emphasis

The Emphasis/De-Emphasis circuit is used for improving S/N ration by decreasing high frequency noise in case of the frequency characteristic of signal not being changed.

The digital de-emphasis circuit, which can de-emphasise the signal emphasised on disc, is built-in KS9286B, and the frequency characteristic is as follows.

Frequency	Characteristic
1KHz	-0.51dB
5KHz	-4.5dB
10KHz	-7.59dB
20KHz	-9.5dB

Table 16. Frequency characteristic of de-emphasis circuit

13. ESP INTERFACE BLOCK

1) Introduction

Because the location of normal table CD Player used in family is fixed, it is possible to play music stabilitable when the degree of damage on disc is in limit range.

But in now, it is general that user can hear music when moving by Walkman-CD Player. In this case, if user has been shocked suddenly, it often happens that music playing is unstable.

On this, the ESP interface block is added to KS9286B for realizing the function of Anti-shock.

The application circuit of using NPC anti-shock memory controller IC SM5859AF and KS9286B is as follows.

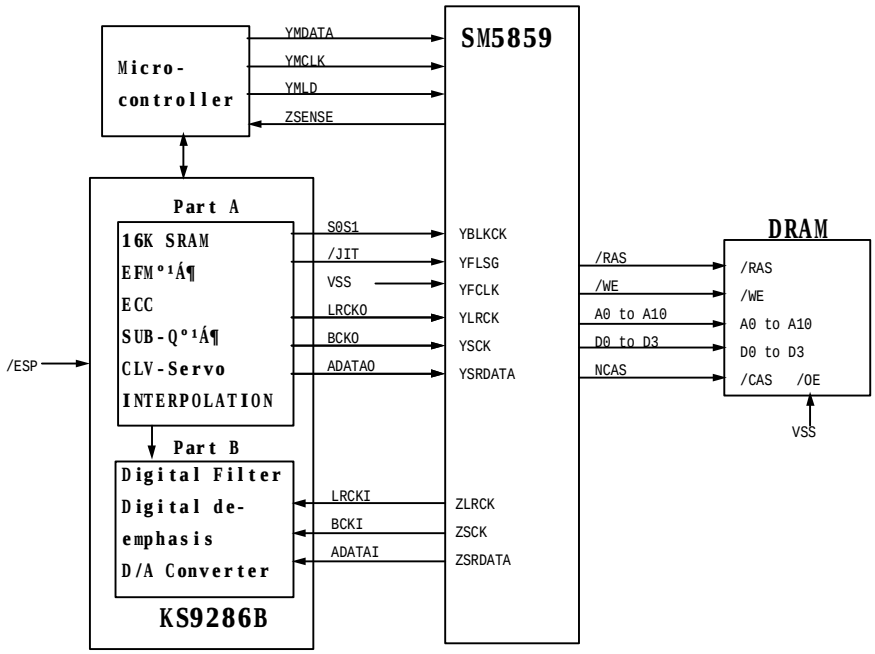


Fig.19. ESP interface application

The operation of KS9286B is different when normal operation and forming anti- shock function with external ESP IC. From Fig.19, the operation of part B composed by Digital Filter, Digital de-emphasis and 16-bit D/A Converter in KS9286B and part A except part B is separated. When anti-shock function is used in case of /ESP Pin being "L", part A block operates in double speed and part B block operates in normal speed. That is, after EFM Demodulation, Error Correction and Interpolation block operation in double speed, audio data is inputted to ESP IC which is the anti-shock memory controller. Audio data received by ESP IC is saved in external memory and then inputted to KS9286B. In part B of KS9286B, the data is dealed with in normal speed and then outputted .

The anti-shock function is not used in case of /ESP terminal being "H".

2) Timing Chart

The interface timing diagram of ESP IC is as follows.

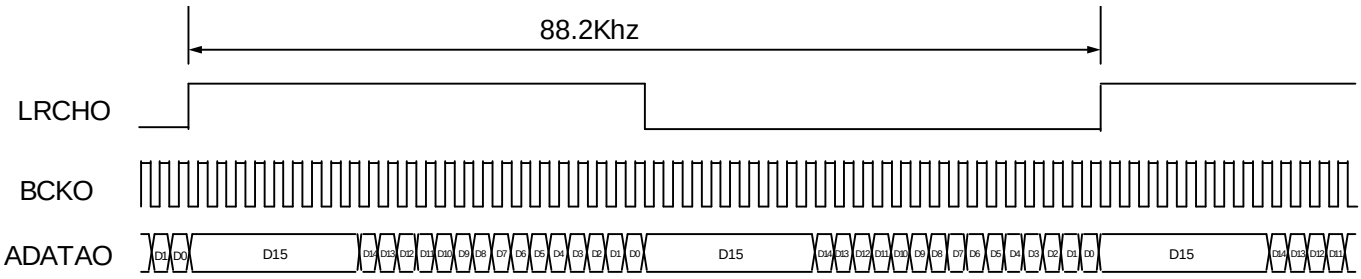


Fig.20. Timing chart of signal outputting to ESP IC

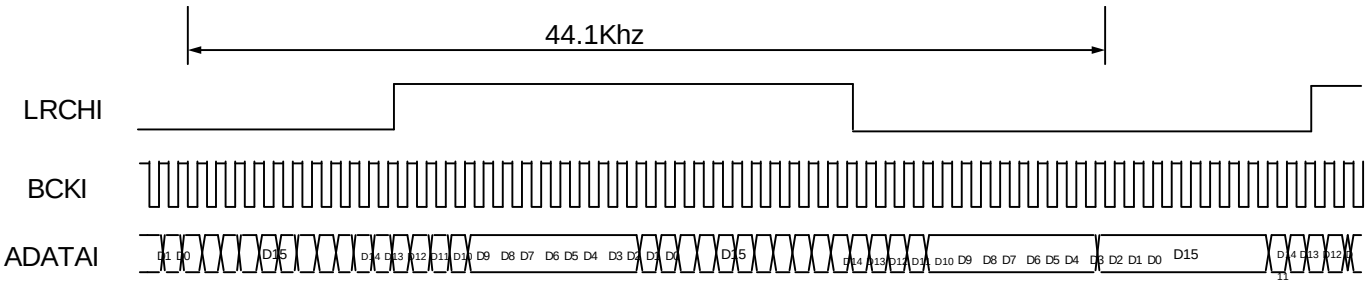


Fig.21. Timing chart of signal ESP IC outputting to DSP

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APPLICATION INFORMATION

1. ESP Part

If ESP IC is not used, you must connect follow pins to GND.

- LRCHI
- ADATAI
- BCKI

2. Pin setting condition

- TEST1 : Ground
- FOK

: Connect the servo IC # 40 Pin (KB9223) when use the FOK signal through /ISTAT pin otherwise, connect VDD or GND except upper application

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