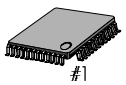
GENERAL DESCRIPTION

FCM(Frequency Conversion Memory) is the high speed line memory that has two 1024X10bits memory banks. KS7308 is designed as low power consumption by CMOS technology. KS7308 is used for camcorder with digital image stabilizer feature.

48-QFP-0707



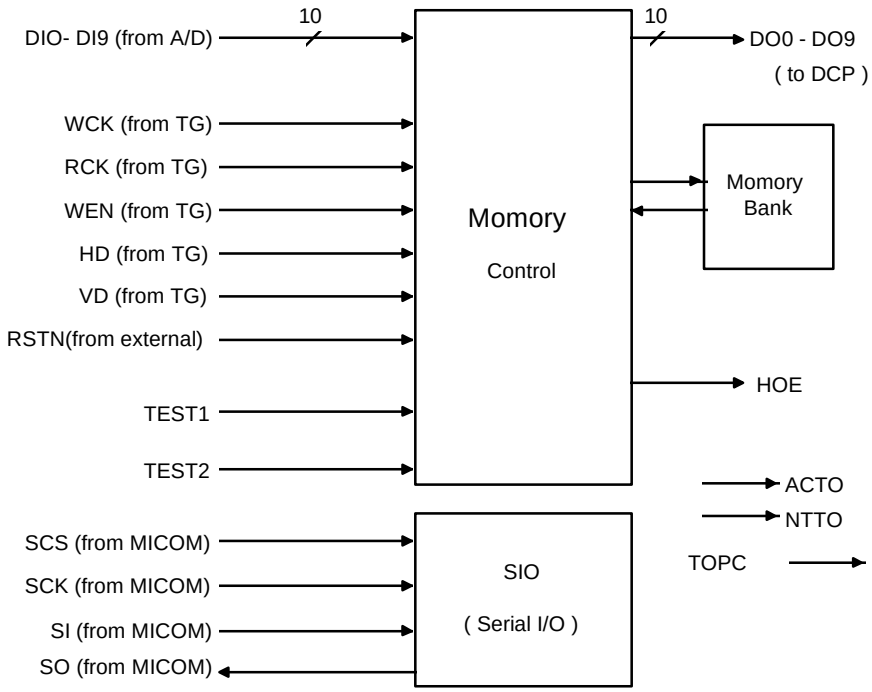
FEATURES

- 1024X10bits 2 bank Line memory.
- Independent Read/Write Operation.
- Programmable Read Start Address and Write Start Address.
- HD Pre-counter for Horizontal blanking.
- Serial-Interface Circuit
- CMOS Double metal technology
- 5V Power supply

ORDRING INFORMATION

Device	Package	Operating Temperature
KS7308	48-QFP-0707	0 ~ 70°C

BLOCK DIAGRAM

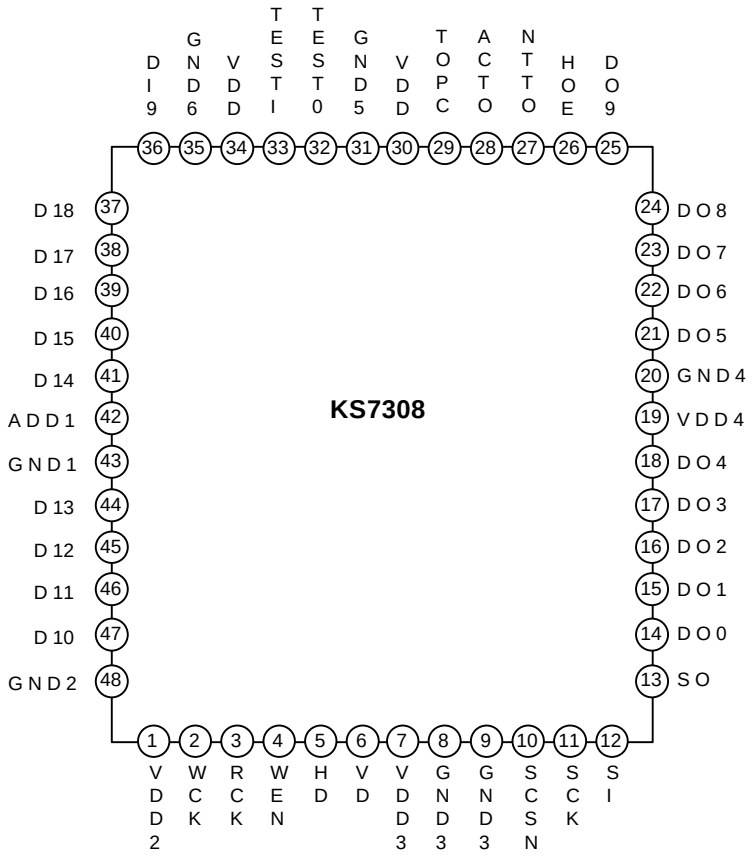


PIN DESCRIPTION

PIN NO.	Symbol	I/O	Description	Note
1	VDD1	-	Power Supply (5V)	vdd5p
2	WCK	I	Memory write clock from TG	
3	RCK	I	Memory read clock from TG	
4	WEN	I	Memory write enable from TG	
5	HD	I	Horizontal Driving pulse from TG	
6	VD	I	Vertical Driving pulse from TG	
7	VDD3	-	Power Supply (5V)	vdd5i
8	GND3	-	Ground	vssi
9	RSTN	I	Reset	
10	SCSN	I	SIO enable from MICOM	
11	SCK	I	SIO clock from MICOM	
12	SI	I	SIO data input from MICOM	
13	SO	O	SIO data output to MICOM	
14	DO0	O	Data output bit0	
15	DO1	O	Data output bit1	
16	DO2	O	Data output bit2	
17	DO3	O	Data output bit3	
18	DO4	O	Data output bit4	
19	VDD4	-	Power Supply (5V)	vdd5o
20	GND4	-	Ground	vsso
21	DO5	O	Data output bit5	
22	DO6	O	Data output bit6	
23	DO7	O	Data output bit7	
24	DO8	O	Data output bit8	
25	DO9	O	Data output bit9	
26	HOE	O	Horizontal odd/even signal output	
27	NTTO	O	Test output (Vin test)	
28	ACTO	O	Test output (Vin test)	
29	TOPC	I	Test input (ACTO control)	
30	VDD5	-	Power Supply (5V)	vdd
31	GND5	-	Ground	vdd5o
32	TEST0	I	Test input (Mode control)	
33	TEST1	I	Test input (Mode)	
34	VDD6	-	Power Supply (5V)	vdd5p
35	GND6	-	Ground	vssp
36	DI9	I	Data input bit9	
37	DI8	I	Data input bit8	
38	DI7	I	Data input bit7	
39	DI6	I	Data input bit6	
40	DI5	I	Data input bit5	
41	DI4	I	Data input bit4	
42	VDD1	-	Power supply (5V)	vdd5i
43	GND1	-	Ground	vssi
44	DI3	I	Data input bit3	
45	DI2	I	Data input bit2	
46	DI1	I	Data input bit1	
47	DI0	I	Data input bit0	
48	GND2	-	Ground	vssp

TEST1	TEST0	TEST Mode
0	0	Normal operation
0	1	Memory Function Test
1	0	SRAM-A Read/Write Test
1	1	SRAM-B READ/Write Test

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

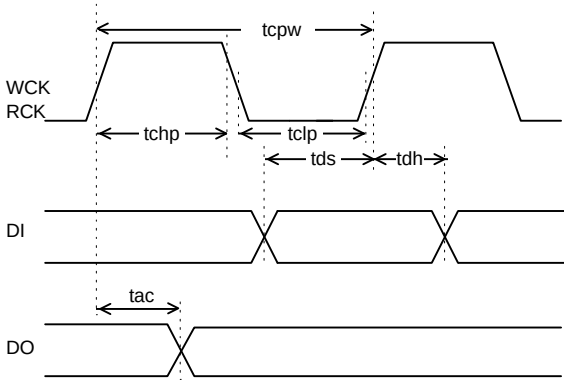
Characteristics	Symbol	Rating	Unit
Storage temperature	Tstg	-40 ~125	°C
Operating temperature	Topr	0 ~ 70	°C
Supply voltage	Vdd	-0.3 ~ 7.0	V
Input voltage	Vin	-0.3 ~ Vdd +0.3	V

ELECTRICAL CHARACTERISTICS (Vdd = 4.75 ~ 5.25V Ta = +25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Low level input voltage	VIL		-	-	0.3Vdd	V
High level input voltage	VIH		0.7Vdd	-		V
Low level output voltage *1	VOL1	IOL = 4mA	-	-	0.4	V
Low level output voltage *2	VOL2	IOL = 1mA	-	-	0.4	V
High level output voltage *1, *2	VOH	IOH = 1mA	2.4	-	-	V
Input Low current	IIL	Vin = Vss(Gnd)	-10	-	+10	uA
Input High current	IIH	Vin = Vdd	-10	-	+10	uA
Output leakage current	IOZ		-10	-	+10	uA
Supply current	Idd	Vin = Vdd	-	-	40	mA

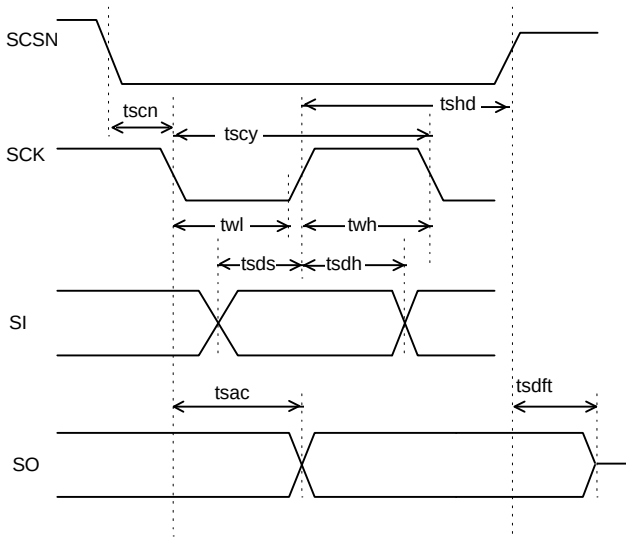
NOTE : *1 = NTTO,ACTO
*2 = SO, DO [9 : 0], HOE

AC ELECTRICAL CHARACTERISTICS



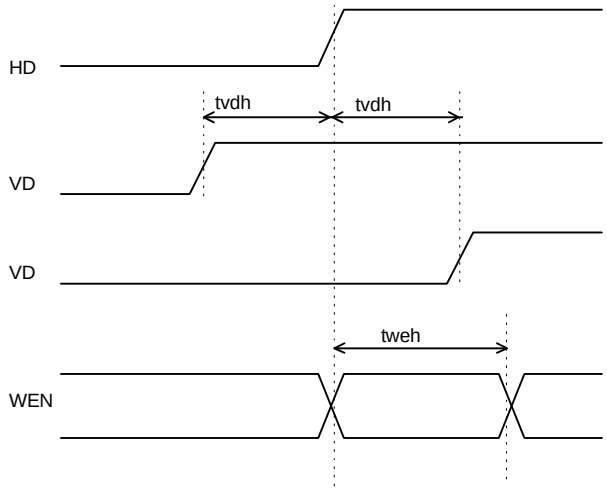
Vdd = 5.0 V

Characteristics	Symbol	Min	Max	Unit	
Clock cycle time	tcpw	54	tscy	ns	tscy : SCK clock
Clock high time	tchp	20		ns	
Clock low time	tclp	20		ns	
Write data hold time	tdh	0		ns	
Write data set up time	tds	10		ns	
Data access time	tac		40	ns	CL = 75pF



Vdd = 5.0

Characteristics	Symbol	Min	Max	Unit	Condition
Serial clock cycle time	tscy	2		us	
Serial clock high time	twh	700		ns	
Serial clock low time	twl	700		ns	
Serial data hold time	tsdh	30		ns	
Serial data set up time	tsds	30		ns	
Serial data set access time	tsac		500	ns	
Serial daa floating time	tsdft		20	ns	
SCSN set up time	tscn	30		ns	
SCSN hold time	tshd	30		ns	



Vdd = 5.0V

Characteristics	Symbol	Min	Max	Unit	Condition
VD level hold time	tvdh	4		RCK	RCL clock
WEN level hold time	tweh	5		RCK	RCK clock

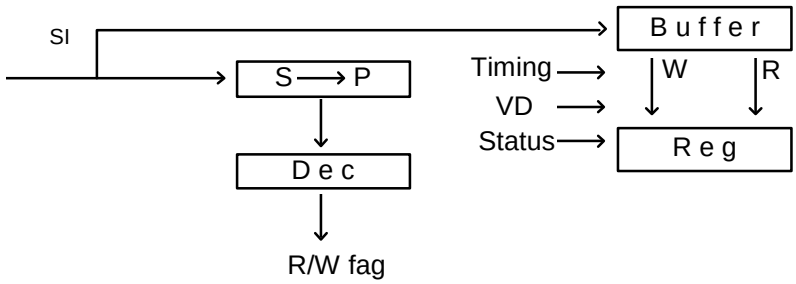
OPERATING

FCM has a SIO which is connected to DIS-MICOM. This SIO type can take 4wire type serial commuication with DIS-MICOM. MICOM can read the status of serial communication error such as parity error and Stop - Byte error. Read start address should contain a zoom value and a motion vecter calculated by DIS -MICOM. FCM starts to out data regarding ot the contents of the read start address resister. Thus, by setting proper read start address, Digital Image Stabilizer can be realized in a hoizontal direction. FCM has a HD precounter also to eliminate unnecessary data count in the memory bank.

1. DATA ACCESS

FCM supports normal 4 wired serial interface. The serial data is shifted from the MSB side. There are 6 resisters with 8 bit.
These are :
(1) SMOD (Serial Mode Resister)
(2) Read start address reister (2 Byte)
(3) Writer start address resister (2 Byte)
(4) HD precounter resister (1 Byte)

When user want to change one of above register contents, always user has to provide whole contents of each registers. And STOP Byte should follow. Thus, user has to send total 7 Byte data per each serial communication. For read only status register is valid for normal operation to check SIO operation condition.



2. SIO REGISTER

[Register diagram]

SMOS resister

(lst Byte)

MSB							LSB
0	0	0	0	RE	WE	0	0

group address

RE = 0, WE = 1 : Write enable (Write to register)
RE = 1, WE = 0 : Read enable (Read from counter outupt without UD bit)
RE = 0, WE = 0 : No operation RE = 1, WE = 1 : Prohibited

Read start address register (2 Byte)
Defines read start position in the bank memory.

(2nd Byte)

MSB							LSB
0	0	0	0	0	UD	A9	A8

(3rd Byte)

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

UD = 0 : Ciybter increment UD = 1 : Counter decrement

Write start address register (2 Byte)
Defines write start position in the bank memory

(4th Byte)

MSB							LSB
0	0	0	0	0	0	A9	A8

(5th Byte)

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

HD control register
Control to start read address counter incrementation from rising edge of HD.

(6th Byte)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Stop Byte

(7th Byte)

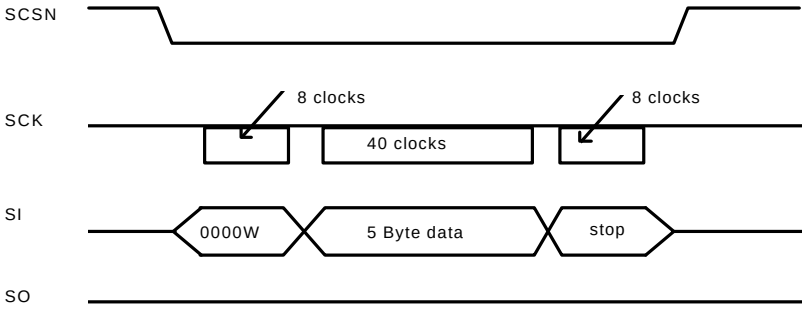
MSB							LSB
1	1	1	0	0	1	0	P

P : Even parity

3. MICOM DATA WRITE

(1) First data (SMOD) will entr to S/P buffer from SI for Command decoding. To specify write mode, W - bit has to be set "1" then. FCM is configurated to accept write access from MICOM.
(2) 4 Address data and HD control data will be written to Serial buffer.
(3) Last data (Stop Byte) in S/P will be checked such as Stop code and even parity.
(4) Data in serial buffer will be transferd to internal register at VD rising edge.

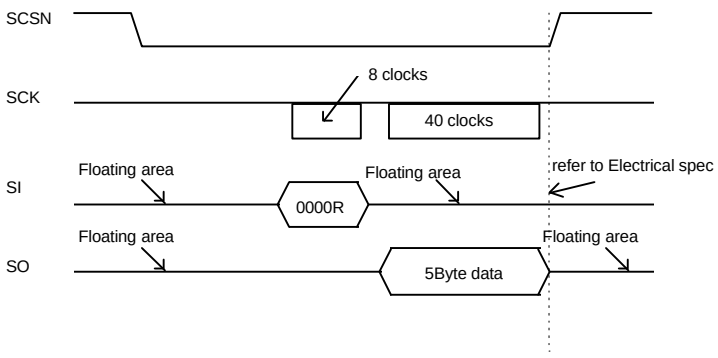
[Timing diagram]



4. MICOM Data Read

(1) First data (SMOD) will enter to S/P buffer from SI for Command decoding.
To specify read mode, R - bit has to be set "1" then. FCM is configured to accept read operation by driving SO.
(2) 4 counter values (Read Address counter ; 2 Byte, Writer Address counter ; 2 Byte,) and HD counter value are read out to SO pin.

[Timing diagram]



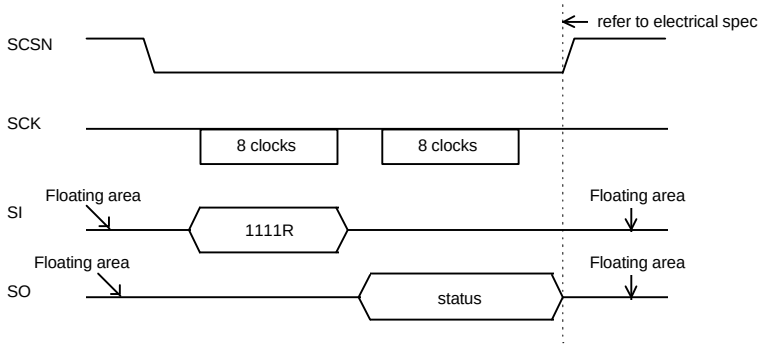
5. SIO STATUS READ

There is one status register to be read out by MICOM. There are 2 bit flags whigh are PE and WF respectivity.
The MICOM should check this status to test.

(1) Serial communication is successfully completed or not.
(2) Setting data are loaded into each register or not.

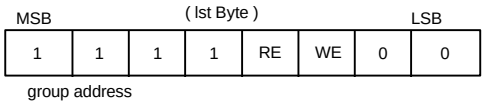
It is up to user to judge this flag or not.

[Timing diagram]



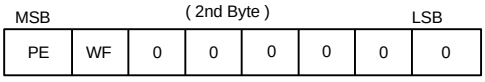
[Status register diagram]

Command



RE = 1, WE = 0 : Read enable
RE = 0, WE = 1 : Prohibited
RE = 0, WE = 0 : Prohibited
RE = 1, WE = 1 : Prohibited

Read data

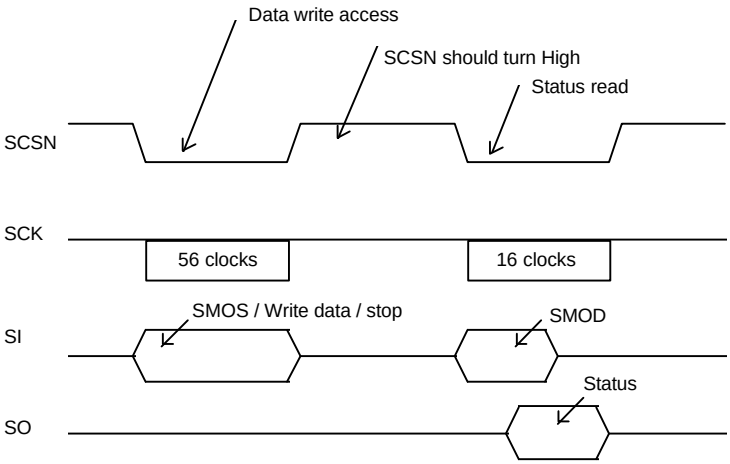


PE : Register write error flag
PE = 1 : Error
PE = 0 : No Error

WF : Register write status flag
WF = 1 : Waiting for loading into the register
WF = 0 : Loaded

6. SIO COMMUNICATION PROTOCOL

(1) Standard protocol of data write



(2) Invalid write data

When user initiate SIO operation before previouse write operation data is loaded into resister at VD timiing, then initial data will be broken.

7. RESET CONDITION

The system should supply reset condition by RSTN pin as low level. FCM will initialize each register value as follows.

(1) Read/Write address register and Counter is set to “0”
(2) HD register is set to “0”.
(3) SMOD register is set to “0”
(4) SO becomes high impedance state.

PKG DIAGRAM

48-QFP-0707

Unit : mm