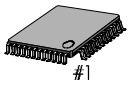
GENERAL DESCRIPTION

The KS7212 is a CMOS integrated circuit designed for making various timing pulses for B/W CCD camera.

48-QFP-0707



FEATURES

- Compatible with both EIA and CCIR mode (EIA : KC73125(U)-M, CCIR : KC73129(U)-M)
- Built in auto iris function (Electronic Exposure)
- Mirror mode timing generation
- Field interlace mode only
- Timing and sync one chip IC
- Oscillation frequency
  EIA : 19.06992MHz, CCIR : 18.93750MHz

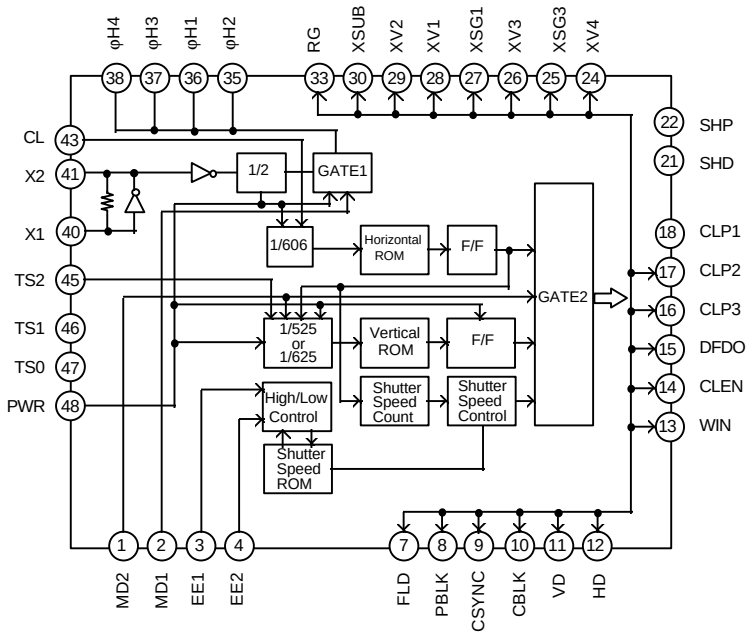
APPLICATION

- B/W CCD Camera

ORDERING INFORMATION

Device	Package	Operating Temperature
KS7212	48-QFP-0707	-20~75°C

BLOCK DIAGRAM



PIN DESCRIPTIONS

No	Symbol	I/O	Description	Remark
1	MD2	I	CCIR/EIA mode selection	* Information (1)
2	MD1	I	NORMAL/MIRROR mode selection	* Information (1)
3	EE1	I	EE mode control input 1	* Information (2)
4	EE2	I	EE mode control input 2	* Information (2)
5	VSS1	-	Ground	
6	VDD1	-	+5V	
7	FLD	O	Field separation pulse	
8	PBLK	O	Pre - blanking pulse	
9	CSYNC	O	Composite Sync.pulse	
10	CBLK	O	Composite Blanking pulse	
11	VD	O	Vertical driving pulse	
12	HD	O	Horizontal driving pulse	
13	WIN	O	Window pulse	
14	CLEN	O	1/2 HD frequency pulse	
15	DFDO	O	1/2 VD frequency pulse	
16	CLP3	O	Clamp pulse 3 (Dummy black level)	
17	CLP2	O	Clamp pulse 2 (Optical black level)	
18	CLP1	O	Clamp pulse 1 (Optical black level)	
19	VSS2	-	Ground	
20	VDD2	-	+5V	
21	SHD	O	Data Sample & Hold pulse	
22	SHP	O	Pre - Charge Sample & Hold pulse	
23	VSS3	-	Ground	
24	XV4	O	Vertical transfer clock 4	
25	XSG3	O	Read out Pulse 3	
26	V3	O	Vertical transfer clock 3	
27	XSG1	O	Read out Pulse 1	
28	XV1	O	Vertical transfer clock 1	
29	XV2	O	Vertical transfer clock 2	
30	XSUB	O	Shutter speed control for auto Iris	
31	VDD3	-	+5V	
32	VSS4	-	Ground	
33	φRG	O	Reset gate pulse	
34	VDD4	-	+5V	
35	φH2	O	Horizontal transfer pulse 2 (Mirror mode)	
36	φH1	O	Horizontal transfer pulse 1 (Normal mode'H')	
37	φH3	O	Horizontal transfer pulse 3 (Normal mode'H2')	
38	φH4	O	Horizontal transfer pulse 4 (Mirror mode)	
39	VSS5	-	Ground	
40	X1	I	Oscillation clock Input EIA : 19,069928MIHz CCIR : 18.93750MHz	
41	X2	O	Oscillation clock Output	
42	VDD5	O	+5V	
43	CL	O	1/2 Oscillation clock EIA : 9.953496Mhz CCIR : 9.46875MHz	
44	VSS6	-	Ground	
45	TS2	I	Test Input 2	
46	TS1	I	Test Input 1	
47	TS0	I	Test Input 0	
48	PWR	-	Power On Reset	

Information 1) MD2 and MD1 mode selection (Pull - down)

MD2	MD1	MODE
L	L	EIA NORMAL
	H	EIA MIRROR
H	L	CCIR NORMAL
	H	CCIR MIRROR

Information 2) EE2 and EE1 shutter speed mode selection (Pull- up)

EE2	EE1	MODE
L	L	SHUTTER SPEED STOP
	H	SHUTTER SPEED UP
H	L	SHUTTER SPEED DOWN
	H	SHUTTER SPEED STOP

ABSOLUTE MAXIMUM RATINGS

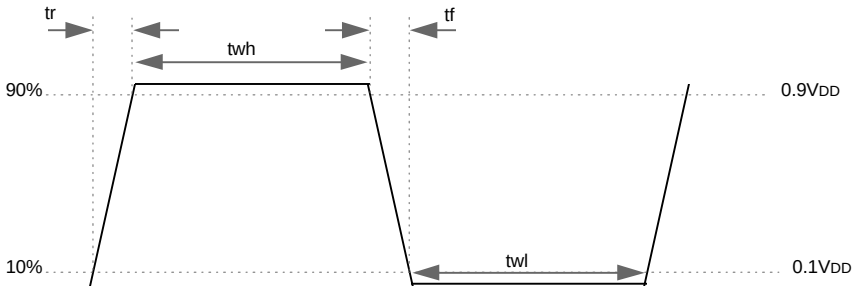
Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_O	V_{SS}-0.5 ~ V_{DD}+0.5	V
Operating Temperature	T_{OPR}	-20 ~ +75	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{DD}=5V, Ta=25°C, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	4.75	5.0	5.25	V
Input Voltage	V_{IH}	-	0.7V_{DD}	-	-	V
	V_{IL}	-	-	-	0.3V_{DD}	V
Output Voltage 1	V_{OH1}	IOH1=-2mA	V_{DD}-0.5	-	-	V
	V_{OL1}	ICL1=4mA	-	-	0.4	V
Output Voltage 2 (CL, RG, SHP, SHD)	V_{OH2}	ICH2=-4mA	V_{DD}-0.5	-	-	V
	V_{OL2}	IOL2=3mA	-	-	0.4	V
Output Voltage 3 (H1, H2, H3, H4)	V_{OH3}	ICH3=-8mA	V_{DD}-0.5	-	-	V
	V_{OL3}	ICL3=8mA	-	-	0.4	V

AC CHARACTERISTICS



PULSES	twh			twl			tr			tf			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
XSG1 , XSG3	2.3	2.5						0.5			0.5		us
XV1 , XV2 , XV3 , XV4								0.015			0.24		us
H1 , H2 , H3 , H4	26	32		26	32			11	12		11	12	ns
RG	11	13			51			5			5		ns
XSUB	1.5	2.0							0.5			0.5	us
SHP , SHD , CLP1 , CLP2 , CLP3 , DFD0 , CLEN , WIN , HD , VD , CBLK , CSYNC , FLD							13	14	16	13	14	16	ns

OPERATING PRINCIPLES & METHOD

POWER ON RESET

KS7212 has two reset methods. The one is power on reset and the other is normal reset.

When user wants to use power on reset , which generates automatical reset signal that is needed to initialize the KS7212 internal system when power is on, user should be connect 1000pF capacitor at PWR (pin 48) termial.

Power on reset system has internal 100Kohm pull up resister. So , user can control reset signal timing when user changes value of capacitor , which is connected to PWR terminal.

When user wants to use normal reset , user should be remove capacitor from PWR terminal , and supplies reset signal to PWR terminal.

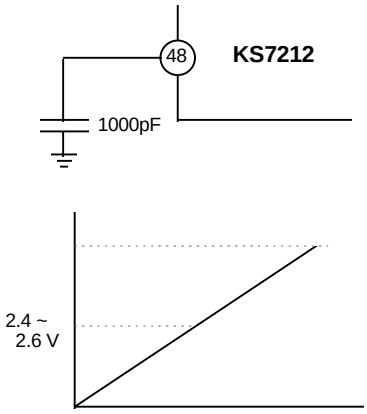


Fig. 1 POWER ON RESET

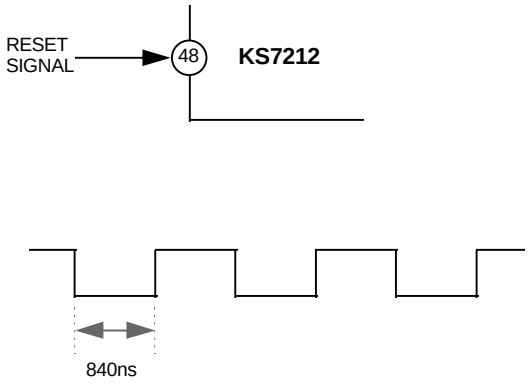
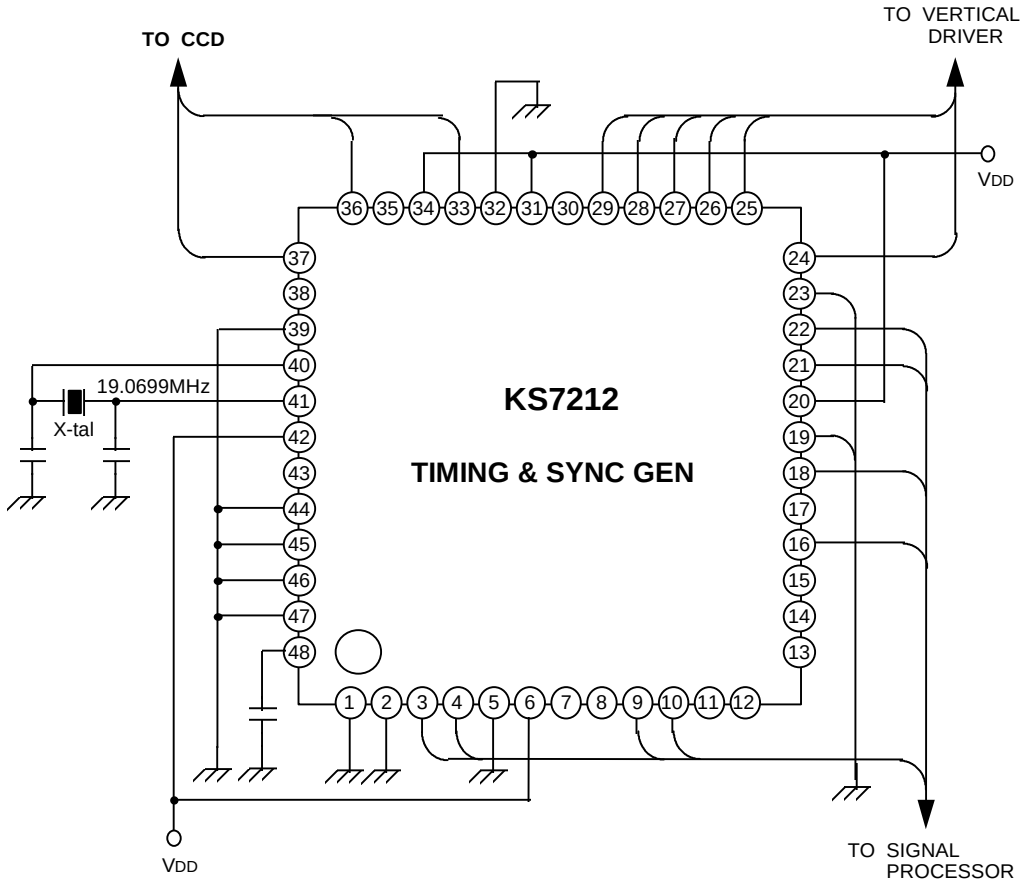


Fig. 2 NORMAL RESET

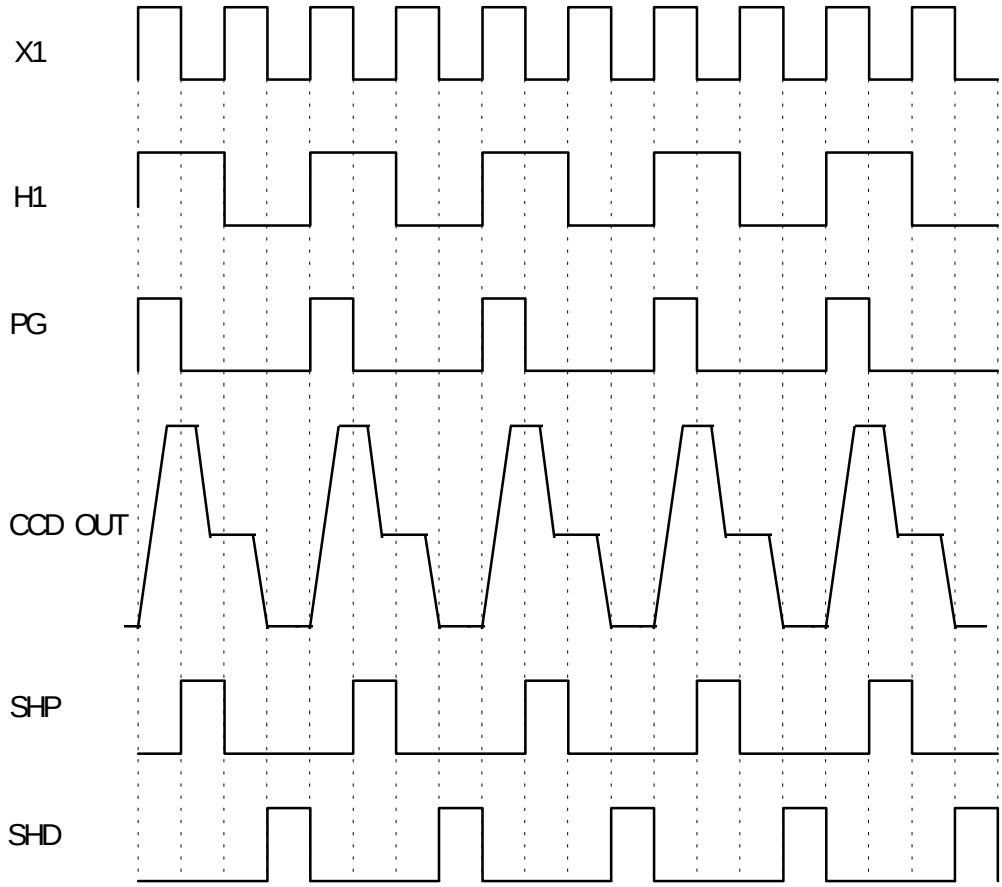
When use u-Com system , reset signal can be supplied three times and times of 1 signal should be larger than four times of CL clock.

APPLICATION CIRCUIT (EIA , NORMAL mode)

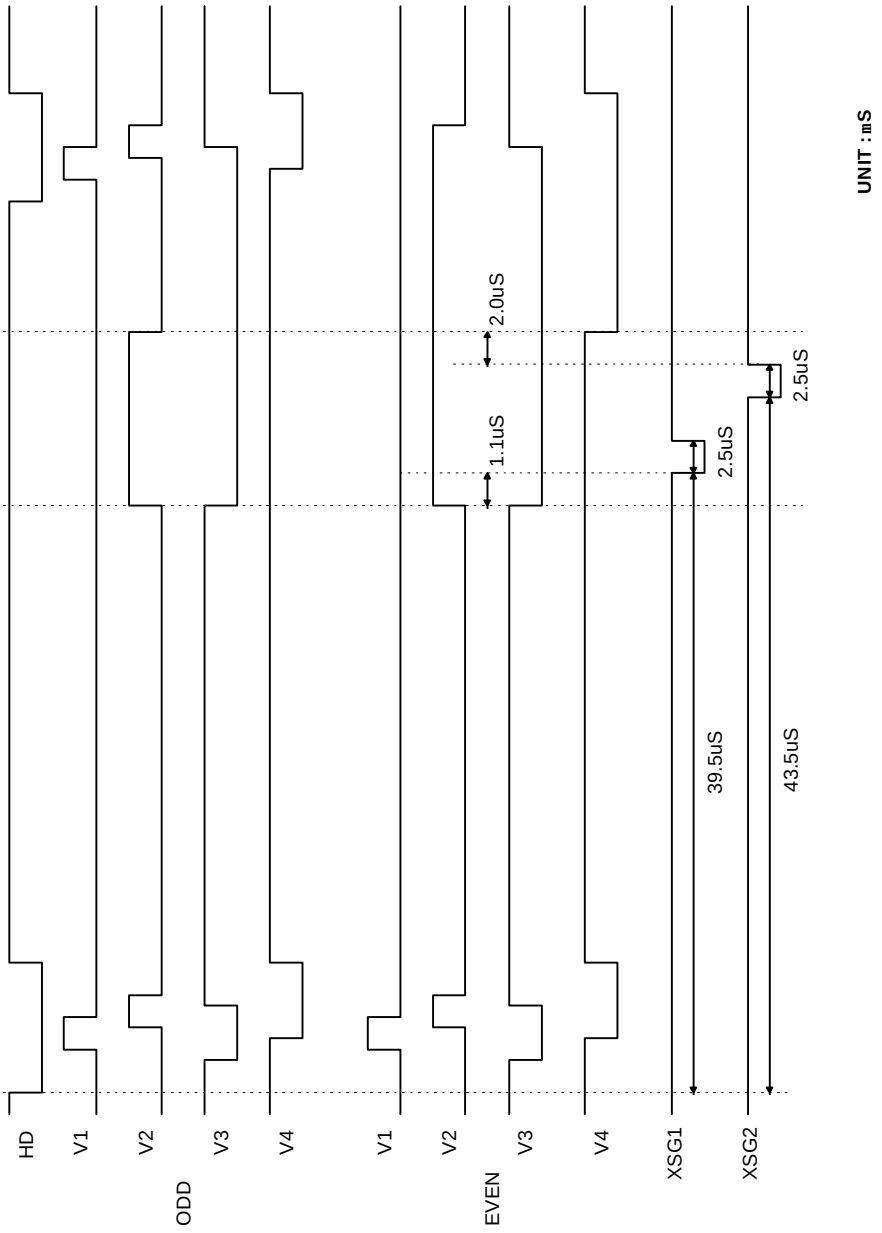


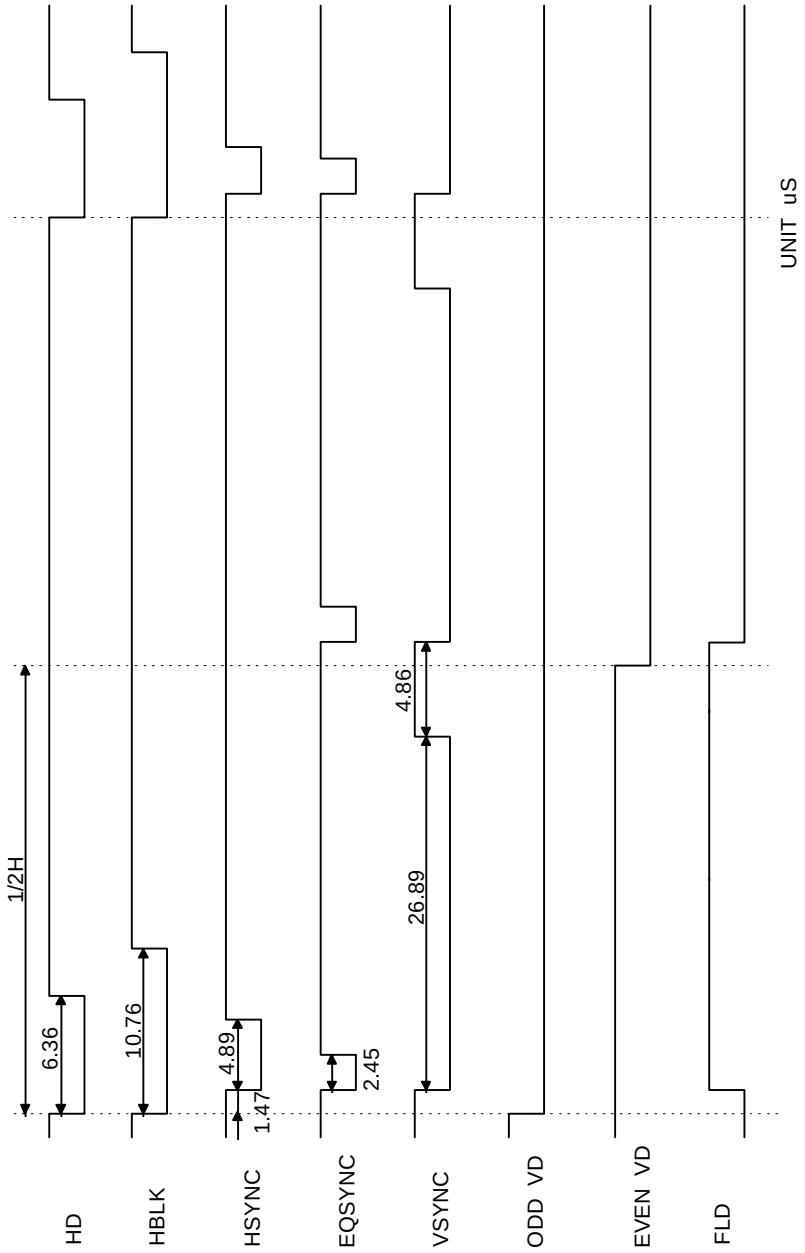
* Application circuit for normal mode
EIA : 19.06992MHz
CCIR : 18.93750MHz

HIGH SPEED TIMING RELATIONSHIP

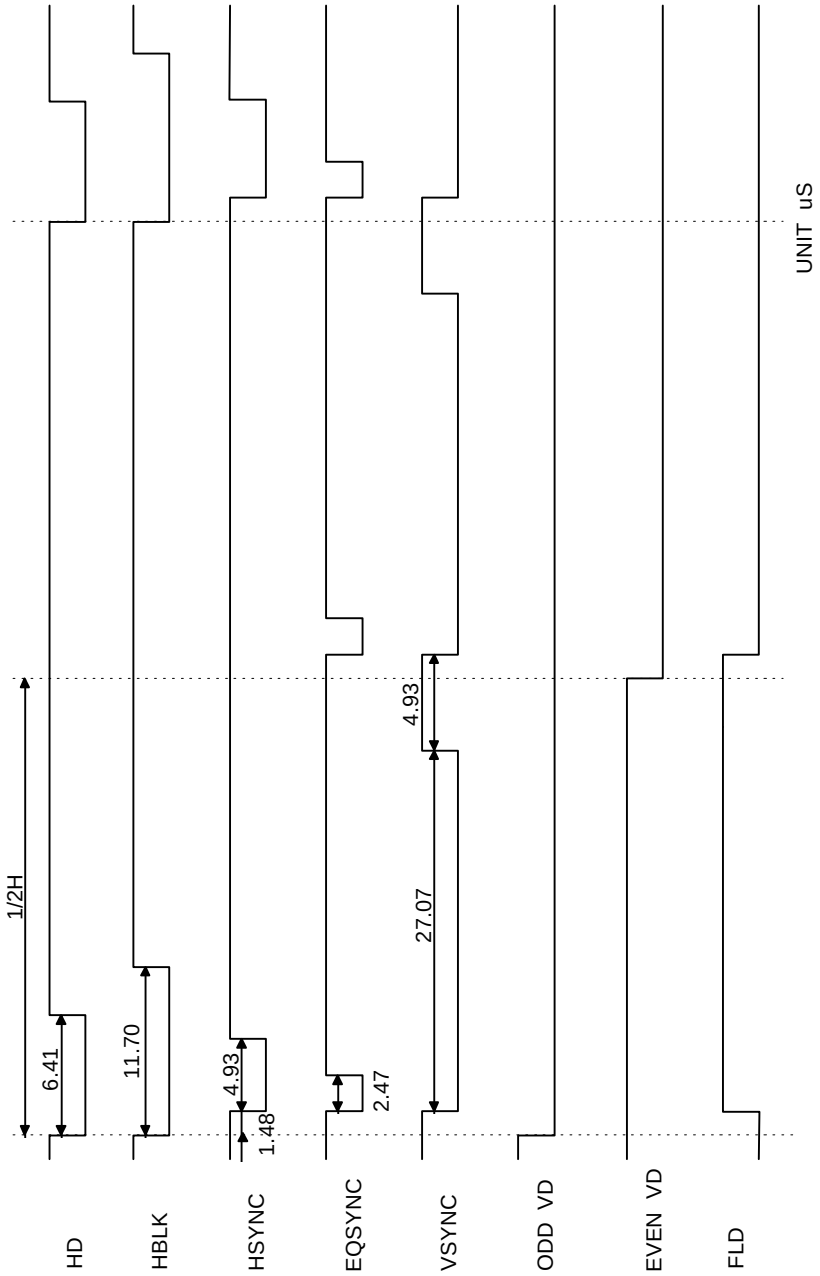


CCD VERTICAL DRIVING PULSE TIMING DIAGRAM

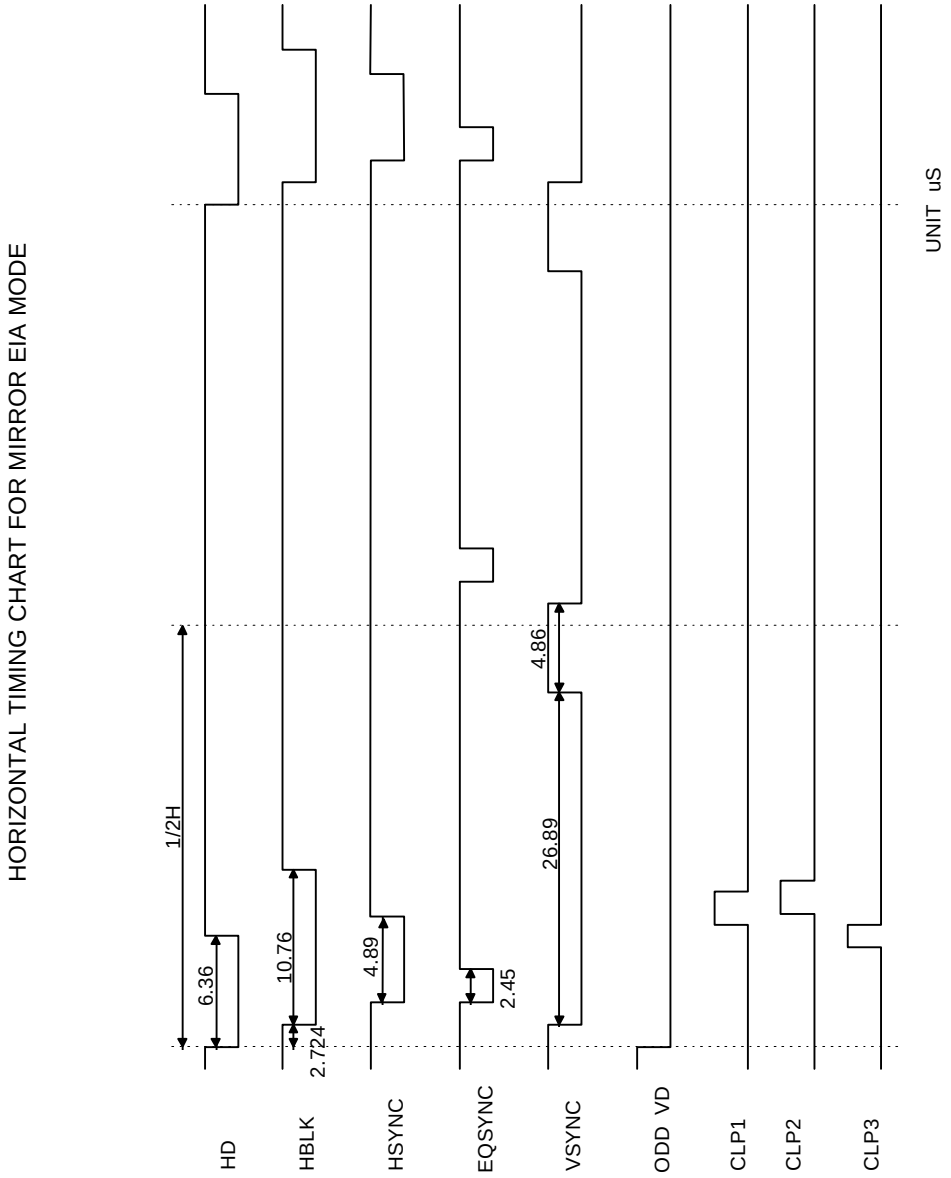



UNIT uS
1/2H
6.36
10.76
4.89
1.47
2.45
26.89
4.86
HD
HBLK
HSYNC
EQSYNC
VSYNC
ODD VD
EVEN VD
FLD

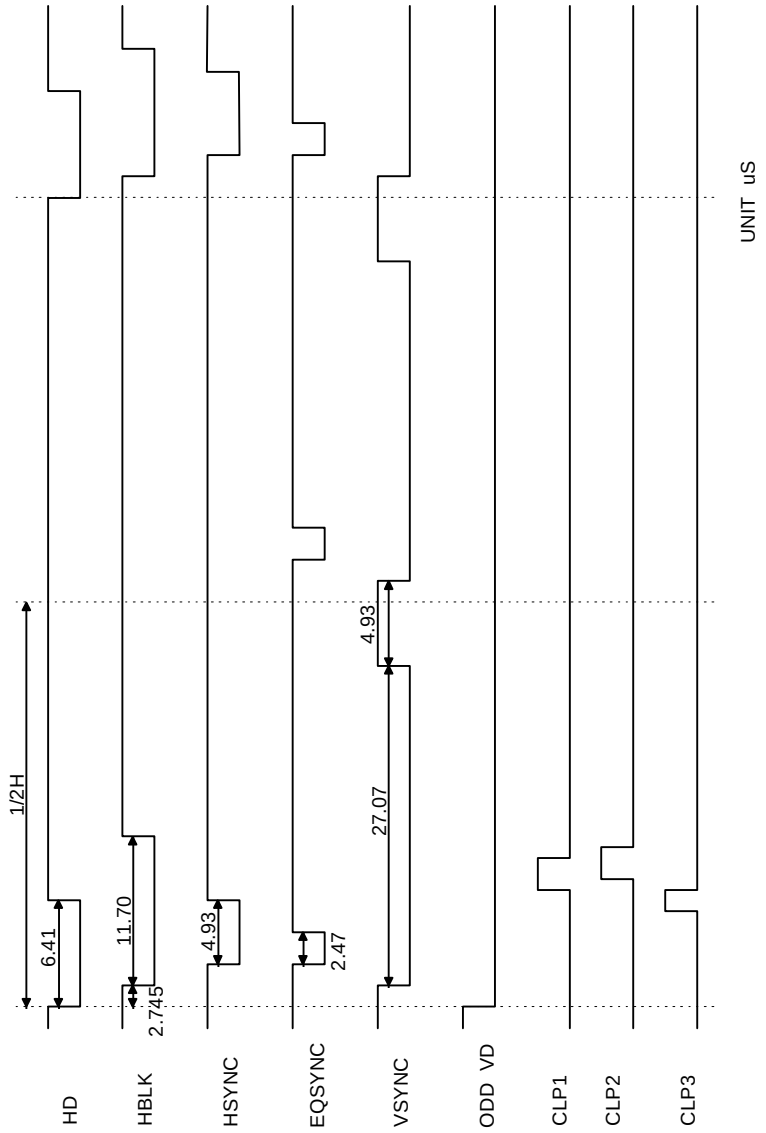
HORIZONTAL TIMING CHART FOR CCIR



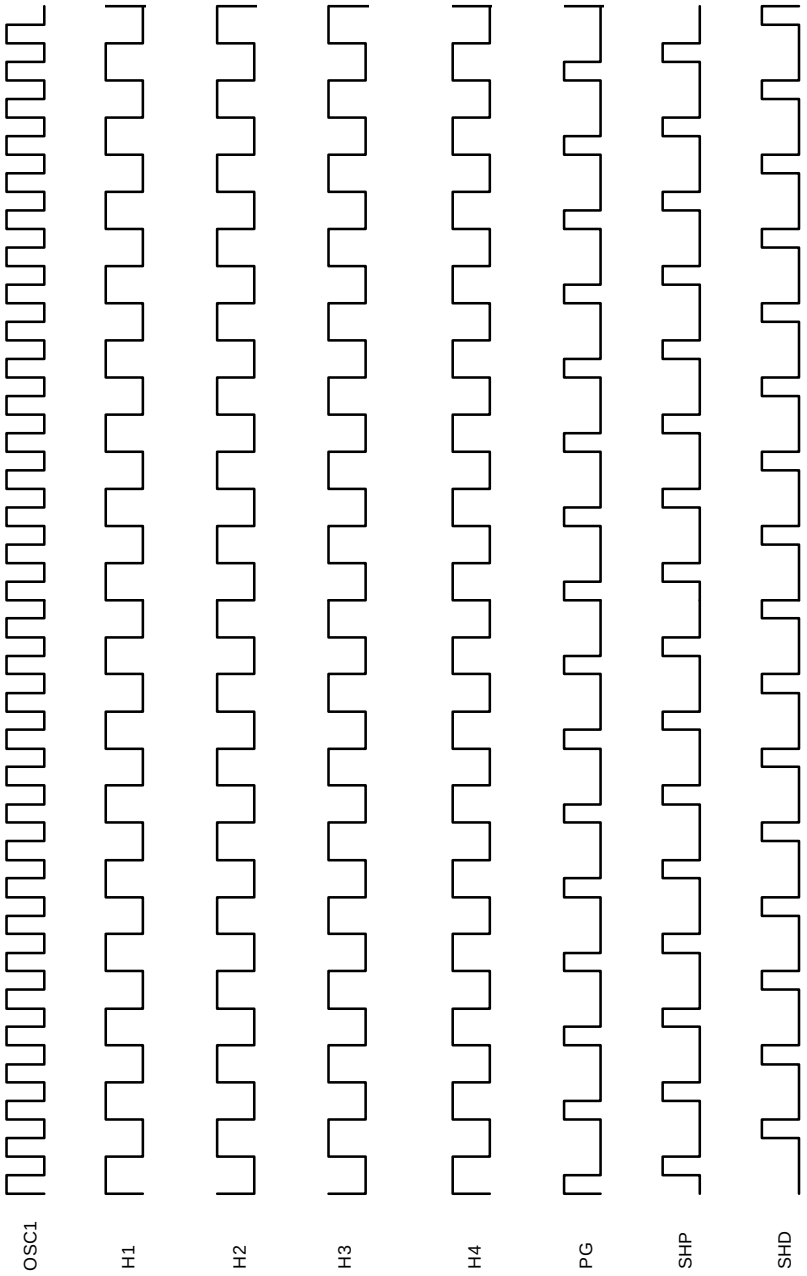
HORIZONTAL TIMING CHART FOR MIRROR EIA MODE



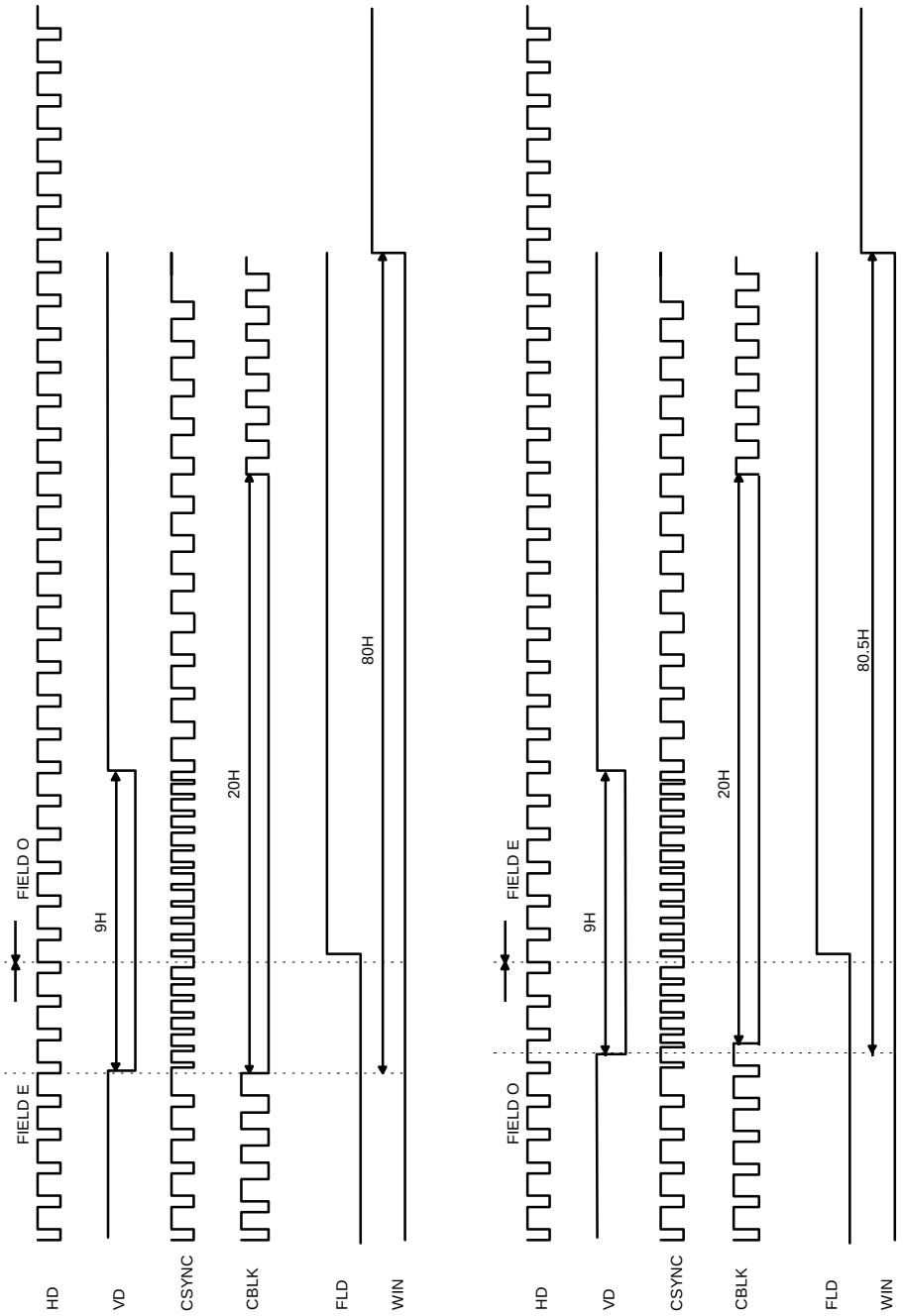
HORIZONTAL TIMING CHART FOR MIRROR CCIR MODE



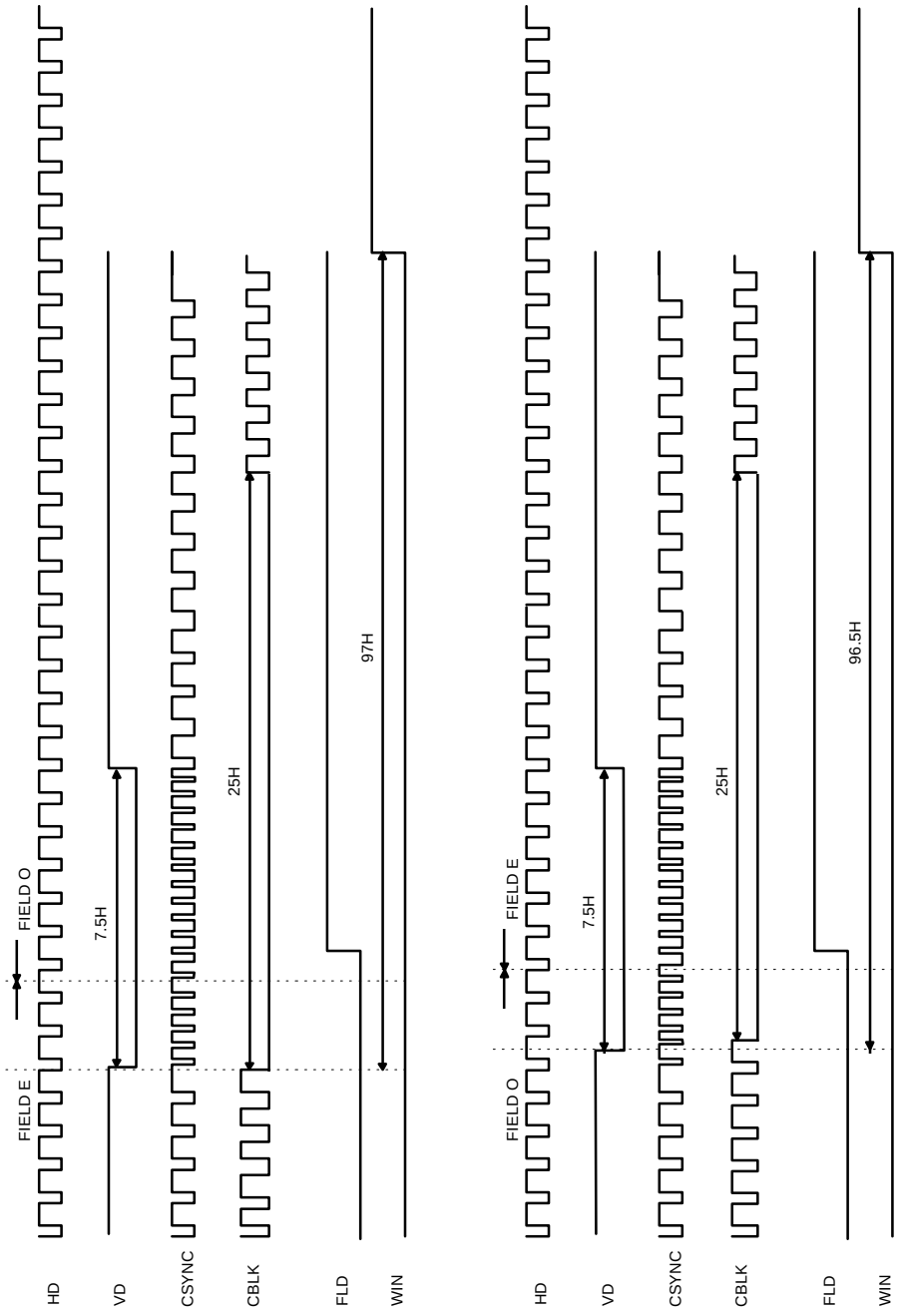
H1, H2, H3, H4, PG, SHP, SHD TIMING CHART AT MIRROR MODE OF CCIR



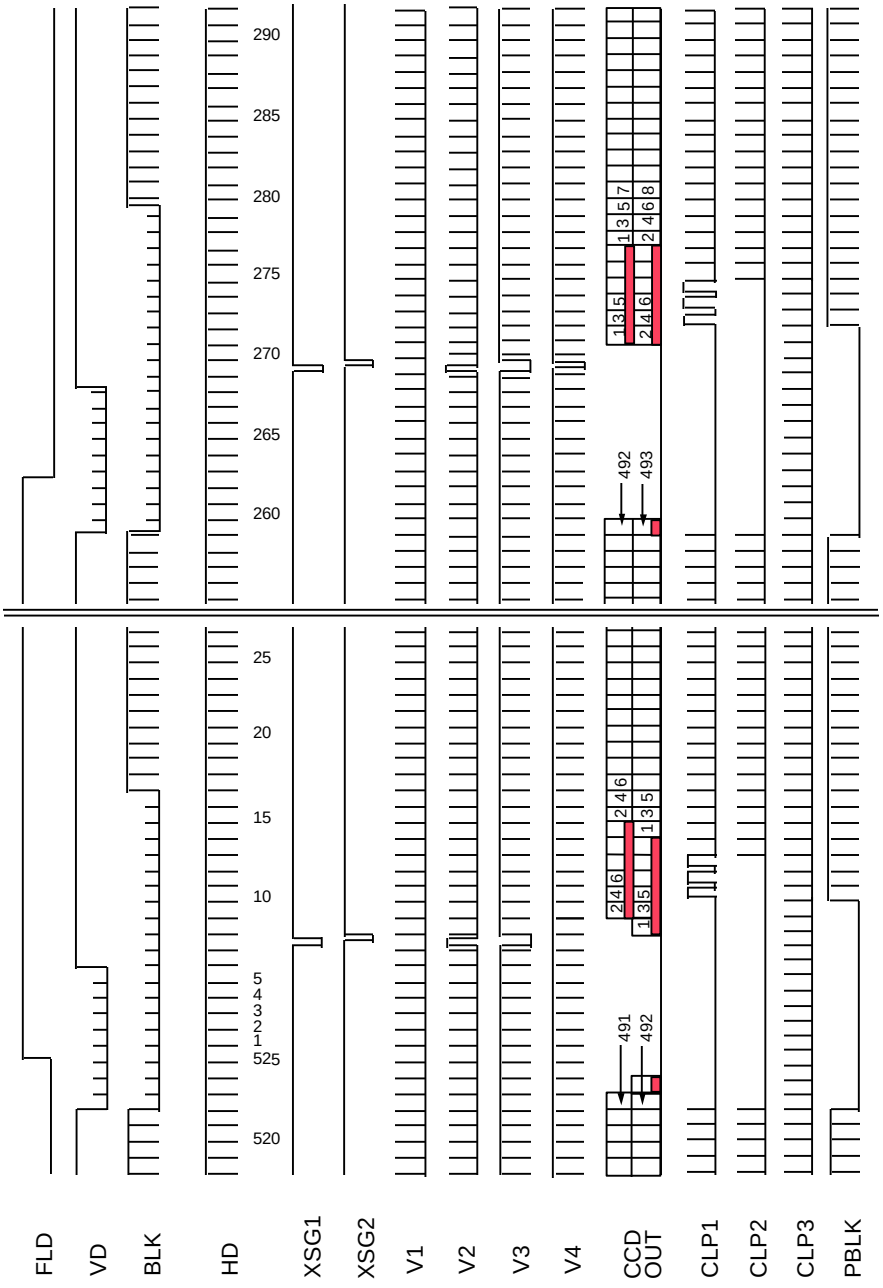
EIA VERTICAL TIMING CHART



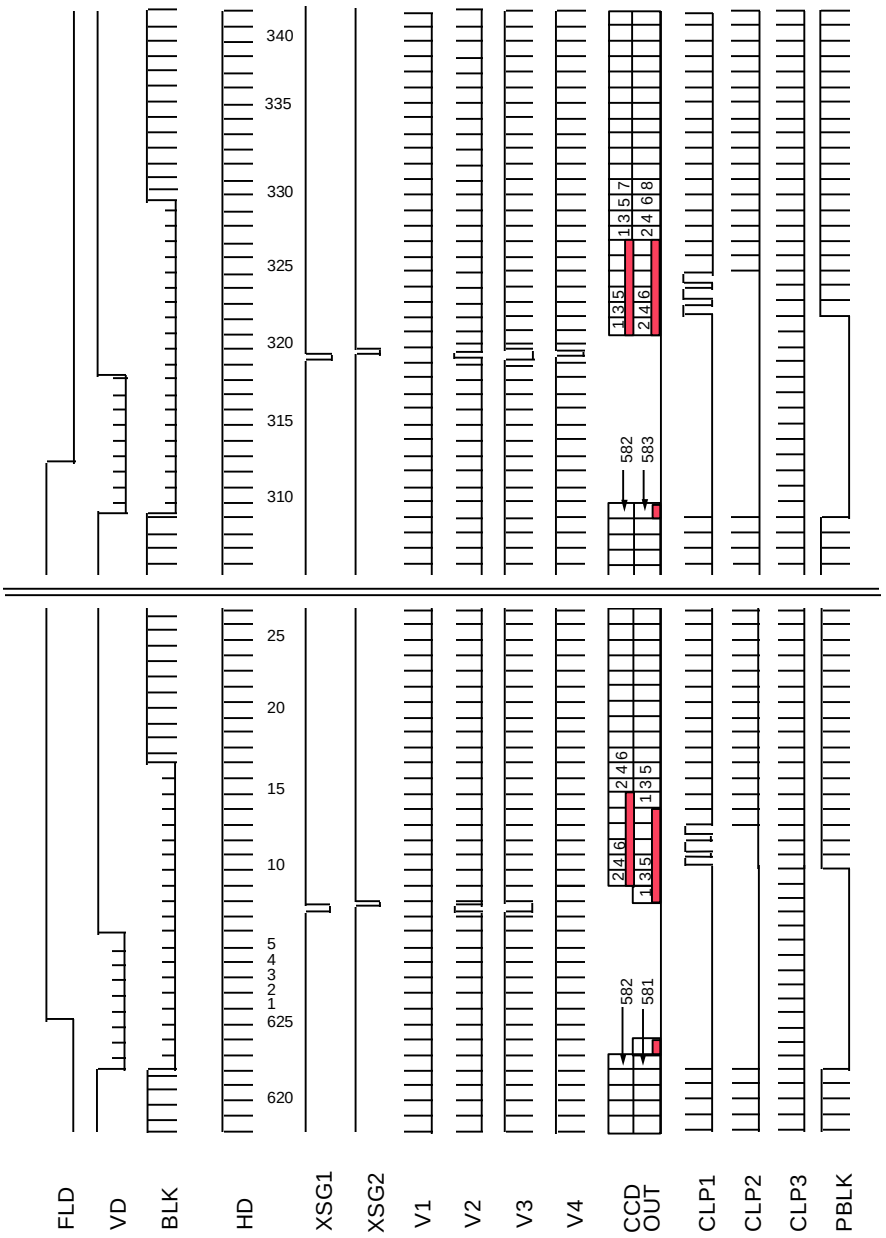
CCIR VERTICAL TIMING CHART



VERTICAL TIMING CHART FOR EIA



VERTICAL TIMING CHART FOR CCIR



PACKAGE DIMENSION

48-QFP-0707

unit : mm