

INTRODUCTION

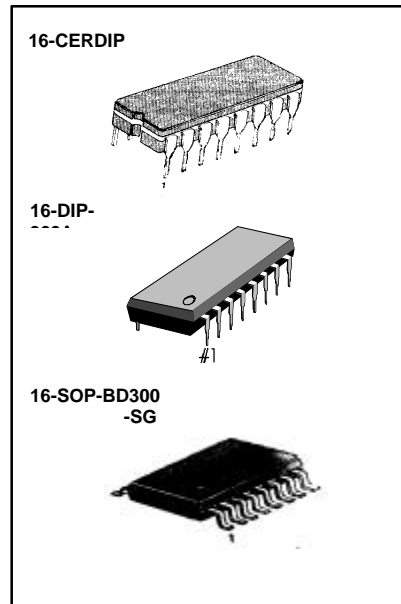
The KT8554B/7B are single-chip PCM encoders and decoders (PCM CODECS) and PCM line filters. These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplex (TDM) system.

These devices are designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering functions in PCM system. They are intended to be used at the analog termination of a PCM line or trunk.

These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signalling and supervision information.

FEATURES

- Complete CODEC and filtering system
- Meets or exceeds AT&T D3/D4 and CCITT specifications
 μ-Law : KT8554B, A-Law : KT8557B
- On-chip auto zero, sample and hold, and precision voltage references
- Low power dissipation : 60mW (operating)
 3mW (standby)
- ± 5V operation
- TTL or CMOS compatible
- Automatic power down



ORDERING INFORMATION

Device	Package	Operating Temperature
KT8554BJ KT8557BJ	16-CERDIP	- 25 ~ 125°C
KT8557BN KT8554BN	16-DIP-300A	- 25 ~ 70°C
KT8554BD KT8557BD	16-SOP-BD300 -SG	- 25 ~ 70°C

PIN CONFIGURATION

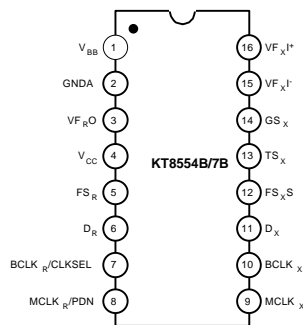


Fig. 1

PIN DESCRIPTION

Pin No	Symbol	Description
1	V _{BB}	V _{BB} = -5V ±5%.
2	GNDA	Analog ground.
3	VF _R O	Analog output of the receive power Amp.
4	V _{CC}	V _{CC} = +5V ± 5%.
5	FS _R	Receive frame sync pulse. 8KHz pulse train.
6	D _R	PCM data input.
7	BCLK _R / CLKSEL	Logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in normal operation and BCLK _x is used for both TX and RX directions. Alternately direct clock input available, very from 64KHz to 2.048MHz.
8	MCLK _R / PDN	When MCLK _R is connected continuously high, the device is powered down. Normally connected continuously low, MCLK _x is selected for all DAC timing. Alternately direct 1.536MHz/1.544MHz or 2.048MHz clock input available.
9	MCLK _x	Must be 1.536MHz/1.544MHz or 2.048MHz.
10	BCLK _x	May be vary from 64KHz to 2.048MHz but BCLK _x is externally tied with MCLK _x in normal operation.
11	D _x	PCM data output.
12	FS _x	TX frame sync pulse. 8KHz pulse train.
13	$\overline{\text{TS}}_x$	Changed from high to low during the encoder timeslot. Open drain output.
14	GS _x	Analog output of the TX input amplifier. Used to set gain through external resistor.
15	VF _x I ⁻	Inverting input stage of the TX analog signal.
16	VF _x I ⁺	Non-inverting input stage of the TX analog signal.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V _{CC}	7	V
Negative Supply Voltage	V _{BB}	- 7	V
Voltage at Any Analog Input or Output	V _{I(A)}	V _{CC} + 0.3 to V _{BB} - 0.3	V
Voltage at Any Digital Input or Output	V _{I(D)}	V _{CC} + 0.3 to GNDA - 0.3	V
Operating Temperature Range	Ta	- 25 to + 125	°C
Storage Temperature Range	T _{STG}	- 65 to + 150	°C
Lead Temperature (Soldering, 10 secs)	T _{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $G_NDA = 0V$, $T_a = 0^\circ C$ to $70^\circ C$; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_a = 25^\circ C$; all signals referenced to G_NDA).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Dissipation						
Power-Down Current	$I_{CC(DOWN)}$	No Load		0.5	1.5	mA
Power-Down Current	$I_{BB(DOWN)}$	No Load		0.05	0.3	mA
Active Current	$I_{CC(A)}$	No Load		6.0	9.0	mA
Active Current	$I_{BB(A)}$	No Load		6.0	9.0	mA
Digital Interface						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Input Low Current	I_{IL}	$G_NDA \leq V_{IN} \leq V_{IL}$, all digital inputs	-10		10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	μA
Output Low Voltage	V_{OL}	$D_X, I_L = 3.2mA$			0.4	V
		$SIG_R, I_L = 1.0mA$			0.4	V
		$\overline{TS}_X, I_L = 3.2mA, \text{open drain}$			0.4	V
Output High Voltage	V_{OH}	$D_X, I_H = -3.2mA$	2.4			V
		$SIG_R, I_H = -1.0mA$	2.4			V
Output Current in High Impedance State (TRI-STATE)	$I_{O(HZ)}$	$D_X, G_NDA \leq V_O \leq V_{CC}$	-10		10	μA
Analog Interface with Receive Filter						
Output Resistance	R_O	Pin VF_{R0}		1	3	Ω
Load Resistance	R_L	$VF_{R0} = \pm 2.5V$	600			Ω
Load Capacitance	C_L				500	pF
Output DC Offset Voltage	$V_{OO(RX)}$		-200		200	mV
Analog Interface with Transmit input Amplifier						
Input Leakage Current	I_{LKG}	$-2.5V \leq V_S \leq +2.5V, VF_X + \text{ or } VF_X -$	-200		200	nA
Input Resistance	R_i	$-2.5V \leq V_S \leq +2.5V, VF_X + \text{ or } VF_X -$	10			$M\Omega$
Output Resistance	R_O	Closed loop, unity gain		1	3	Ω
Load Resistance	R_L	GS_X	10			$K\Omega$
Load Capacitance	C_L	GS_X			50	pF
Output Dynamic Range	$V_{OD(TX)}$	$GS_X, R_L \leq 10KW$	± 2.8			V
Voltage Gain	G_V	$VF_X + \text{ to } GS_X$	5,000			V/V
Unity Gain Bandwidth	BW		1	2		MHz
Offset Voltage	$V_{IO(TX)}$		-20		20	mV
Common-Mode Voltage	$V_{CM(TX)}$	$CMRR_X > 60dB$	-2.5		2.5	V
Common-Mode Rejection Ratio	CMRR	DC Test	60			dB
Power Supply Rejection Ratio	PSRR	DC Test	60			dB

TIMING CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0 \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $GNDA = 0V$, $T_a = 0^\circ C$ to $70^\circ C$; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_a = 25^\circ C$; all signals referenced to $GNDA$.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Frequency of Master Clocks	f_{MCK}	Depends on the device used and the BCLK _R /CLKSEL Pin. MCLK _X and MCLK _R		1.536 1.544 2.048		MHz MHz MHz
Rise Time of Bit Clock	$t_{R(BCK)}$	$t_{PB} = 488ns$			50	ns
Fall Time of Bit Clock	$t_{F(BCK)}$	$t_{PB} = 488ns$			50	ns
Holding Time from Bit Clock Low to Frame Sync	$t_{H(LFS)}$	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	$t_{H(HFS)}$	Short frame only	0			ns
Set-Up Time from Frame Sync to Bit Clock Low	$t_{SU(FBCL)}$	Long frame only	80			ns
Delay Time from BCLK _X High to Data Valid	$t_{D(HDV)}$	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to \overline{TS}_X Low	$t_{D(TSKL)}$	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from BCLK _X Low to Data Output Disabled	$t_{D(LDD)}$		50		165	ns
Delay Time to Valid Data from FS _X or BCLK _X , Whichever Comes Later	$t_{D(VD)}$	$C_L = 0pF$ to $150pF$	20		165	ns
Set-Up Time from D _R Valid to BCLK _{R/X} Low	$t_{SU(DRBL)}$		50			ns
Hold Time from BCLK _{R/X} Low to D _R Invalid	$t_{H(BLDR)}$		50			ns
Set-Up Time from FS _{X/R} to BCLK _{X/R} Low	$t_{SU(FBLS)}$	Short frame sync pulse (1 or 2 bit clock periods long) (Note1)	50			ns
Width of Master Clock High	$t_{W(MCKH)}$	MCLK _X and MCLK _R	160			ns
Width of Master Clock Low	$t_{W(MCKL)}$	MCLK _X and MCLK _R	160			ns
Rise Time of Master Clock	$t_{R(MCK)}$	MCLK _X and MCLK _R			50	ns
Fall Time of Master Clock	$t_{F(MCK)}$	MCLK _X and MCLK _R			50	ns
Set-Up Time from BCLK _X High (and FS _X In Long Frame Sync Mode) to MCLK _X Falling Edge	$t_{SU(BHMF)}$	First bit clock after the leading edge of FS _X				
Period of Bit Clock	t_{CK}		485	488	15,725	ns
Width of Bit Clock High	$t_{W(BCKH)}$	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	$t_{W(BCKL)}$	$V_{IL} = 0.6V$	160			ns

TIMING CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Hold Time from BCLK _{X/R} Low to FS _{X/R} Low	$t_{H(BLFL)}$	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS _X or FS _R)	$t_{H(3rd)}$	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1 : For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

TIMING DIAGRAM

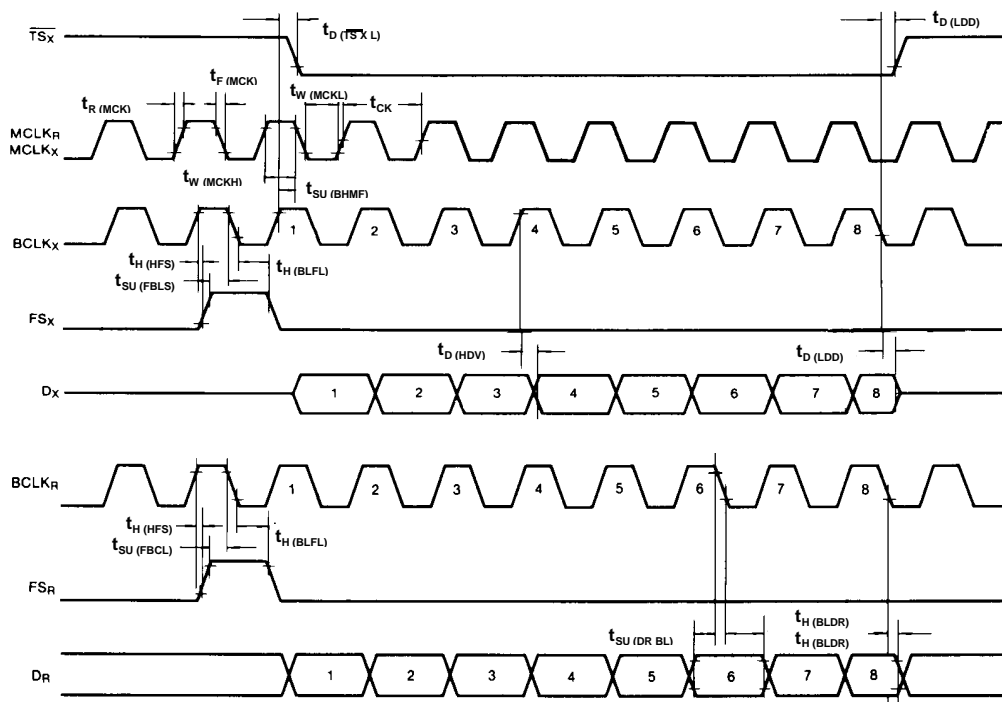


Fig. 2. Short Frame Sync Timing

TIMING DIAGRAM (Continued)

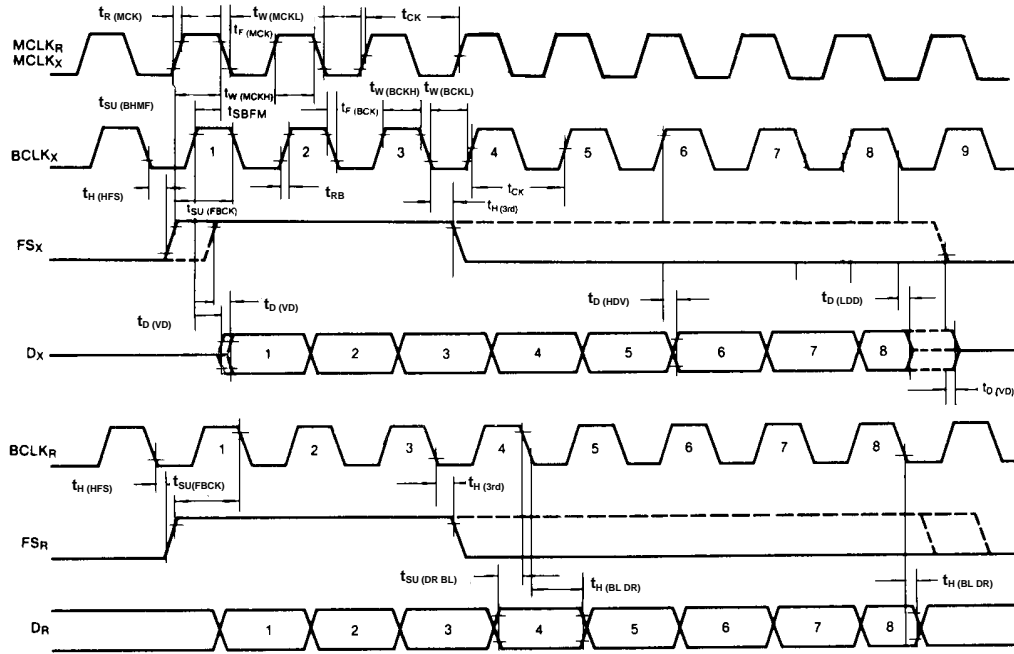


Fig. 3 Long Frame Sync Timing

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified : Ta = 0°C to 70 °C, V_{CC} = 5V ±5%, V_{BB} = -5V ±5%, G_{NDA} = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Amplitude Resposns						
Receive Gain, Absolute	G _{V (ARX)}	Ta = 25 °C, V _{CC} = 5V, V _{BB} = -5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	-0.15		0.15	dB
Receive Gain, Relative to G _{V (ARX)}	G _{V (RRX)}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	-0.15 -0.35 -0.7		0.15 0 -14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	$\Delta G_{V (ARX)} / \Delta T$	Ta = 0 °C to 70 °C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	$\Delta G_{V (ARX)} / \Delta V$	V _{CC} = 5V ±5%, V _{BB} = -5V ±5%			±0.05	dB
Receive Gain Variations with Level	$\Delta G_{V (RXL)}$	Sinusoidal test method ; reference input PCM code corresponds to an Ideally encoded -10dBm0 signal PCM level = -40dBm0 to +3dBm0 PCM level = -50dBm0 to -40dBm0 PCM level = -55dBm0 to -50dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
Receive Output Drive Level	V _{O (RX)}	R _L = 600Ω	-2.5		2.5	V
Absolute Levels	V _{AL}	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V _{rms}
Max Overload Level	V _{OL (MAX)}	Max overload level (3.17dBm0): KT8554B Max overload level (3.14dBm0): KT8557B		2.501		V _{PK}
Transmit Gain, Absolute	G _{V (ATX)}	Ta = 25 °C, V _{CC} = 5V, V _{BB} = -5V Input at GS _X = 0dBm0 at 1020Hz	-0.15		0.15	dB
Transmit Gain, Relative to G _{V (ATX)}	G _{V (RTX)}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz - 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	-1.8 -0.15 -0.35 -0.7		-40 -30 -26 -0.1 0.15 0.05 0 -14 -32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	$\Delta G_{V (ATX)} / \Delta T$	Ta = 0 °C to 70 °C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	$\Delta G_{V (ATX)} / \Delta V$	V _{CC} = 5V ±5%, V _{BB} = -5V ±5%			±0.05	dB
Transmit Gain Variations with Level	$\Delta G_{V (TXL)}$	Sinusoidal test method Reference level = - 10dBm0 VF _{X1} + = - 40dBm0 to + 3dBm0 VF _{X1} - = - 50dBm0 to - 40dBm0 VF _{X1} + = - 55dBm0 to - 50dBm0	- 0.2 - 0.4 - 1.2		0.2 0.4 1.2	dB dB dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Receive Delay, Absolute	$t_{D(ARX)}$	f = 1600Hz		180	200	μ S
Receive Delay, Relative to $t_{D(ARX)}$	$t_{D(RRX)}$	f = 500Hz - 1000Hz	-40	-25		μ S
		f = 1000Hz - 1600Hz	-30	-20		μ S
		f = 1600Hz - 2600Hz		70	90	μ S
		f = 2600Hz - 2800Hz		100	125	μ S
		f = 2800Hz - 3000Hz		145	175	μ S
Transmit Delay, Absolute	$t_{D(ATX)}$	f = 1600Hz		290	315	μ S
Transmit Delay, Relative to $t_{D(ATX)}$	$t_{D(RTX)}$	f = 500Hz - 600Hz		195	220	μ S
		f = 600Hz - 800Hz		120	145	μ S
		f = 800Hz - 1000Hz		50	75	μ S
		f = 1000Hz - 1600Hz		20	40	μ S
		f = 1600Hz - 2600Hz		55	75	μ S
		f = 2600Hz - 2800Hz		80	105	μ S
		f = 2800Hz - 3000Hz		130	155	μ S
Noise						
Receive Noise, C Message Weighted	N_{RXC}	PCM code equals alternating positive and negative zero, KT8554B		8	11	dBrnc0
Receive Noise, P Message Weighted	N_{RXP}	PCM code equals, positive zero, KT8557B		-82	-79	dBm0p
Transmit Noise, C Message Weighted	N_{TXC}	KT8554B		12	15	dBrnc0
Transmit Noise, P Message Weighted	N_{TXP}	KT8557B		74	-67	dBm0p
Noise, Single Frequency	N_{SF}	f = 0KHz to 100KHz, loop around measurement, $V_{F_x I} + = 0V_{rms}$			-53	dBm0
Positive Power Supply Rejection, Transmit	PSRR (PTX)	$V_{F_x I} + = 0V_{rms}$ $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz - 50KHz	40			dB
Negative Power Supply Rejection, Transmit	PSRR (NTX)	$V_{F_x I} + = 0V_{rms}$ $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz - 50KHz	40			dB
Positive Power Supply Rejection, Receive	PSRR (PRX)	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz - 4000Hz	40			dB
		f = 4KHz - 25KHz	40			dB
		f = 25KHz - 50KHz	36			dB
Negative Power Supply Rejection, Receive	PSRR (NRX)	PCM code equals positive zero $V_{BB} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz - 4000Hz	40			dB
		f = 4KHz - 25KHz	40			dB
		f = 25KHz - 50KHz	36			dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz - 3400Hz input PCM applied to D_R . Measure individual image signals at V_{F_xO}				
		4600Hz - 760Hz			-32	dB
		7600Hz - 8400Hz			-40	dB
		8400Hz - 100,000Hz			-32	dB
Distortion						
Signal to Total Distortion Transmit or Receive Half-Channel	THD _{TX} THD _{RX}	Sinusoidal test method Level = 3.0dBm0	33			dB
		= 0dBm0 to 30dBm0	26			dB
		= -40dBm0 XMT	29			dB
		RCV	30			dB
		= -55dBm0 XMT	14			dB
RCV	15			dB		
Single Frequency Distortion, Transmit	THD _{SF(TX)}				-46	dB
Single Frequency Distortion, Receive	THD _{SF(RX)}				-46	dB
Intermodulation Distortion	THD _{IMD}	Loop around measurement, $V_{F_xI} = -4dBm0$ to $-21dBm0$, two frequencies in the range 300Hz - 3400Hz			-41	dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit Level	CT _(TX-RX)	f = 300Hz - 3400Hz D_R = Steady PCM code		-90	-75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive Level	CT _(RX-TX)	f = 300Hz - 3400Hz, $V_{F_xI} = 0V$		-90	-70 (Note1)	dB

Note 1. CT_(RX-TX) is measured with a -40dBm0 activating signal applied at $V_{F_xI} +$

ENCODING FORMAT AT D_x OUTPUT

	m-Law KT8554B	A-Law KT8557B
V_{IN} (at GS_x) = + Full Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_x) = 0V	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
V_{IN} (at GS_x) = - Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0



APPLICATION CIRCUIT

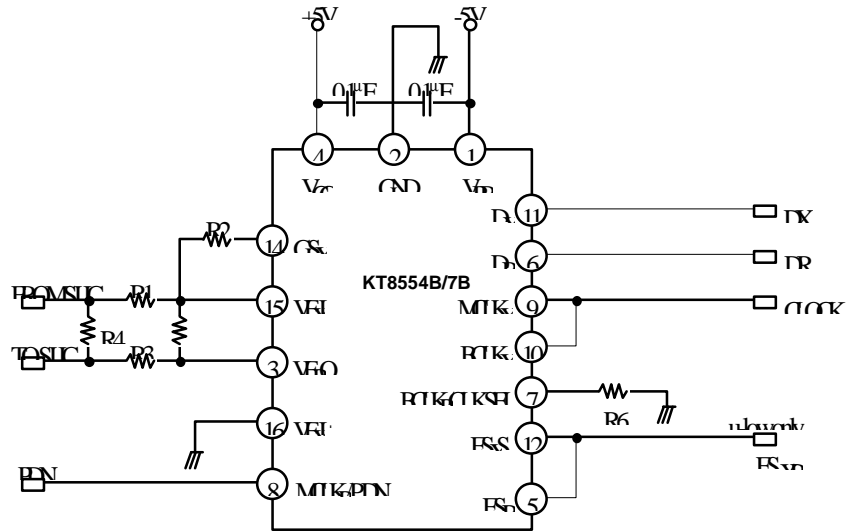


Fig. 4

NOTE 1 : Supposing Desired Line Termination Impedance $R_L = 600\text{ohm}$
It is $0\text{dBm} = 0.77459\text{Vrms}$

NOTE 2 : $T_x \text{Gain } 20 \log (R2/R1)$, $R1 + R2 < 100\text{Kohm}$, or The Correspondence of 1-CHIP CODEC $0\text{dBm } 0 = 4\text{dBm}$.

SELECTION OF MASTER CLOCK FREQUENCY

BCLKR/CLKSEL	KT 8554	KT 8557
Clocked	1.536 / 1.544 MHz	2.048MHz
0	2.048 MHz	1.536 / 1.544 MHz
1 (or open)	1.536 / 1.544 MHz	2.048MHz