1 PRODUCT OVERVIEW

OVERVIEW

The S3C72G9 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With an up-to-896-dot LCD direct drive capability, and flexible 8-bit timer/counters, the S3C72G9 offers an excellent design solution for a high-end LCD game.

Up to 12 pins of the 100-pin QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events. In addition, the S3C72G9's advanced CMOS technology provides for low power consumption.

OTP

The S3C72G9 microcontroller is also available in OTP (One Time Programmable) version, S3P72G9. S3P72G9 microcontroller has an on-chip 32 K-byte one-time-programmable EPROM instead of masked ROM. The S3P72G9 is comparable to S3C72G9, both in function and in pin configuration.

FEATURES

Memory

- 768 × 4-bit RAM (excluding LCD display RAM)
- 32,768 × 8-bit ROM

12 I/O Pins

- I/O: 12 pins

LCD Controller/Driver

- 56 segments and 16 common terminals
  (8, 12 and 16 common selectable)
- Capacitor bias for LCD output.
- Voltage booster and regulator
- All dots can be switched on/off

8-bit Basic Timer

- 4 interval timer functions
- Watch-dog timer

One 16-bit Timer/Counter 1

- Programmable 16-bit timer
- Arbitrary clock output (TCLO1)
- Inverted clock output (TCLO1)
- Configurable two 8-bit timer/counters

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms
  at 32768 Hz
- Four frequency outputs to BUZ pin and BUZ pin
- Clock source generation for LCD

Battery Level Detector

- Programmable low voltage detector
- One criteria voltage (2.4 V)

Interrupts

- Three Internal vectored interrupt
- Four external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Subsystem clock stop mode

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 0.4-4.19 MHz
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz (main)
- 122 µs at 32.768 kHz (subsystem)

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.2 V to 3.4 V (0.4 MHz to 4.19 MHz)

Package Type

- 100-pin QFP or pellet

BLOCK DIAGRAM

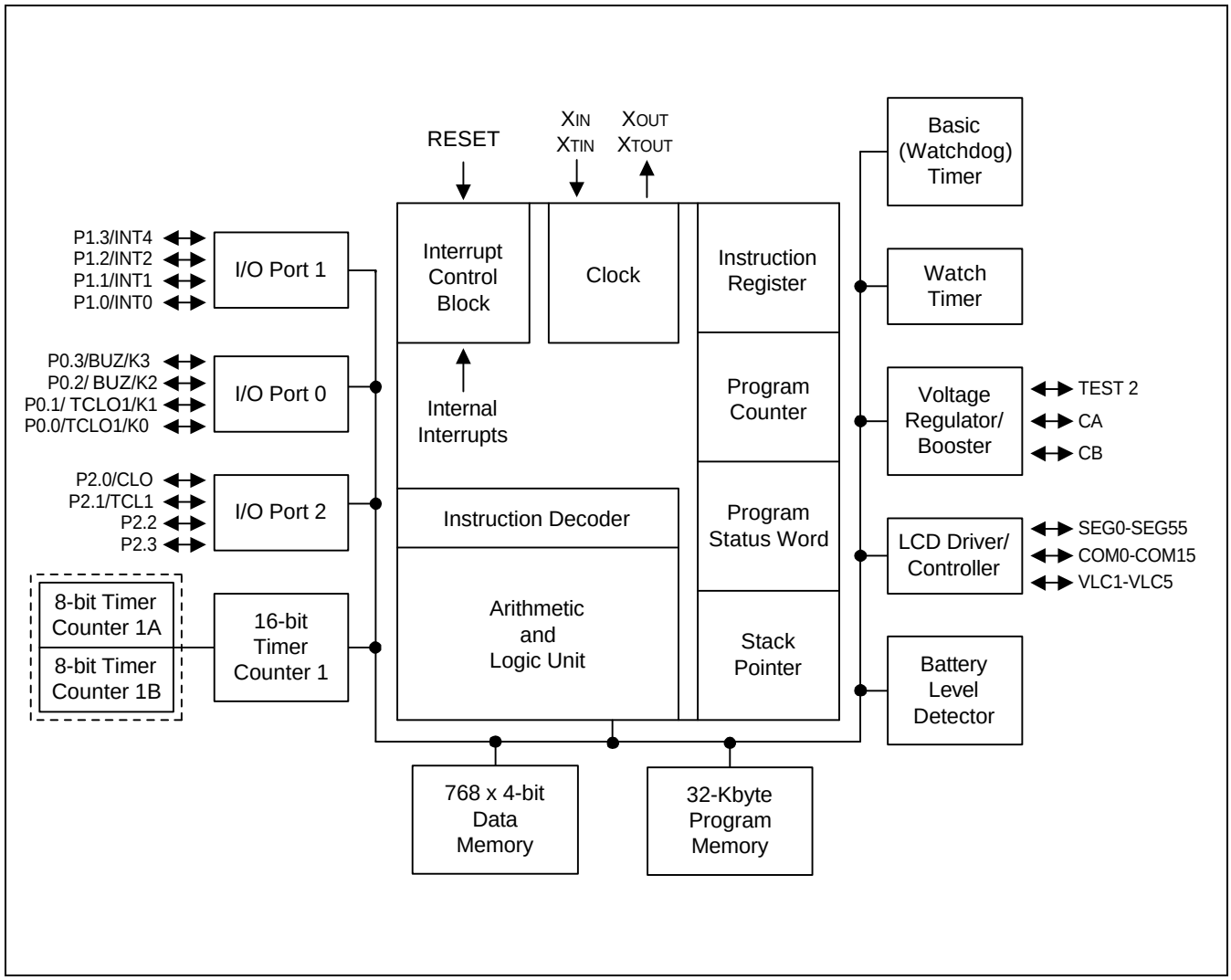


Figure 1-1. S3C72G9 Simplified Block Diagram

PIN ASSIGNMENTS

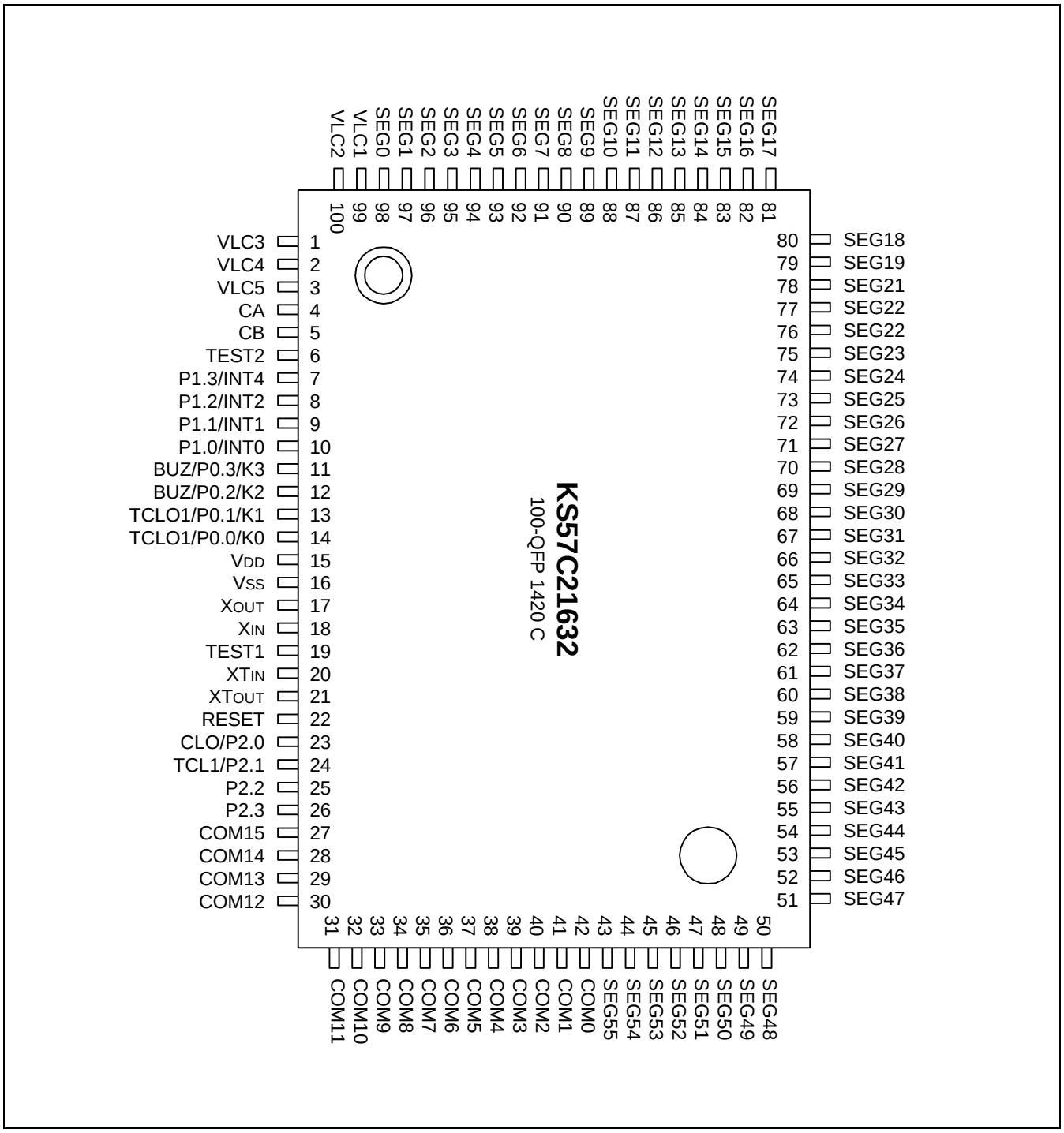


Figure 1-2. S3C72G9 100-QFP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. S3C72G9 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. Individual pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	14 13 12 11	TCLO1/K0 TCLO1/K1 BUZ/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I/O	Same as port 0	10 9 8 7	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0	23 24 25 26	CLO TCL1
INT0, INT1	I/O	External interrupts. The triggering edge for INT0 and INT1 is selectable.	10, 9	P1.0, P1.1
INT2	I/O	Quasi-interrupt with detection of rising or falling edges.	8	P1.2
INT4	I/O	External interrupt with detection of rising and falling edges.	7	P1.3
BUZ	I/O	2 kHz, 4 kHz, 8 kHz or 16 kHz frequency output for buzzer signal.	11	P0.3/K3
BUZ	I/O	Inverted BUZ signal	12	P0.2/K2
CLO	I/O	Clock output	23	P2.0
TCL1	I/O	External clock input for timer/counter 1	24	P2.1
TCLO1	I/O	Timer/counter 1 inverted clock output	13	P0.1/K1
TCLO1	I/O	Timer/counter 1 clock output	14	P0.0/K0
COM0–COM15	O	LCD common signal output	42-27	–
SEG0–SEG55	O	LCD segment signal output	98-43	–

Table 1-1. S3C72G9 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
K0–K3	I/O	External interrupt (triggering edge is selectable)	14–11	P0.0–P0.3
V_{DD}	–	Main power supply	15	–
V_{SS}	–	Ground	16	–
RESET	I	Reset signal	22	–
CA, CB	–	Capacitor terminal for voltage boosting	4, 5	–
VCL1–VCL2 VCL3–VCL5	–	LCD power supply	99–100 1–3	–
TEST2	I	Test input (must be connected V_{SS})	6	–
X_{IN}, X_{OUT}	–	Crystal, ceramic or RC oscillator pins for system clock	18, 17	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock	20, 21	–
TEST1	I	Test input (must be connected to V_{SS}) (2)	19	–

NOTES

1. Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.
2. Refer to chapter 16 for OTP version.

Table 1-2. Overview of S3C72G9 Pin Data

Pin Name	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	TCLO1/K0, TCLO1/K1 BUZ/K2, BUZ/K3	I/O	Input	E-2
P1.0–P1.3	INT0, INT1, INT2, INT4	I/O	Input	E-2
P2.0–P2.1	CLO, TCL1	I/O	Input	E-2
P2.2–P2.3	–	I/O	Input	E-2
COM0–COM15	–	O	Low	H-6
SEG0–SEG55	–	O	Low	H-6
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
RESET	–	I	–	B
CA	–	–	–	–
CB	–	–	–	–
VLC1–VLC5	–	–	–	–
X_{IN}, X_{OUT}	–	–	–	–
XT_{IN}, XT_{OUT}	–	–	–	–
TEST1, 2	–	I	–	–

PIN CIRCUIT DIAGRAMS

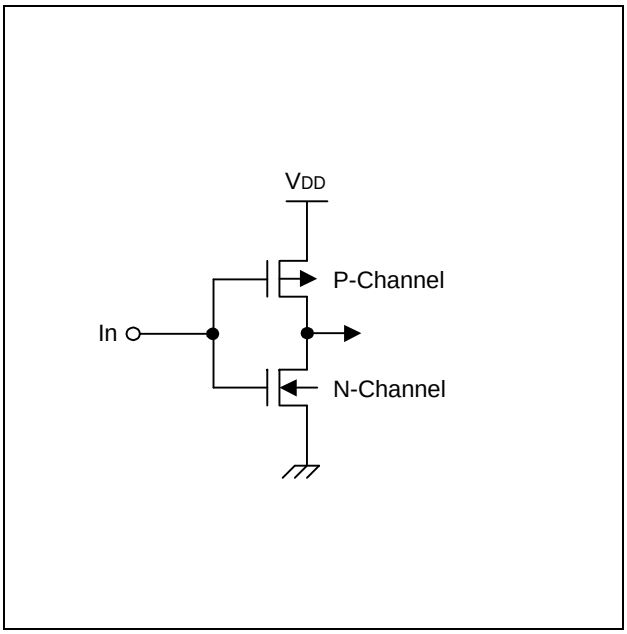


Figure 1-3. Pin Circuit Type A

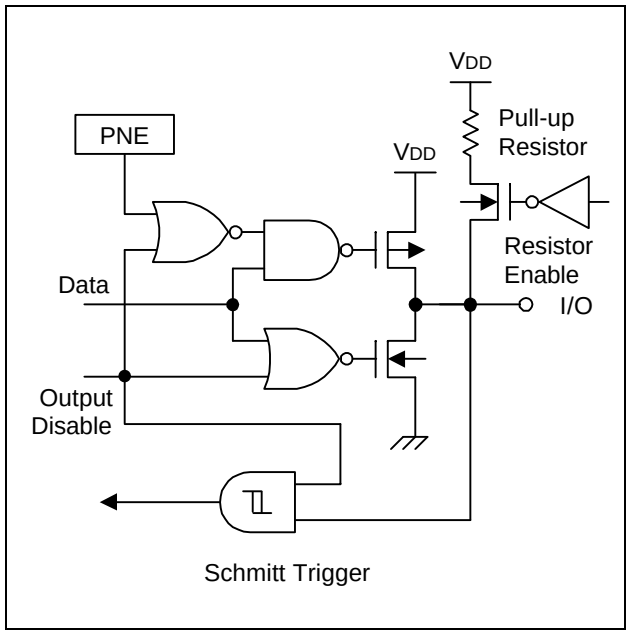


Figure 1-5. Pin Circuit Type E-2

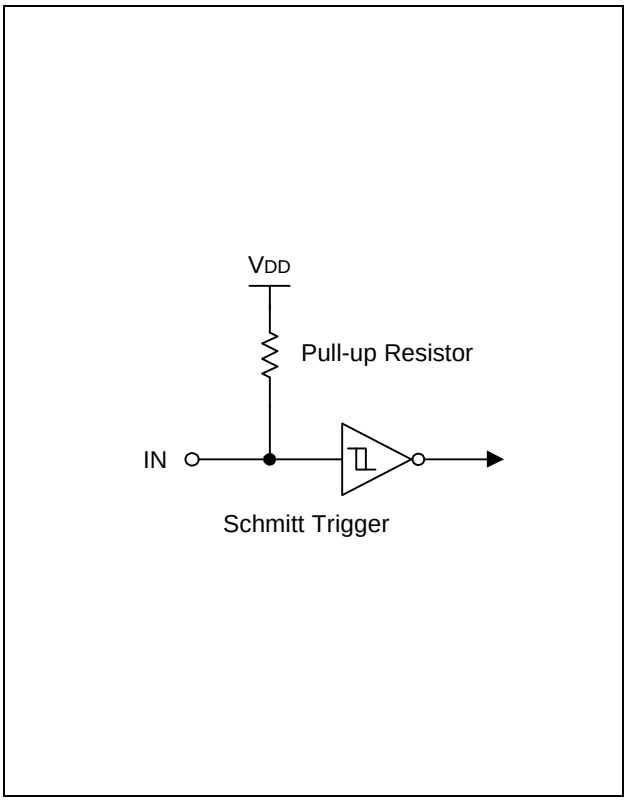


Figure 1-4. Pin Circuit Type B

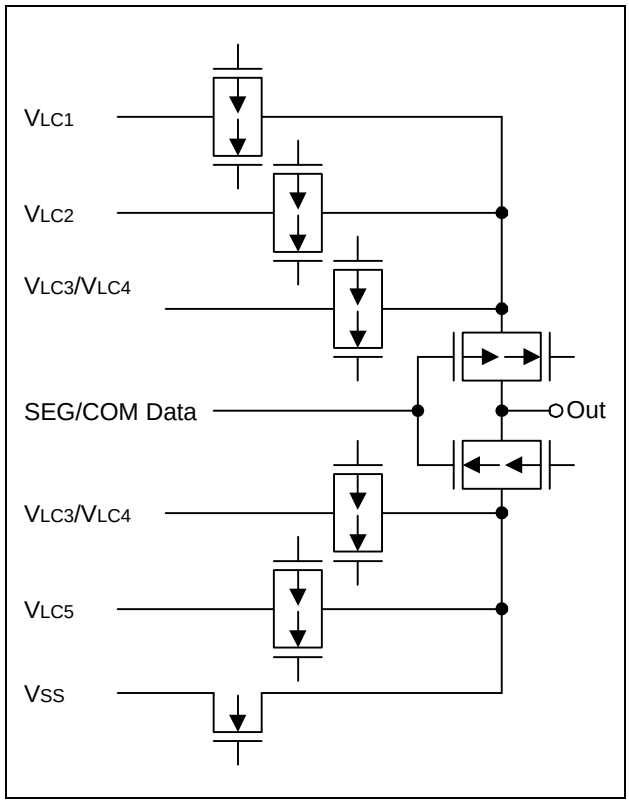


Figure 1-6. Pin Circuit Type H-6

14 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C72G9 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Main system clock oscillator characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— Battery level detector characteristics
— Voltage booster characteristics
— A.C. electrical characteristics
— Operating voltage range

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{IN}
— Clock timing measurement at XT_{IN}
— Input timing for RESET signal
— Input timing for external interrupts and quasi-interrupts

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 4.5	V
Input Voltage	V_I	Ports 0–2	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O pins active	– 30	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	mA
			+ 15 (note)	
		Total for pins 0, 1	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 0, 1, 2, and RESET	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}, X_{OUT}, and XT_{IN}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	Ports 0, 1, 2, and RESET	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}, X_{OUT}, and XT_{IN}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 2.2 V to 3.4 V I_{OH} = – 1 mA Ports 0, 1, 2	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 2.2 V to 3.4 V I_{OL} = 5 mA Ports 0, 1, 2	–	–	1.0	V

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ RESET, X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except RESET, X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}			– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 3 V, Ports 0–2	50	100	200	kΩ
	R_{L2}	V_I = 0 V; V_{DD} = 3 V, RESET	200	450	800	
$\|V_{LCD}–COMi\|$ Voltage Drop (i = 0–15)	V_{DC}	V_{LCD} = 5.0 V – 15 µA per common pin	–	–	120	mV
$\|V_{LCD}–SEGx\|$ Voltage Drop (i = 0–55)	V_{DS}	V_{LCD} = 5.0 V – 15 µA per common pin	–	–	120	

Table 14-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

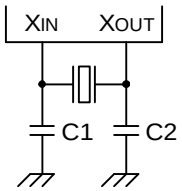
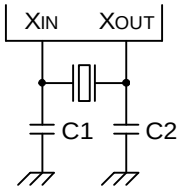
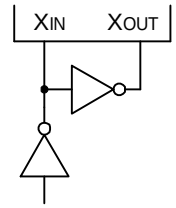
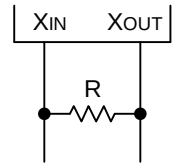
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	V_{DD} = 3 V ± 10% crystal oscillator C1 = C2 = 22 pF	4.19 MHz (PCON = 3H)	–	1.2	3	mA
	I_{DD2}	Idle mode; V_{DD} = 3 V ± 10% crystal oscillator C1 = C2 = 22 pF	4.19 MHz (PCON = 3H)	–	0.4	1	mA
	I_{DD3} (2)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4} (2)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator (LCD off)		–	6	15	µA
	I_{DD5}	Stop mode; V_{DD} = 3 V ± 10%	SCMOD = 0000B, XT_{IN} = 0 V	–	0.5	3	µA
		Stop mode; V_{DD} = 3 V ± 10%	SCMOD = 0000B		0.2	2	

NOTES:

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
3. Current in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage booster circuit, and output port drive currents.

Table 14-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	4.19	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range; V_{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	4.19	MHz
		Stabilization time (2)	V_{DD} = 3 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	–	0.4	–	4.19	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Frequency	V_{DD} = 3 V	0.4	–	2	MHz

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Recommended Oscillator Constants

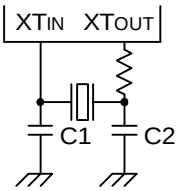
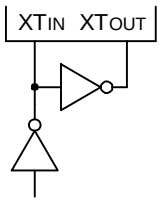
(T_A = – 40 °C + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.2	3.4	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.2	3.4	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.2	3.4	On-chip C SMD Type

NOTES:
1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 14-5. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 3.0 V	–	1.0	3	s
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 14-6. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 14-7. Battery Level Detector Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
BLD Voltage	VB0	BLC = 0 (when BREF = #05H)	2.2	2.4	2.6	V
BLD Circuit Response Time	TB	fw = 32.768 kHz	–	–	1	ms
BLD Operating Current	IBL	–	–	–	10	µA

Table 14-8. Voltage Booster Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V, C1 = C2 = C3 = C4 = 0.1 µF, CA/CB = 0.1 µF)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Liquid Crystal Drive Voltage (1)	V_{LC5}	Connect a 1 MΩ load resistance between V_{SS} and V_{LC5} (2) (no panel load)	LCR = 0	Typ × 0.9	0.85	Typ × 1.1	V
			LCR = 1		0.90		
			LCR = 2		0.95		
			LCR = 3		1.00		
			LCR = 4		1.05		
			LCR = 5		1.10		
			LCR = 6		1.15		
			LCR = 7		1.20		
	$V_{LC4/3}$	Connect a 1 MΩ load resistance between V_{SS} and $V_{LC4/3}$ (2) (no panel load)		$2 \times V_{LC5} \times 0.9$	–	$2 \times V_{LC5} \times 1.1$	
	V_{LC2}	Connect a 1 MΩ load resistance between V_{SS} and V_{LC2} (2) (no panel load)		$3 \times V_{LC5} \times 0.9$	–	$3 \times V_{LC5} \times 1.1$	
	V_{LC1}	Connect a 1 MΩ load resistance between V_{SS} and V_{LC1} (2) (no panel load)		$4 \times V_{LC5} \times 0.9$	–	$4 \times V_{LC5} \times 1.1$	
Voltage Regulator & Booster Consumed Current	IVB	V_{DD} = 3 V LCR = 7 Display on (LCON = 3H)		–	5.0	10	µA

NOTES:
1. The operating voltage of booster ranges from 2.4 V to 3.4 V.
2. The 1 MΩ load resistance is connected only to selected symbol (VLC1–VLC5) conditions to measure the properties of the circuit.

Table 14-9. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t_{CY}	V_{DD} = 2.2 V to 3.4 V	0.95	–	64	µs
		With subsystem clock (fxt)	114	122	125	
Interrupt Input High, Low Width	f_{INTH}, f_{INTL}	INT0–INT2, INT4 K0–K3, TLC1	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

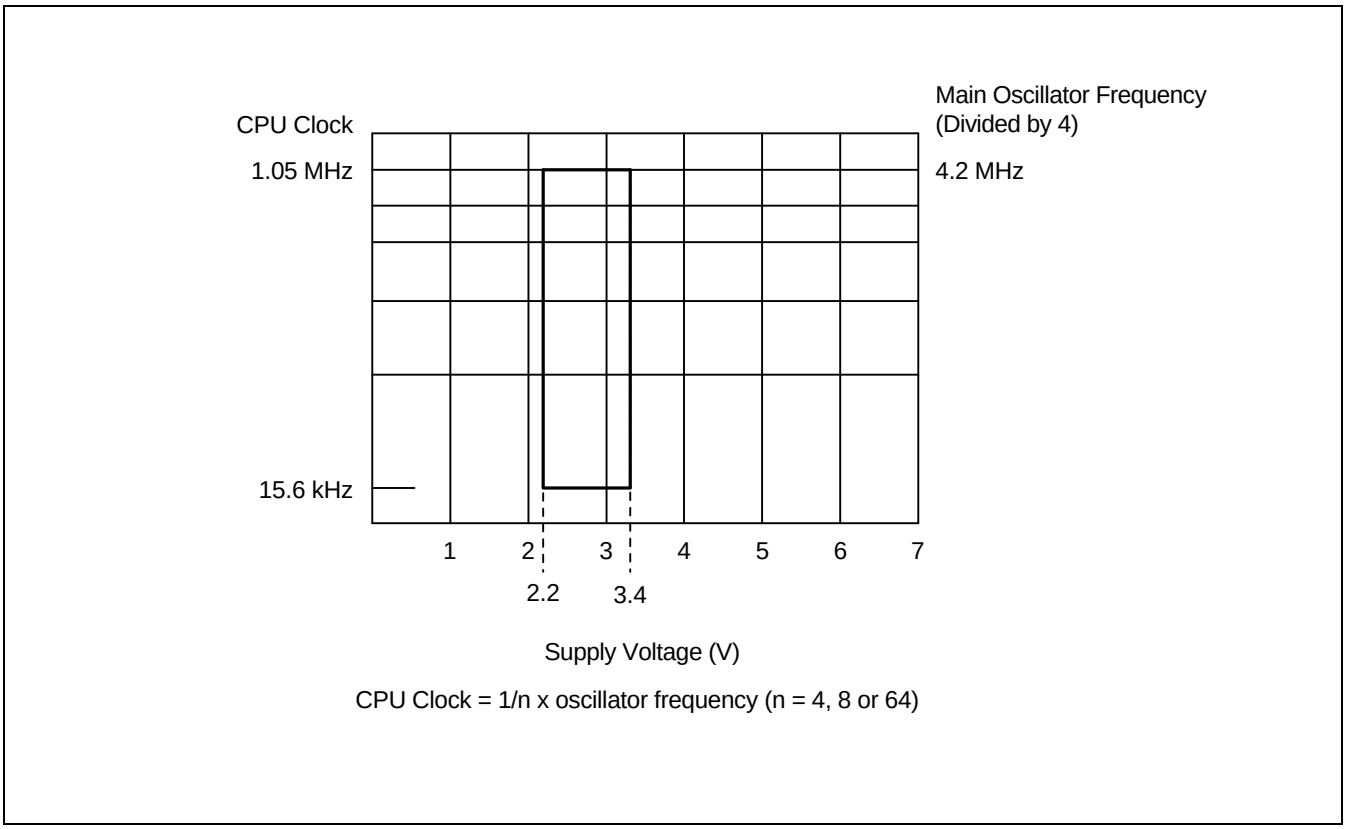


Figure 14-1. Standard Operating Voltage Range

Table 14-10. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	3.4	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.2 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

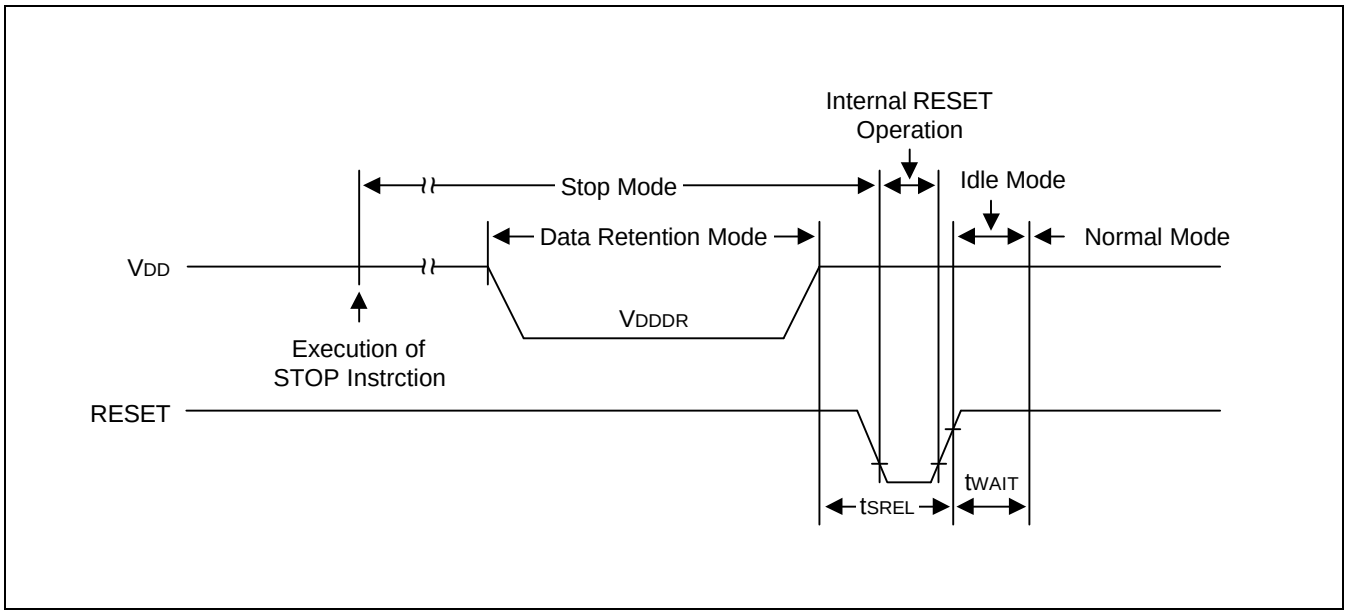


Figure 14-2. Stop Mode Release Timing When Initiated by RESET

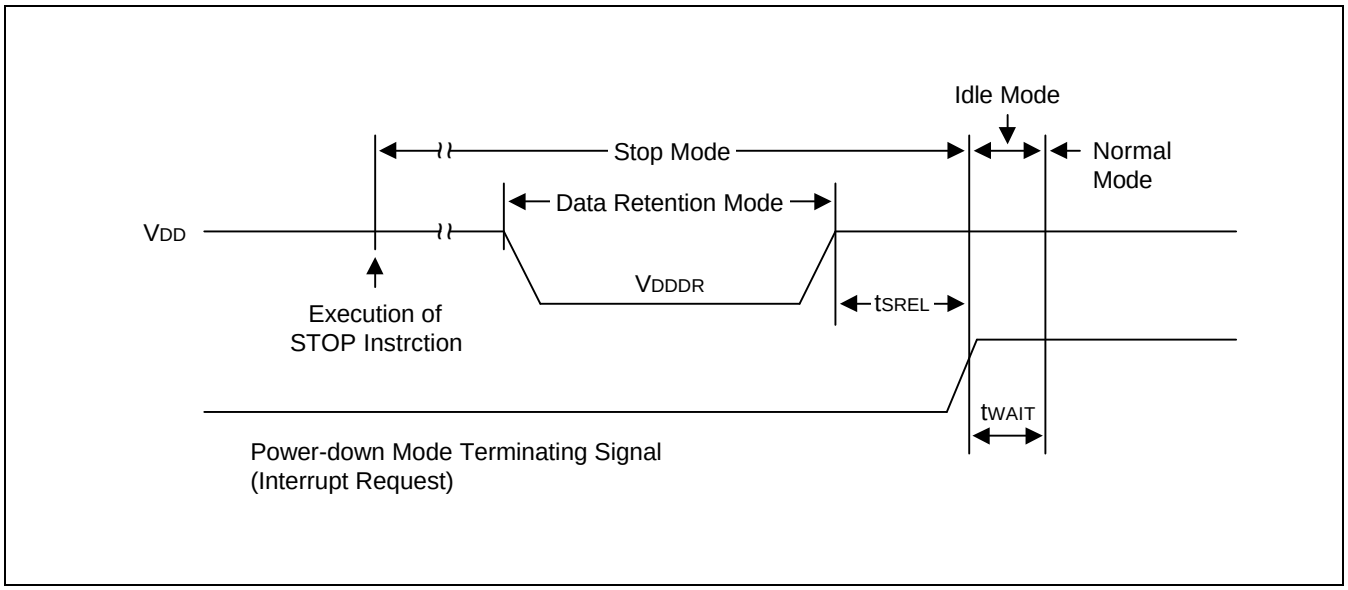


Figure 14-3. Stop Mode Release Timing When Initiated by Interrupt Request

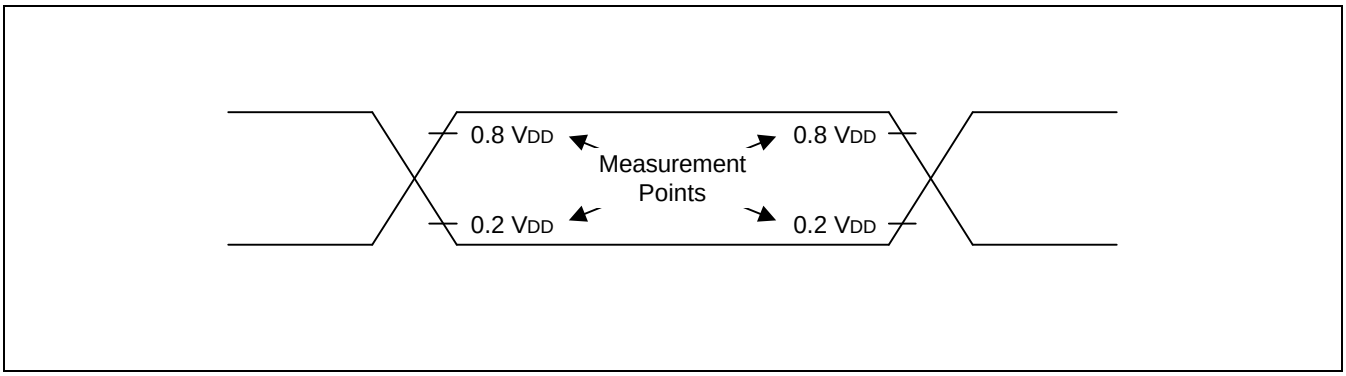


Figure 14-4. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

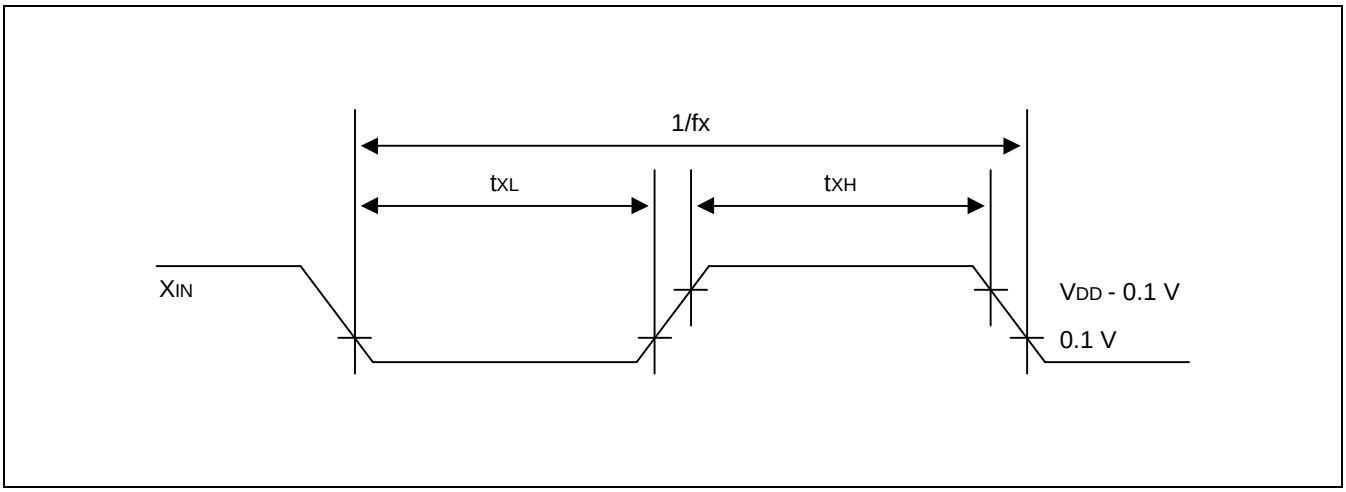


Figure 14-5. Clock Timing Measurement at X_{IN}

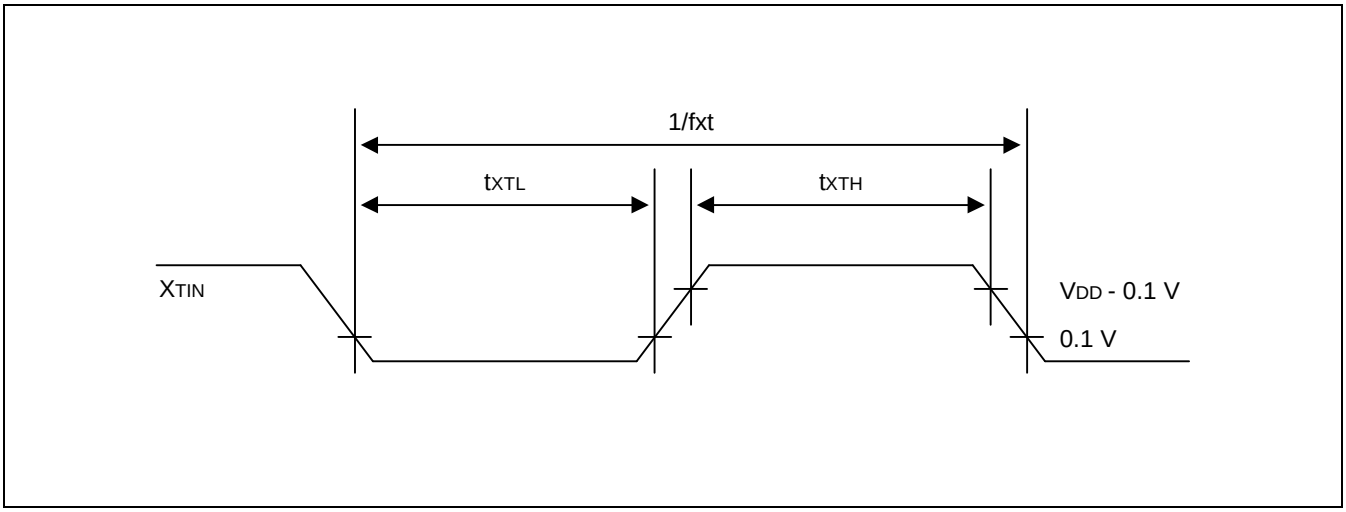


Figure 14-6. Clock Timing Measurement at XT_{IN}

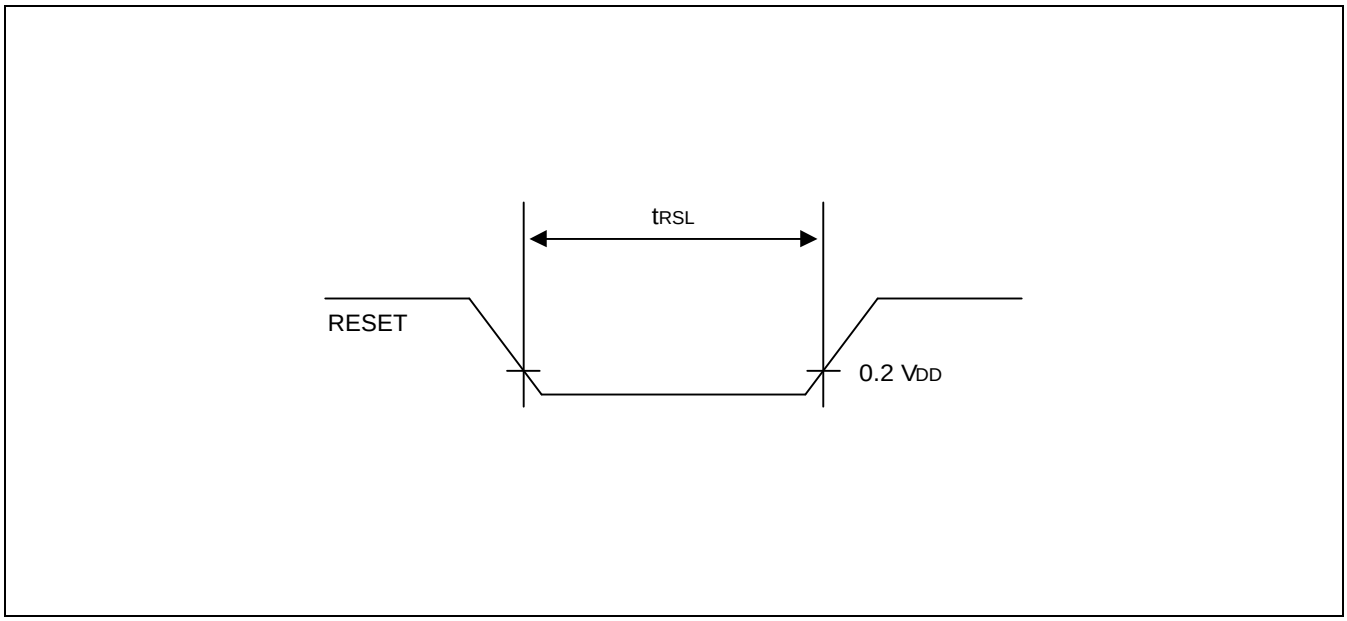


Figure 14-7. Input Timing for RESET Signal

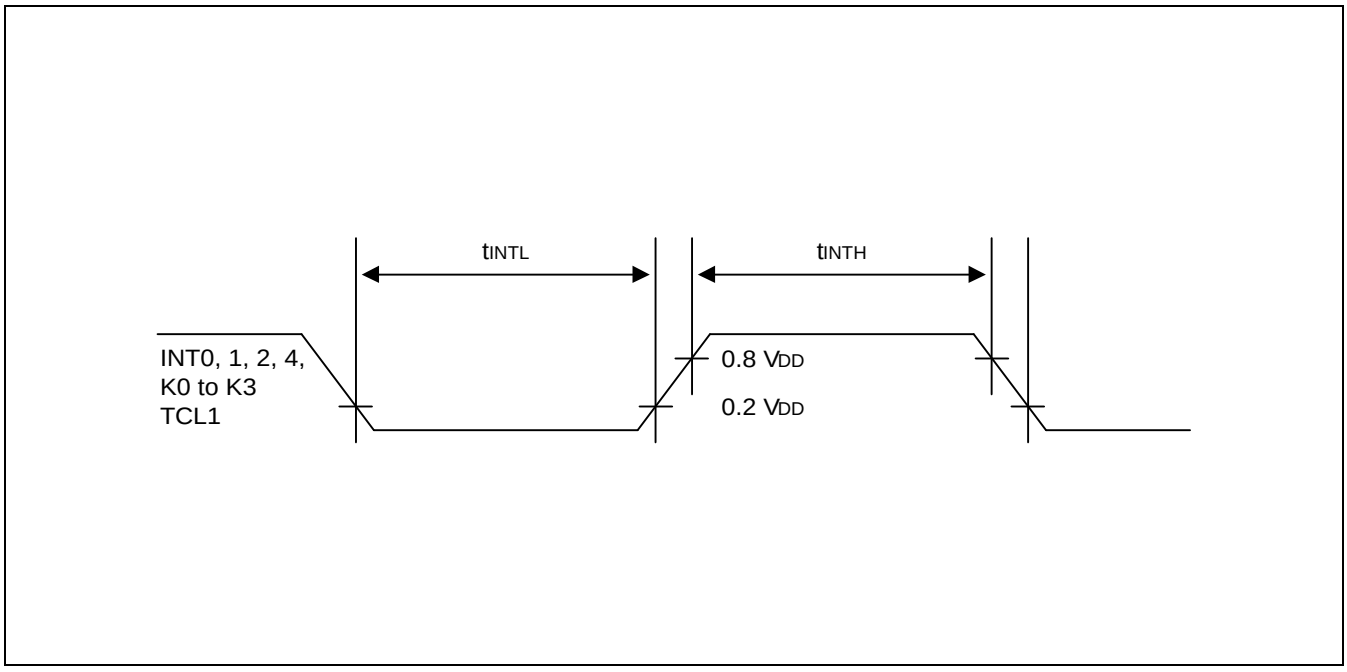


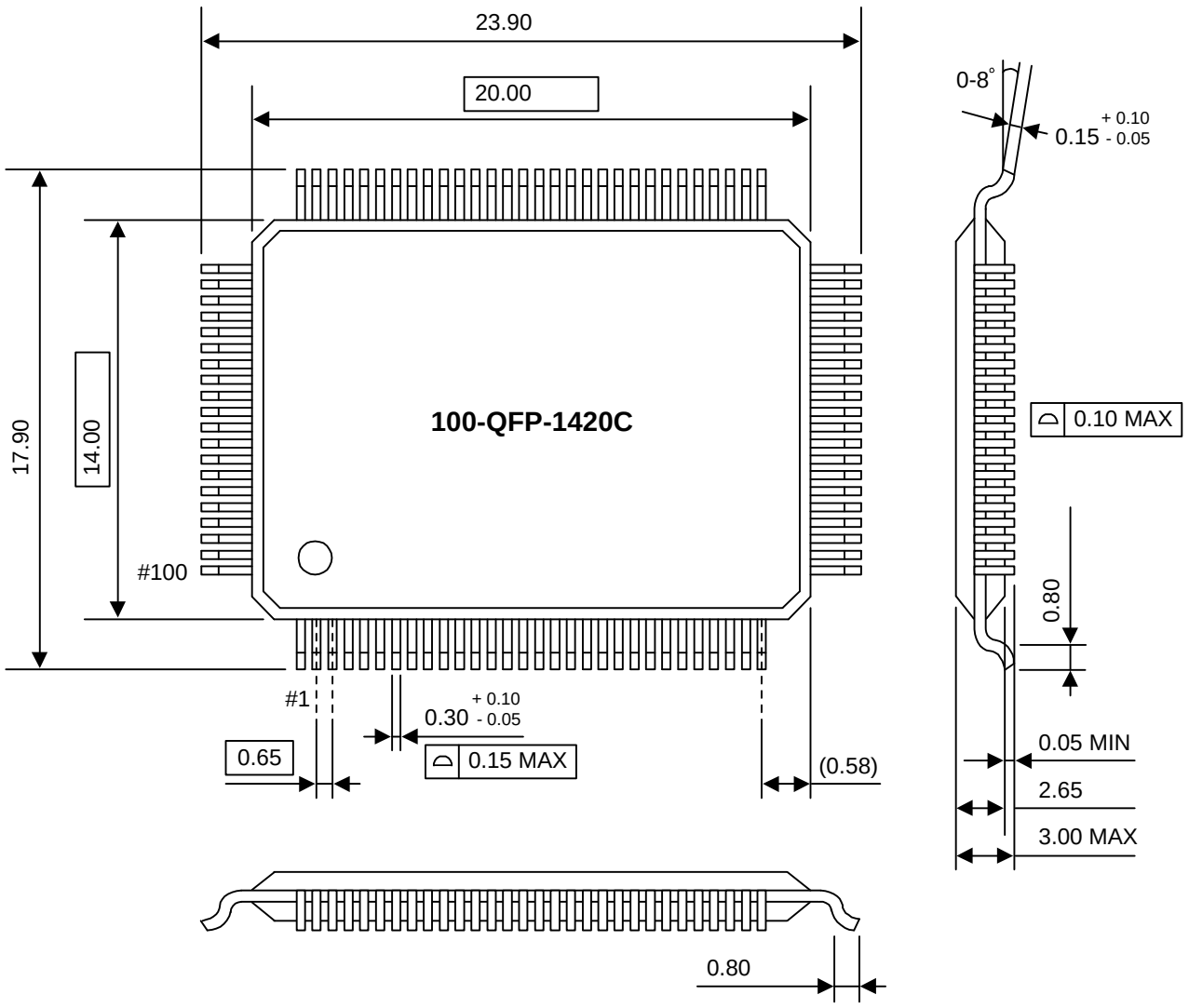
Figure 14-8. Input Timing for External Interrupts

15 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters



NOTE: Dimensions are in millimeters.

Figure 15-1. 100-QFP-1420C Package Dimensions

16 S3P72G9 OTP

OVERVIEW

The S3P72G9 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72G9 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P72G9 is fully compatible with the S3C72G9, both in function and in pin configuration.
Because of its simple programming requirements, the S3P72G9 is ideal for use as an evaluation chip for the S3C72G9.

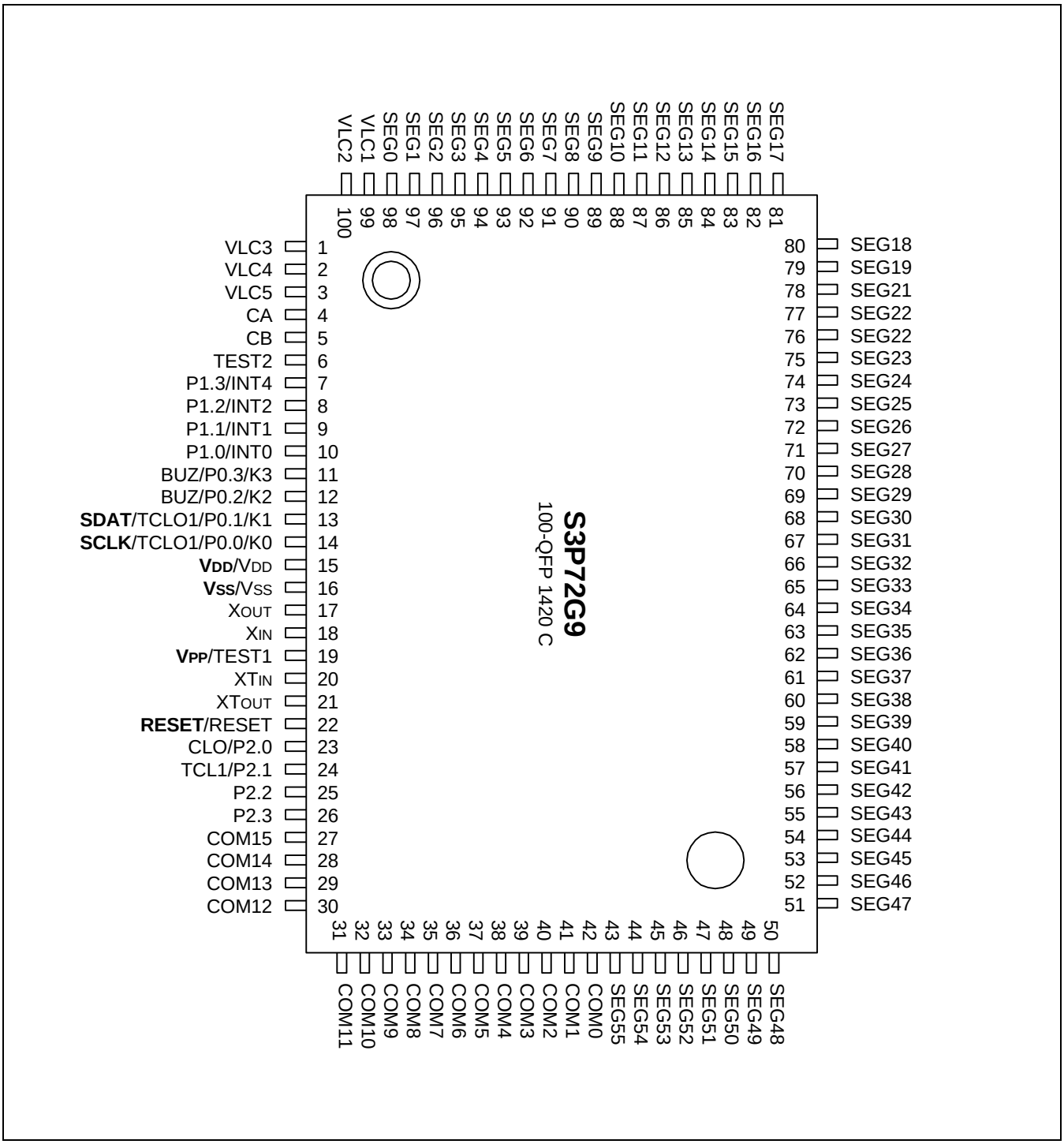


Figure 16-1. S3P72G9 Pin Assignments (100-QFP Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.1	SDAT	13	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P0.0	SCLK	14	I/O	Serial clock pin. Input only pin.
TEST	V_{PP} (TEST1)	19	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	22	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	15/16	I	Logic power supply pin. VDD should be tied to +5 V during programming.

Table 16-2. Comparison of S3P72G9 and S3C72G9 Features

Characteristic	S3P72G9	S3C72G9
Program Memory	32 Kbyte EPROM	32 Kbyte mask ROM
Operating Voltage (V_{DD})	2.2 V to 3.4 V	2.2 V to 3.4 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST1) = 12.5 V	–
Pin Configuration	100 QFP	100 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST1) pin of the S3P72G9, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST1)	REG/MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 16-4. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	V_{DD} = 3 V ± 10% 4.19 MHz (PCON = 3H) crystal oscillator C1 = C2 = 22 pF		–	1.2	3.0	mA
	I_{DD2}	Idle mode; V_{DD} = 3 V ± 10% 4.19 MHz (PCON = 3H) crystal oscillator C1 = C2 = 22 pF			0.4	1.0	
	I_{DD3} (2)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4} (2)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			6	1.5	
	I_{DD5}	Stop mode; V_{DD} = 3 V ± 10%	SCMOD = 0000B, XT_{IN} = 0 V		0.5	3	
		Stop mode; V_{DD} = 3 V ± 10%	SCMOD = 0100B		0.2	2	

NOTES:

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
3. Current in the following circuits are not included; on-chip pull-up resistors, voltage boosting capacitors, and output port drive currents.

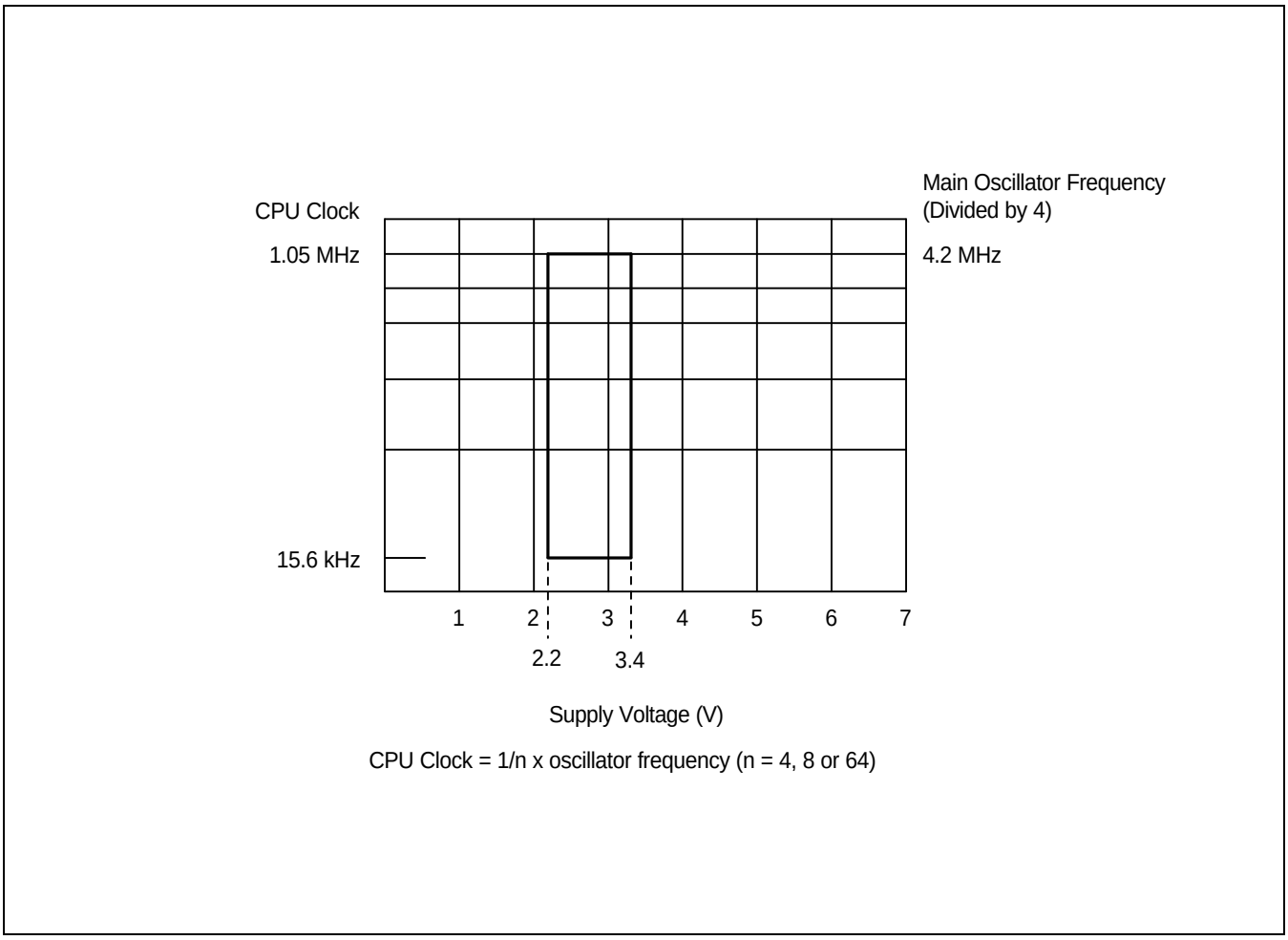


Figure 16-2. Standard Operating Voltage Range