

# 1 PRODUCT OVERVIEW

## OVERVIEW

The S3C7544 single-chip CMOS microcontroller is designed for high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With a versatile 8-bit timer/counter and a D/A converter, the S3C7544 offers an excellent design solution for a wide variety of telecommunication applications.

Up to 17 pins of the 24-pin SDIP package can be dedicated to I/O. Four vectored interrupts provide fast response to internal and external events. In addition, the S3C7544's advanced CMOS technology has realized substantially lower power consumption with a wide operating voltage range — all at a substantially lower cost.

## OTP

The S3C7544 microcontroller is also available in OTP (One Time Programmable) version, S3P7544. S3P7544 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P7544 is comparable to S3C7544, both in function and in pin configuration.

## FEATURES SUMMARY

### Memory

- 512 × 4-bit RAM
- 4096 × 8-bit ROM

### I/O Pins

- 17 pins I/O
- N-channel open-drain I/O: 8 pins

### 8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

### Interval 8-Bit Timer/Counter

- Programmable interval timer
- External event counter function
- Timer/counter clock output to TCLO0 pin

### Buzzer Output

- Four frequency output to BUZ pin

### D/A Converter

- 8-bit D/A converter

### Interrupts

- Two external interrupt vectors
- Two internal interrupt vectors
- One quasi-interrupt

### Memory-Mapped I/O Structure

- Data memory bank 15

### Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

### Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (system clock stops)

### Oscillation Sources

- Crystal, or ceramic for system clock
- Crystal, ceramic: 0.4–6.0 MHz
- CPU clock divider circuit (by 4, 8, or 64)

### Instruction Execution Times

- 0.95, 1.91, and 15.3  $\mu$ s at 4.19 MHz
- 0.67, 1.33, 10.7  $\mu$ s at 6.0 MHz

### Operating Temperature

- –40 °C to 85 °C

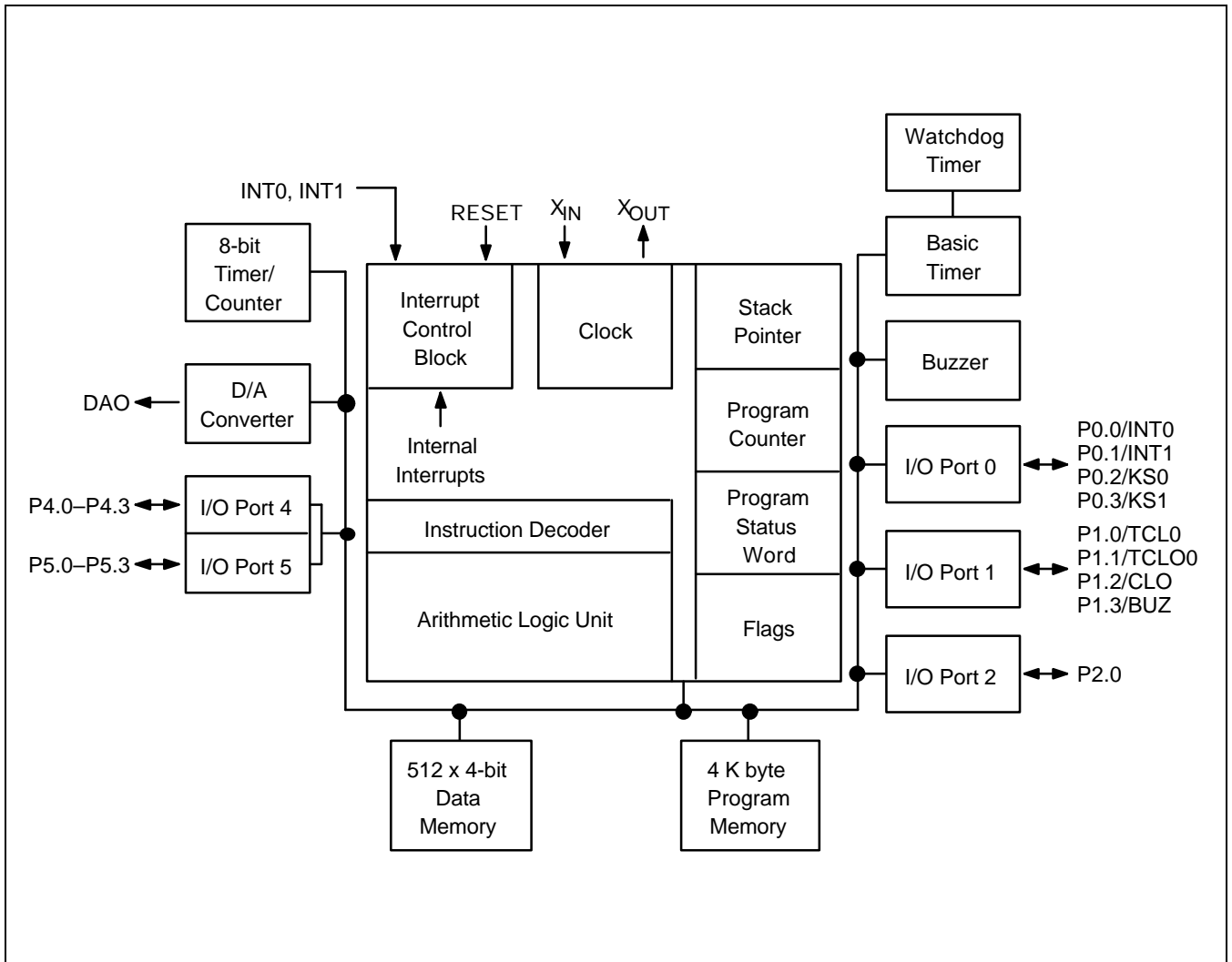
### Operating Voltage Range

- 1.8 V to 5.5 V (at 3 MHz)
- 2.7 V to 5.5 V (at 6 MHz)

### Package Types

- 24-pin SOP-375
- 24-pin SDIP-300

**BLOCK DIAGRAM**



**Figure 1-1. S3C7544 Simplified Block Diagram**

**PIN ASSIGNMENTS**

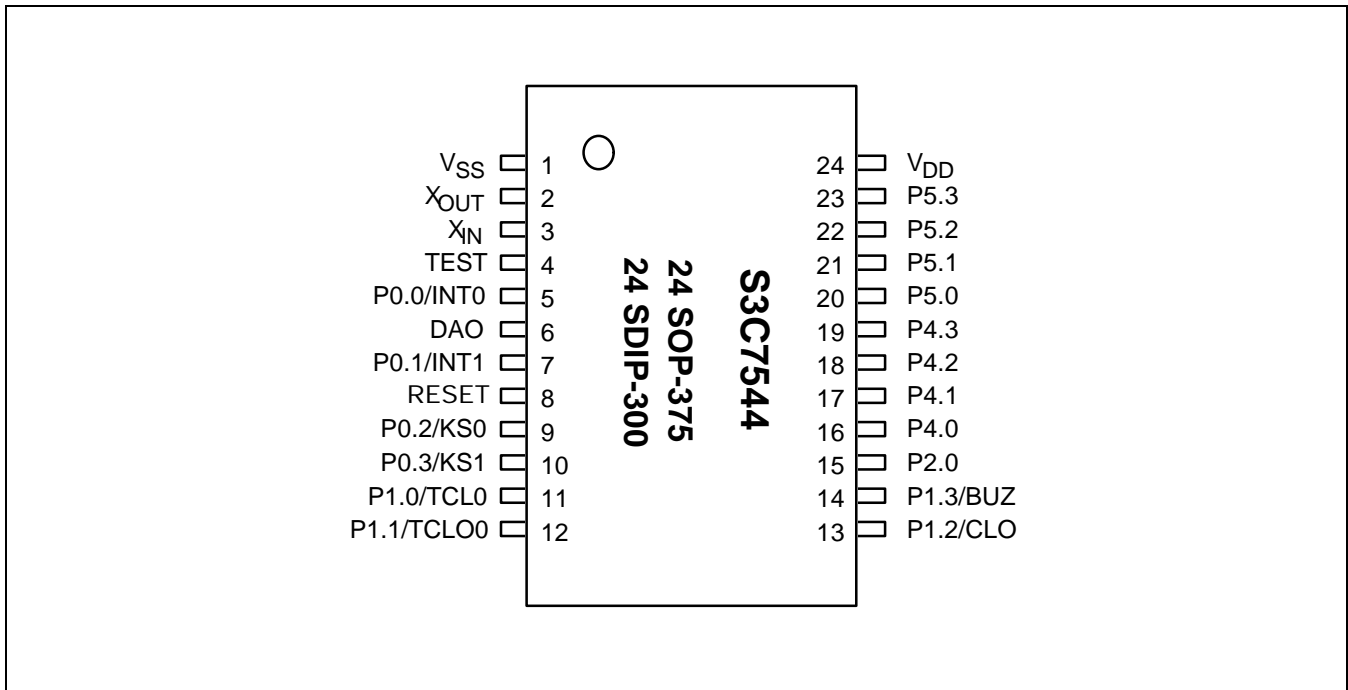


Figure 1-2. S3C7544 Pin Assignment Diagrams

## PIN DESCRIPTIONS

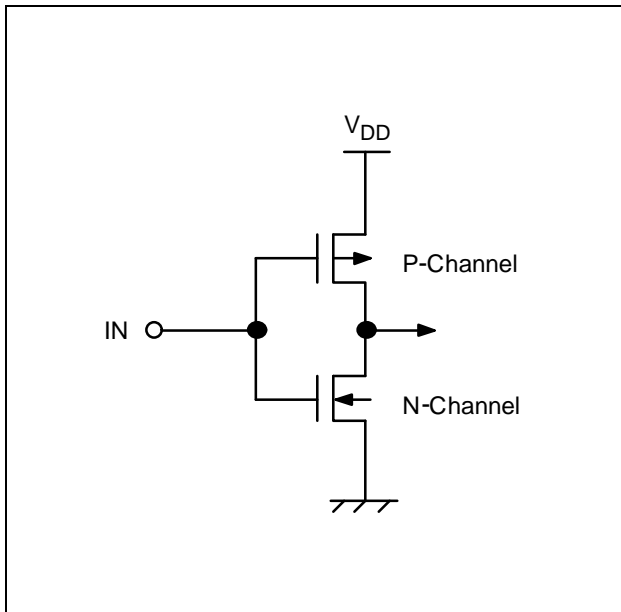
Table 1-1. S3C7544 Pin Descriptions

Pin Name	Pin Type	Description	Share Pin
P0.0 P0.1 P0.2 P0.3	I	4-bit I/O port. 1- or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	INT0 INT1 KS0 KS1
P1.0 P1.1 P1.2 P1.3	I/O	4-bit I/O port. 1- or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	TCL0 TCLO0 CLO BUZ
P2.0	I/O	1-bit I/O port. 1- or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins.	–
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O port. 1- or 4-bit read/write and test is possible. Pins are individually configurable as input or output. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. The N-channel open drain or push-pull output can be selected by software (1-bit unit).	–
INT0	I/O	External interrupts with rising/falling edge detection	P0.0
INT1	I/O	External interrupts with rising/falling edge detection	P0.1
KS0 KS1	I/O	Quasi-interrupt input with falling edge detection	P0.2 P0.3
TCL0	I/O	External clock input for timer/counter	P1.0
TCLO0	I/O	Timer/counter clock output	P1.1
CLO	I/O	CPU clock output	P1.2
BUZ	I/O	0.5, 1, 2, or 4 kHz frequency output at 4.19 MHz for buzzer sound	P1.3
DAO	O	8-bit D/A converter output	–
V <sub>DD</sub>	–	Main power supply	–
V <sub>SS</sub>	–	Ground	–
RESET	I	Reset signal	–
TEST	I	Chip test input pin. Hold GND when the device is operating.	–
X <sub>IN</sub> , X <sub>OUT</sub>	–	Crystal, ceramic oscillator signal for system clock	–

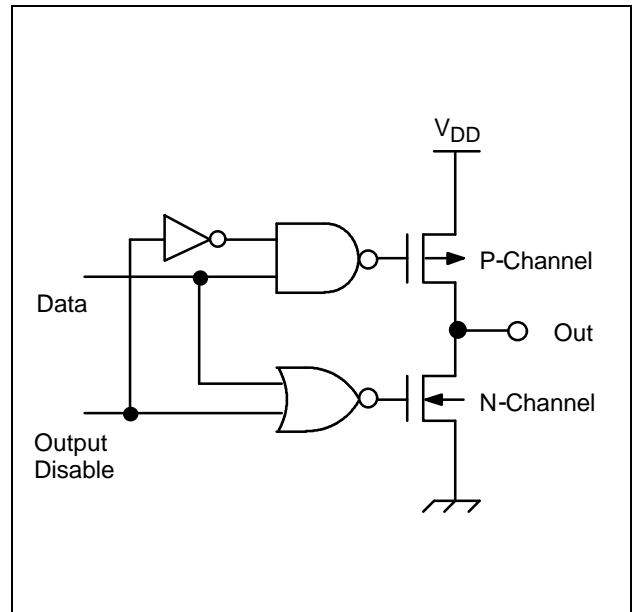
Table 1-2. Overview of S3C7544 Pin Data

SDIP Pin Numbers	Share Pins	I/O Type	Reset Value	Circuit Type
V <sub>SS</sub>	–	–	–	–
X <sub>OUT</sub> , X <sub>IN</sub>	–	–	–	–
TEST	–	I	–	–
P0.0, P0.1	INT0, INT1	I/O	Input	D-4
RESET	–	I	–	B
P0.2 P0.3	KS0 KS1	I/O	Input	D-4
P1.0 P1.1 P1.2 P1.3	TCL0 TCLO0 CLO BUZ	I/O	Input	D-2
P2.0	–	I/O	Input	D-2
DAO	–	O	Output	–
P4.0–P4.3	–	I/O	Input	E-2
P5.0–P5.3	–	I/O	Input	E-2
V <sub>DD</sub>	–	–	–	–

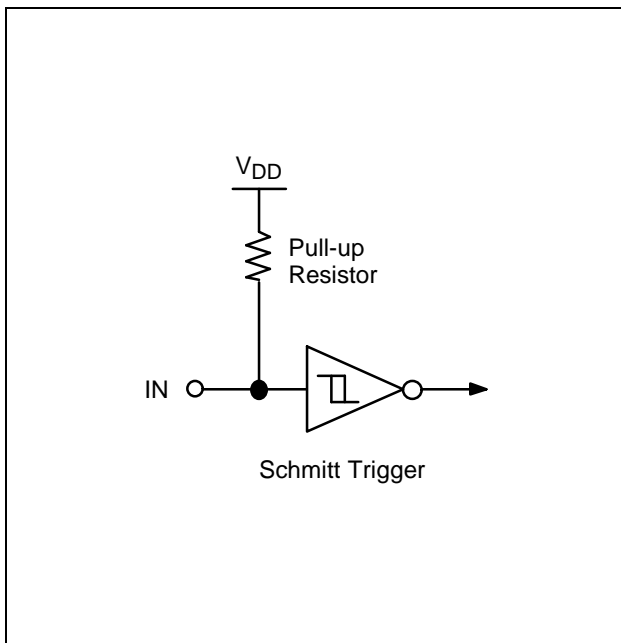
**PIN CIRCUIT DIAGRAMS**



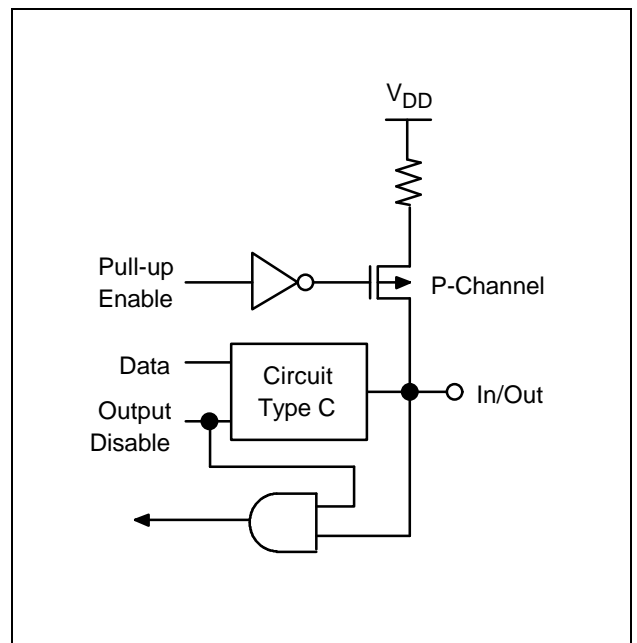
**Figure 1-3. Pin Circuit Type A**



**Figure 1-5. Pin Circuit Type C**



**Figure 1-4. Pin Circuit Type B**



**Figure 1-6. Pin Circuit Type D-2**

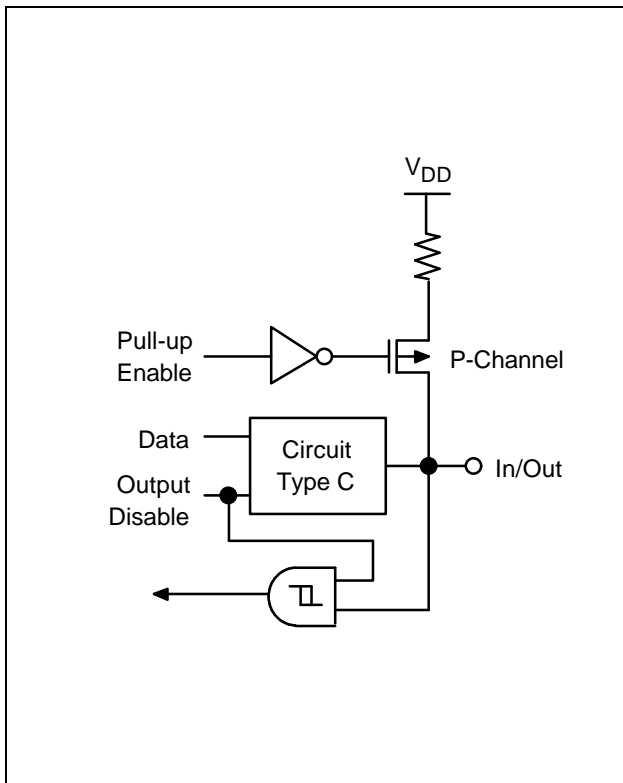


Figure 1-7. Pin Circuit Type D-4

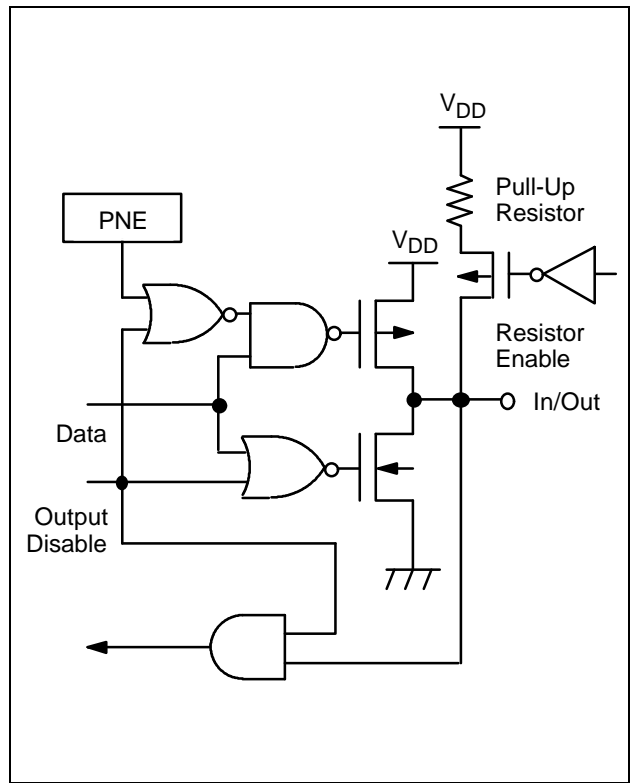


Figure 1-8. Pin Circuit Type E-2



# 14 ELECTRICAL DATA

## OVERVIEW

In this section, S3C7544 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

### Standard Electrical Characteristics

- Absolute maximum ratings
- D.C. electrical characteristics
- Main system clock oscillator characteristics
- Subsystem clock oscillator characteristics
- I/O capacitance
- A.C. electrical characteristics
- Operating voltage range

### Miscellaneous Timing Waveforms

- A.C timing measurement point
- Clock timing measurement at  $X_{iN}$
- Clock timing measurement at  $XT_{iN}$
- TCL timing
- Input timing for RESET
- Input timing for external interrupts
- Serial data transfer timing

### Stop Mode Characteristics and Timing Waveforms

- RAM data retention supply voltage in stop mode
- Stop mode release timing when initiated by RESET
- Stop mode release timing when initiated by an interrupt request

Table 14-1. Absolute Maximum Ratings

(T<sub>A</sub> = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V <sub>DD</sub>	–	– 0.3 to + 6.5	V
Input Voltage	V <sub>I</sub>	All I/O ports	– 0.3 to V <sub>DD</sub> + 0.3	V
Output Voltage	V <sub>O</sub>	–	– 0.3 to V <sub>DD</sub> + 0.3	V
Output Current High	I <sub>OH</sub>	One I/O port active	– 5	mA
		All I/O ports active	– 35	
Output Current Low	I <sub>OL</sub>	One I/O port active	+ 30 (peak)	mA
			+ 15 (note)	
		All I/O ports active	+ 100 (peak)	
			+ 60 (note)	
Operating Temperature	T <sub>A</sub>	–	– 40 to + 85	°C
Storage Temperature	T <sub>stg</sub>	–	– 65 to + 150	°C

**NOTE:** The values for output current low (I<sub>OL</sub>) are calculated as peak value × √Duty .

Table 14-2. D.C. Electrical Characteristics

(T<sub>A</sub> = – 40 °C to + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V <sub>IH1</sub>	All input pins except V <sub>IH2</sub> –V <sub>IH3</sub>	0.7 V <sub>DD</sub>	–	V <sub>DD</sub>	V
	V <sub>IH2</sub>	P0 and RESET	0.8 V <sub>DD</sub>	–	V <sub>DD</sub>	
	V <sub>IH3</sub>	X <sub>IN</sub> and X <sub>OUT</sub>	V <sub>DD</sub> – 0.1	–	V <sub>DD</sub>	
Input Low Voltage	V <sub>IL1</sub>	All input pins except V <sub>IH2</sub> –V <sub>IH3</sub>	–	–	0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	P0 and RESET			0.2 V <sub>DD</sub>	
	V <sub>IL3</sub>	X <sub>IN</sub> and X <sub>OUT</sub>			0.1	

Table 14-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V <sub>OH</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 1.0	-	-	V
Output Low Voltage	V <sub>OL1</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OL</sub> = 15 mA Ports 4, 5	-	-	2	V
		V <sub>DD</sub> = 1.8 V to 5.5 V I <sub>OL</sub> = 1.6 mA			0.4	
	V <sub>OL2</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OL</sub> = 4 mA All out ports except ports 4, 5			2	
		V <sub>DD</sub> = 1.8 V to 5.5 V I <sub>OL</sub> = 1.6 mA			0.6	
Input High Leakage Current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub> All input pins except X <sub>IN</sub> and X <sub>OUT</sub>	-	-	3	μA
	I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub> X <sub>IN</sub> and X <sub>OUT</sub>			20	
Input Low Leakage Current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V All input pins except X <sub>IN</sub> , X <sub>OUT</sub> and RESET	-	-	-3	μA
	I <sub>LIL2</sub>	V <sub>IN</sub> = 0 V X <sub>IN</sub> and X <sub>OUT</sub>			-20	
Output High Leakage Current	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DD</sub> All output pins	-	-	3	μA
Output Low Leakage Current	I <sub>LOL</sub>	V <sub>O</sub> = 0 V All output pins	-	-	-3	μA
Pull-up Resistor	R <sub>L1</sub>	V <sub>DD</sub> = 5 V; V <sub>I</sub> = 0 V except RESET	25	45	100	kΩ
		V <sub>DD</sub> = 3 V	50	90	200	
	R <sub>L2</sub>	V <sub>DD</sub> = 5 V; V <sub>I</sub> = 0 V; RESET	100	220	400	
		V <sub>DD</sub> = 3 V	200	450	800	

**Table 14-2. D.C. Electrical Characteristics (Concluded)**

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply Current (1)	$I_{DD1}$ (DAC on)	Run mode; $V_{DD} = 5.0\text{ V} \pm 10\%$	6.0MHz	-	3.4	10.0	mA
		Crystal oscillator; $C1 = C2 = 22\text{pF}$	4.19MHz		2.7	8.0	
	$I_{DD2}$ (DAC off)	Run mode; $V_{DD} = 5.0\text{ V} \pm 10\%$	6.0MHz	-	2.3	8.0	mA
			Crystal oscillator; $C1 = C2 = 22\text{pF}$		4.19MHz	1.7	
		$V_{DD} = 3\text{ V} \pm 10\%$	6.0MHz		1.1	4.0	
			4.19MHz		0.8	3.0	
	$I_{DD3}$	Idle mode; $V_{DD} = 5.0\text{ V} \pm 10\%$	6.0MHz	-	0.7	2.5	mA
			Crystal oscillator; $C1 = C2 = 22\text{pF}$		4.19MHz	0.5	
		$V_{DD} = 3\text{ V} \pm 10\%$	6.0MHz		0.3	1.5	
			4.19MHz		0.2	1.0	
$I_{DD4}$	Stop mode; $V_{DD} = 5.0\text{ V} \pm 10\%$		-	0.2	3.0	$\mu\text{A}$	
	Stop mode; $V_{DD} = 3.0\text{ V} \pm 10\%$			0.1	2.0		

**NOTES:**

- D.C. electrical values for supply current ( $I_{DD1}$  to  $I_{DD3}$ ) do not include the current drawn through internal pull-up resistors.
- $I_{DD1}$  typical values are measured when DADATA register value is 055H.

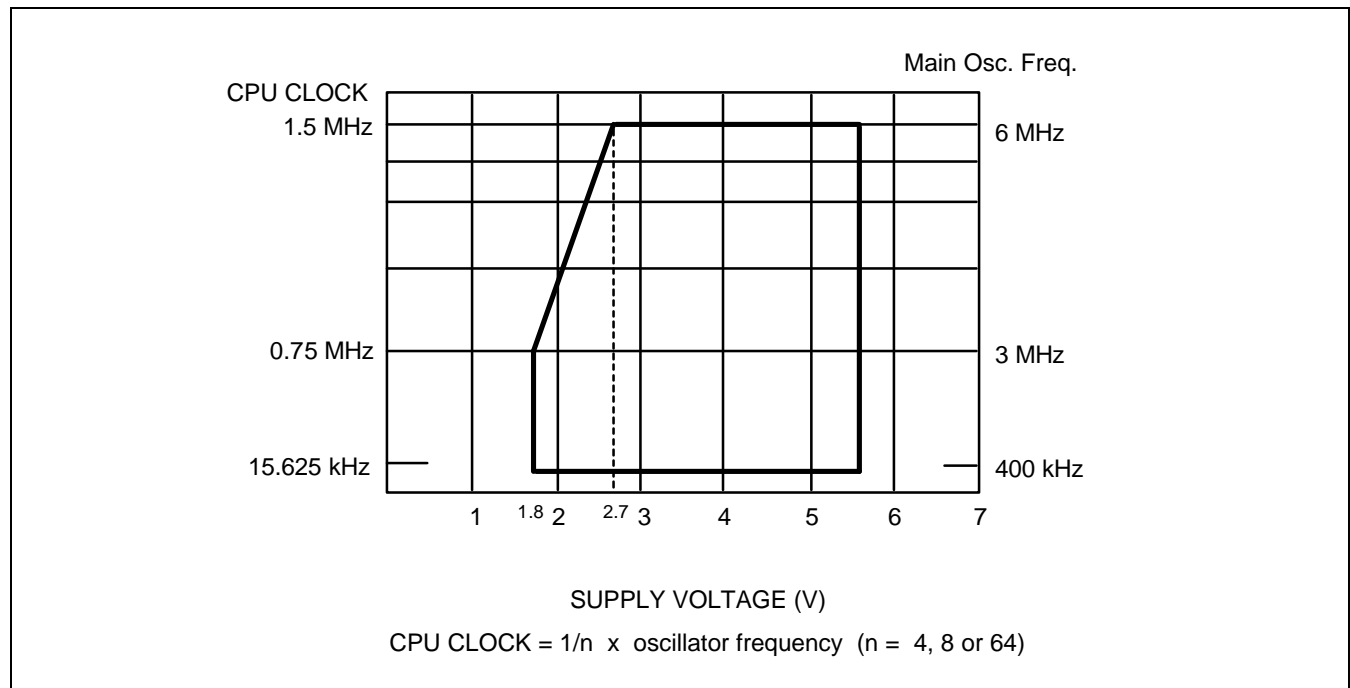
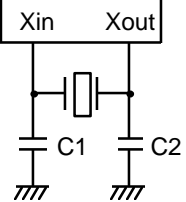
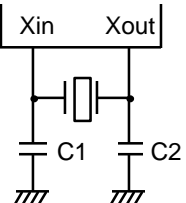
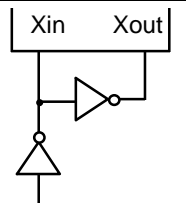
**Figure 14-1. Standard Operating Voltage Range**

Table 14-3. Oscillators Characteristics

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency <sup>(1)</sup>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V <sub>DD</sub> = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time <sup>(2)</sup>	V <sub>DD</sub> = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency <sup>(1)</sup>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V <sub>DD</sub> = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time <sup>(2)</sup>	V <sub>DD</sub> = 3.0 V	–	–	10	ms
External Clock		X <sub>IN</sub> input frequency <sup>(1)</sup>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V <sub>DD</sub> = 1.8 V to 5.5 V	0.4	–	3	
		X <sub>IN</sub> input high and low level width (t <sub>XH</sub> , t <sub>XL</sub> )	–	83.3	–	1250	ns

**NOTES:**

- Oscillation frequency and X<sub>IN</sub> input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Recommended Oscillator Constants

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Manufacturer	Series Number <sup>(1)</sup>	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR 05M5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR 05MC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR 05MC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

**NOTES:**

1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 14-5. Input/Output Capacitance

(T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C <sub>IN</sub>	f = 1 MHz; Unmeasured pins are returned to V <sub>SS</sub>	–	–	15	pF
Output Capacitance	C <sub>OUT</sub>				15	pF
I/O Capacitance	C <sub>IO</sub>				15	pF

Table 14-6. D/A Converter Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 3.5 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution	–	–	–	–	8	bits
Absolute Accuracy	–		–3	–	3	LSB
Differential Linearity Error	DLE		–1	–	1	LSB
Setup Time	t <sub>su</sub>		–	–	5	μs
Output Resistance	R <sub>O</sub>		4.5	5	5.5	KΩ

Table 14-7. A.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t <sub>CY</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.67	–	64	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.33			
TCL0 Input Frequency	f <sub>TI</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0	–	1.5	MHz
		V <sub>DD</sub> = 1.8 V to 5.5 V			1	MHz
TCL0 Input High, Low Width	t <sub>TIH</sub> , t <sub>TIL</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.48	–	–	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.8			
Interrupt Input High, Low Width	t <sub>INTH</sub> , t <sub>INTL</sub>	INT0, INT1, KS0–KS1	10	–	–	μs
RESET Input Low Width	t <sub>RSL</sub>	Input	–	–	10	μs

Table 14-8. RAM Data Retention Supply Voltage in Stop Mode

(T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDDR</sub>	–	1.8	–	5.5	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.8 V	–	0.1	10	μA
Release signal set time	t <sub>SREL</sub>	–	0	–	–	μs
Oscillator stabilization wait time <sup>(1)</sup>	t <sub>WAIT</sub>	Released by RESET	–	2 <sup>17</sup> /f <sub>x</sub>	–	ms
		Released by interrupt	–	(2)	–	ms

**NOTES:**

- During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
- Use the basic timer mode register (BMOD) interval timer to delay the execution of CPU instructions during the wait time.

TIMING WAVEFORMS

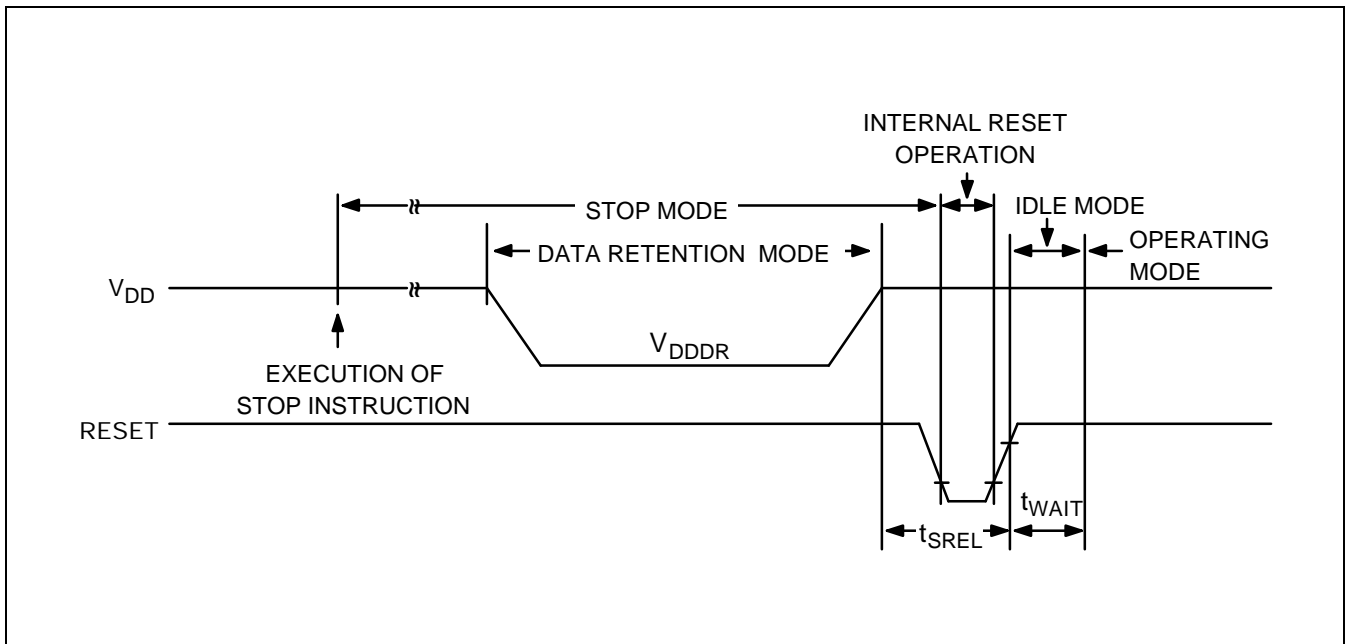


Figure 14-2. Stop Mode Release Timing When Initiated by RESET

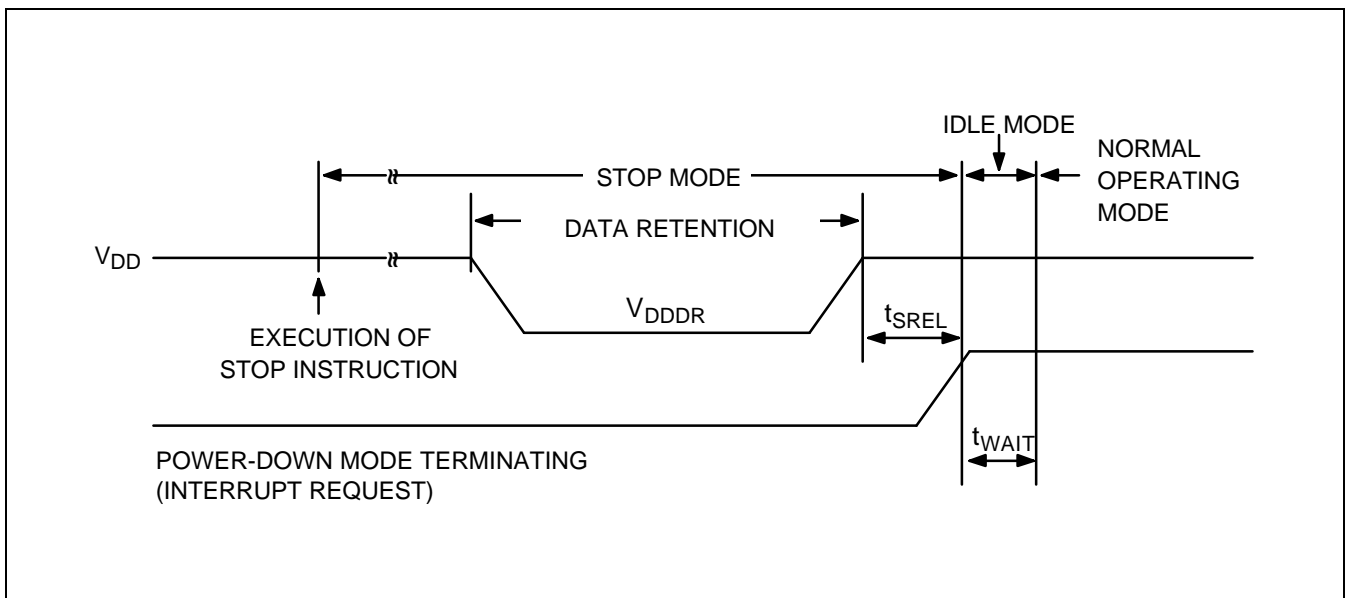


Figure 14-3. Stop Mode Release Timing When Initiated by Interrupt Request



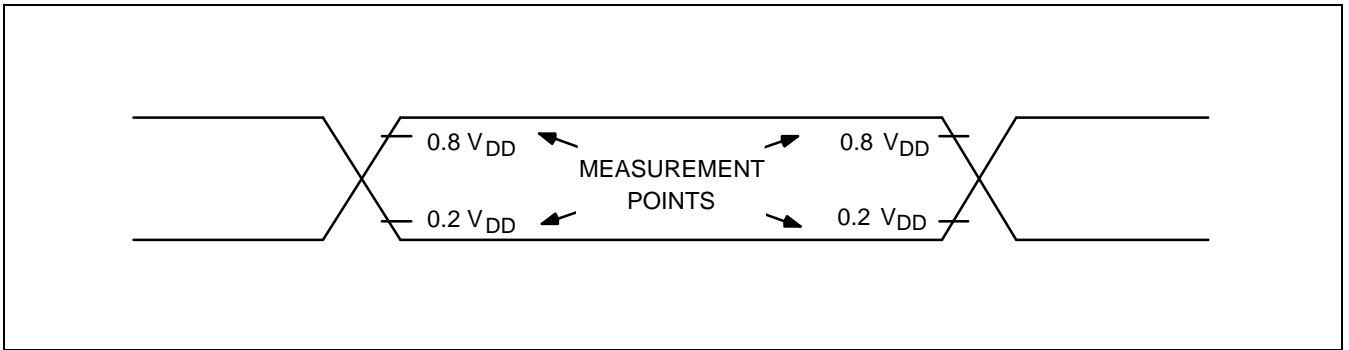


Figure 14-4. A.C. Timing Measurement Points (Except for  $X_{IN}$ )

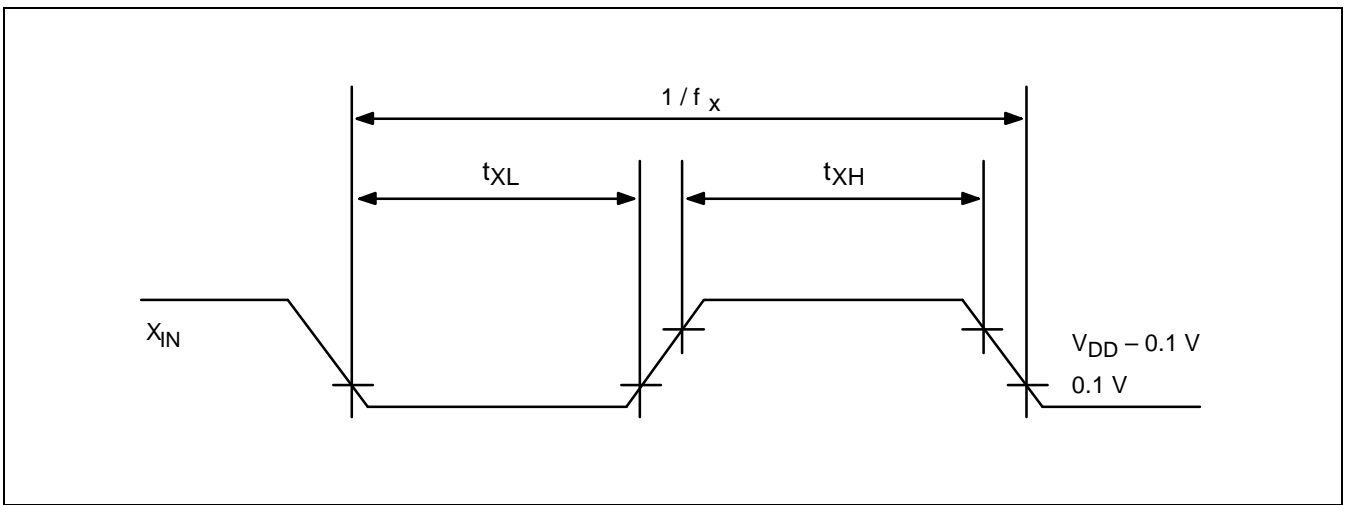


Figure 14-5. Clock Timing Measurement at  $X_{IN}$

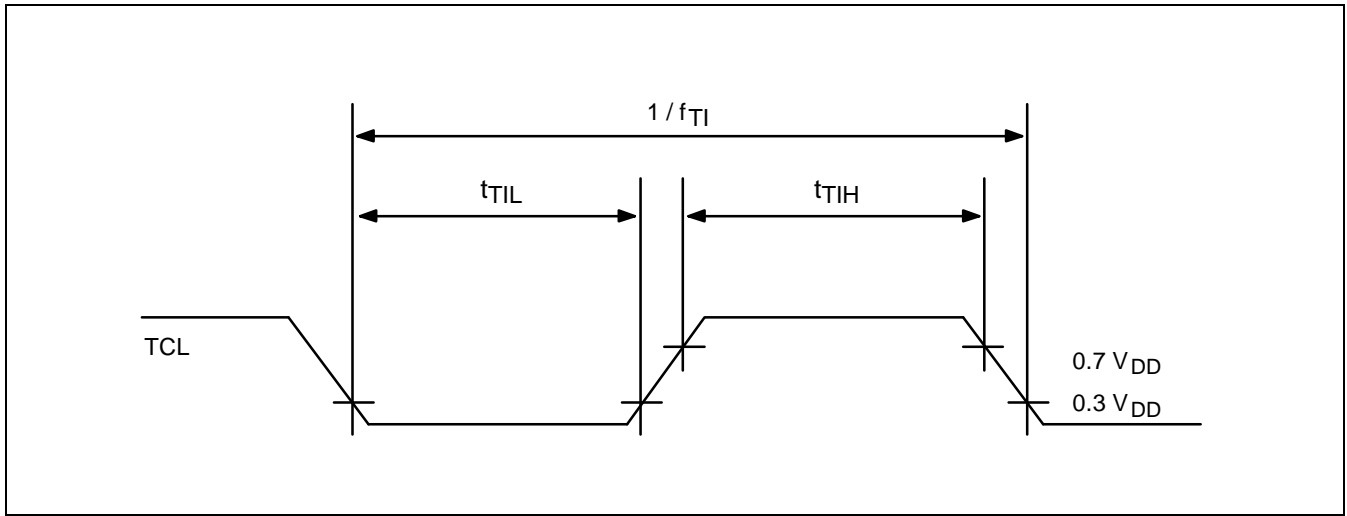


Figure 14-6. TCL Timing

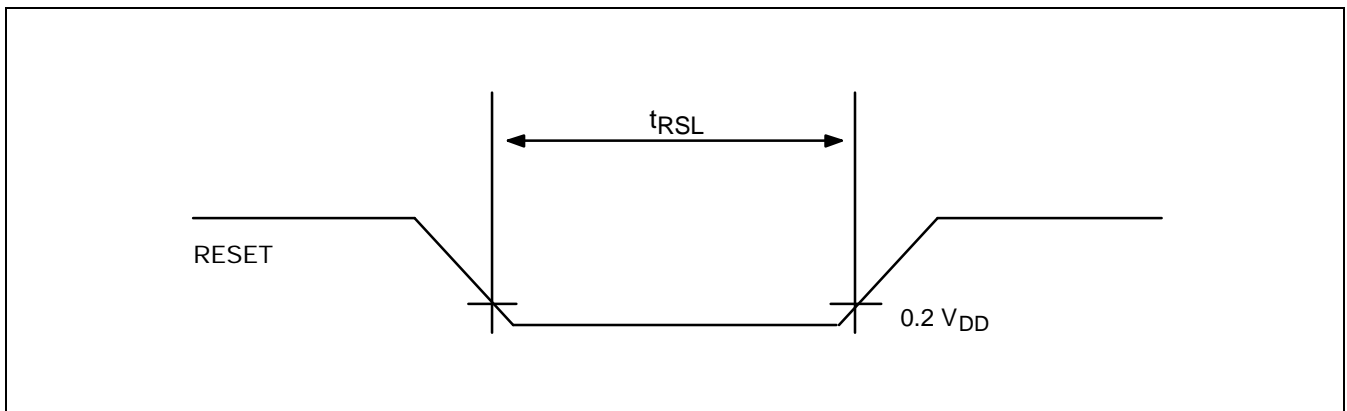


Figure 14-7. Input Timing for RESET Signal

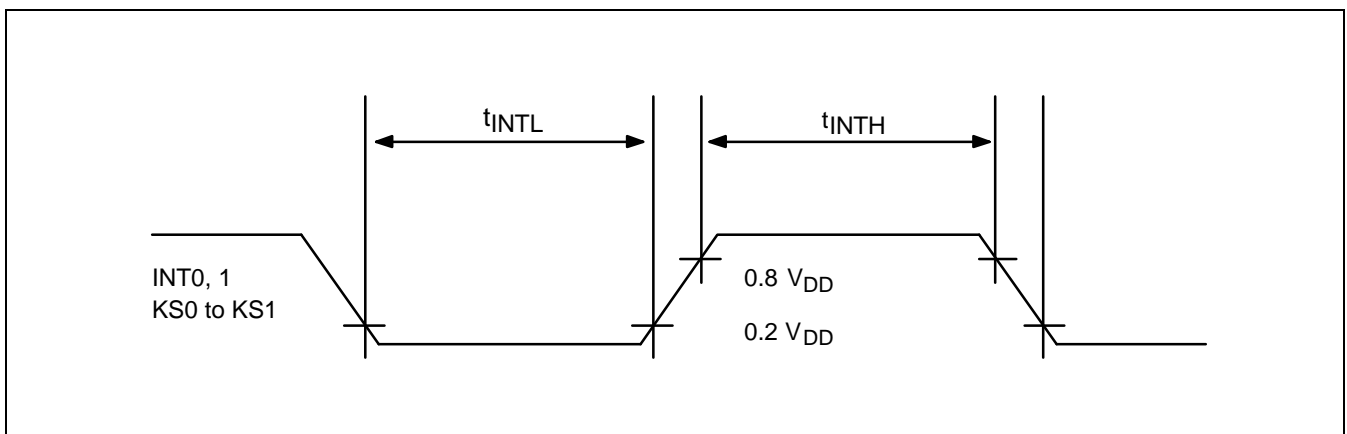


Figure 14-8. Input Timing for External Interrupts

# 15 MECHANICAL DATA

This section contains the following information about the device package:

- Package dimensions in millimeters
- Pad diagram
- Pad/pin coordinate data table

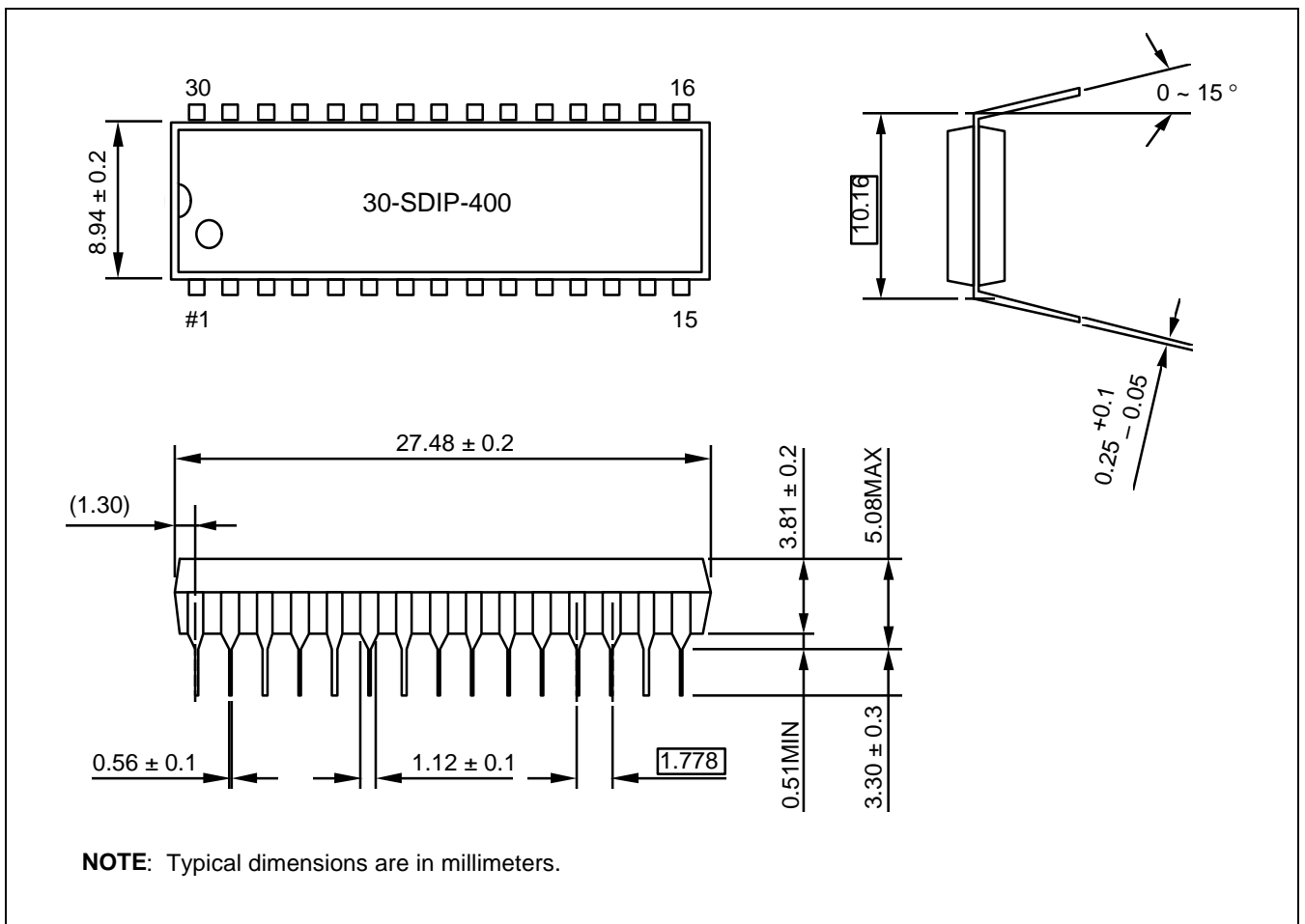


Figure 15-1. 30-SDIP-400 Package Dimensions

# 16

## S3P7544 OTP

### OVERVIEW

The S3P7544 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C7544 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P7544 is fully compatible with the S3C7544, both in function and in pin configuration. Because of its simple programming requirements, the S3P7544 is ideal for use as an evaluation chip for the S3C7544.

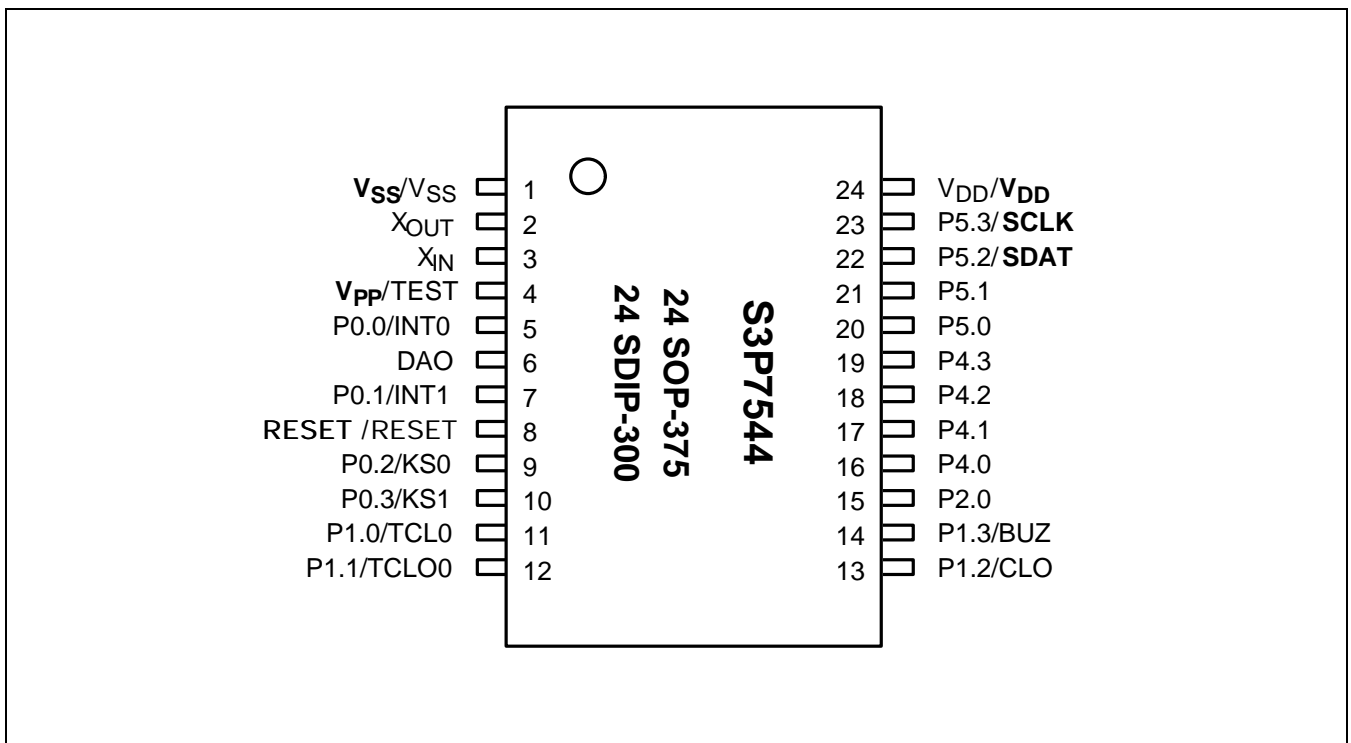


Figure 16-1. S3P7544 Pin Assignments (24 SOP-375, 24 SDIP-300 Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P5.2	SDAT	22	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P5.3	SCLK	23	I/O	Serial clock pin. Input only pin.
TEST	TEST	4	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option) Hold GND when OTP is operating.
RESET	RESET	8	I	Chip initialization
V <sub>DD</sub> /V <sub>SS</sub>	V <sub>DD</sub> /V <sub>SS</sub>	24/1	–	Logic power supply pin. V <sub>DD</sub> should be tied to +5 V during programming.

**NOTE:** ( ) means the 32-SOP OTP pin number.

Table 16-2. Comparison of S3P7544 and S3C7544 Features

Characteristic	S3P7544	S3C7544
Program Memory	4 K-byte EPROM	4 K-byte mask ROM
Operating Voltage (V <sub>DD</sub> )	1.8 V (3 MHz) to 5.5 V	1.8 V (3 MHz) to 5.5 V
OTP Programming Mode	V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST) = 12.5 V	–
Pin Configuration	24 SOP, 24 SDIP	24 SOP, 24 SDIP
EPROM Programmability	User Program one time	Programmed at the factory

## OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub>(TEST) pin of the S3P7544, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

V <sub>DD</sub>	V <sub>PP</sub> (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

**NOTE:** "0" means Low level; "1" means High level.

## OTP ELECTRICAL DATA

Table 16-4. Absolute Maximum Ratings

(T<sub>A</sub> = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V <sub>DD</sub>	–	– 0.3 to + 6.5	V
Input Voltage	V <sub>I</sub>	All I/O ports	– 0.3 to V <sub>DD</sub> + 0.3	V
Output Voltage	V <sub>O</sub>	–	– 0.3 to V <sub>DD</sub> + 0.3	V
Output Current High	I <sub>OH</sub>	One I/O port active	– 5	mA
		All I/O ports active	– 35	
Output Current Low	I <sub>OL</sub>	One I/O port active	+ 30 (peak)	mA
			+ 15 (note)	
		All I/O ports active	+ 100 (peak)	
			+ 60 (note)	
Operating Temperature	T <sub>A</sub>	–	– 40 to + 85	°C
Storage Temperature	T <sub>stg</sub>	–	– 65 to + 150	°C

**NOTE:** The values for output current low (I<sub>OL</sub>) are calculated as peak value ×  $\sqrt{\text{Duty}}$ .

Table 16-5. D.C. Electrical Characteristics

(T<sub>A</sub> = – 40 °C to + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V <sub>IH1</sub>	All input pins except V <sub>IH2</sub> –V <sub>IH3</sub>	0.7 V <sub>DD</sub>	–	V <sub>DD</sub>	V
	V <sub>IH2</sub>	P0 and RESET	0.8 V <sub>DD</sub>	–	V <sub>DD</sub>	
	V <sub>IH3</sub>	X <sub>IN</sub> and X <sub>OUT</sub>	V <sub>DD</sub> – 0.1	–	V <sub>DD</sub>	
Input Low Voltage	V <sub>IL1</sub>	All input pins except V <sub>IH2</sub> –V <sub>IH3</sub>	–	–	0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	P0 and RESET			0.2 V <sub>DD</sub>	
	V <sub>IL3</sub>	X <sub>IN</sub> and X <sub>OUT</sub>			0.1	

Table 16-5. D.C. Electrical Characteristics (Continued)

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C, } V_{DD} = 1.8\text{ V to } 5.5\text{ V})$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	$V_{OH}$	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$ $I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$	–	–	V
Output Low Voltage	$V_{OL1}$	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$ $I_{OL} = 15\text{ mA}$ Ports 4, 5	–	–	2	V
		$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$ $I_{OL} = 1.6\text{ mA}$			0.4	
	$V_{OL2}$	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$ $I_{OL} = 4\text{ mA}$ All out ports except ports 4, 5			2	
		$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$ $I_{OL} = 1.6\text{ mA}$			0.6	
Input High Leakage Current	$I_{LIH1}$	$V_{IN} = V_{DD}$ All input pins except $X_{IN}$ and $X_{OUT}$	–	–	3	$\mu\text{A}$
	$I_{LIH2}$	$V_{IN} = V_{DD}$ $X_{IN}$ and $X_{OUT}$			20	
Input Low Leakage Current	$I_{LIL1}$	$V_{IN} = 0\text{ V}$ All input pins except $X_{IN}$ , $X_{OUT}$ and RESET	–	–	–3	$\mu\text{A}$
	$I_{LIL2}$	$V_{IN} = 0\text{ V}$ $X_{IN}$ and $X_{OUT}$			–20	
Output High Leakage Current	$I_{LOH}$	$V_O = V_{DD}$ All output pins	–	–	3	$\mu\text{A}$
Output Low Leakage Current	$I_{LOL}$	$V_O = 0\text{ V}$ All output pins	–	–	–3	$\mu\text{A}$
Pull-up Resistor	$R_{L1}$	$V_{DD} = 5\text{ V; } V_I = 0\text{ V}$ except RESET	25	50	100	k $\Omega$
		$V_{DD} = 3\text{ V}$	50	100	200	
	$R_{L2}$	$V_{DD} = 5\text{ V; } V_I = 0\text{ V; RESET}$	100	250	400	
		$V_{DD} = 3\text{ V}$	200	500	800	

**Table 16-5. D.C. Electrical Characteristics (Concluded)** $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{DD} = 1.8\text{ V to } 5.5\text{ V})$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply Current (1)	$I_{DD1}$ (DAC on)	Run mode; $V_{DD} = 5.0\text{ V} \pm 10\%$	6.0MHz	-	3.4	10.0	mA
		Crystal oscillator; $C1 = C2 = 22\text{pF}$	4.19MHz		2.7	8.0	
	$I_{DD2}$ (DAC off)	Run mode; $V_{DD} = 5.0\text{ V} \pm 10\%$	6.0MHz	-	2.3	8.0	mA
			Crystal oscillator; $C1 = C2 = 22\text{pF}$		4.19MHz	1.7	
		$V_{DD} = 3\text{ V} \pm 10\%$	6.0MHz		1.1	4.0	
			4.19MHz		0.8	3.0	
	$I_{DD3}$	Idle mode; $V_{DD} = 5.0\text{ V} \pm 10\%$	6.0MHz	-	0.7	2.5	mA
			Crystal oscillator; $C1 = C2 = 22\text{pF}$		4.19MHz	0.5	
		$V_{DD} = 3\text{ V} \pm 10\%$	6.0MHz		0.3	1.5	
			4.19MHz		0.2	1.0	
$I_{DD4}$	Stop mode; $V_{DD} = 5.0\text{ V} \pm 10\%$		-	0.2	3.0	$\mu\text{A}$	
	Stop mode; $V_{DD} = 3.0\text{ V} \pm 10\%$			0.1	2.0		

**NOTES:**

- D.C. electrical values for supply current ( $I_{DD1}$  to  $I_{DD3}$ ) do not include the current drawn through internal pull-up resistors.
- $I_{DD1}$  typical values are measured when DADATA register value is 055H .

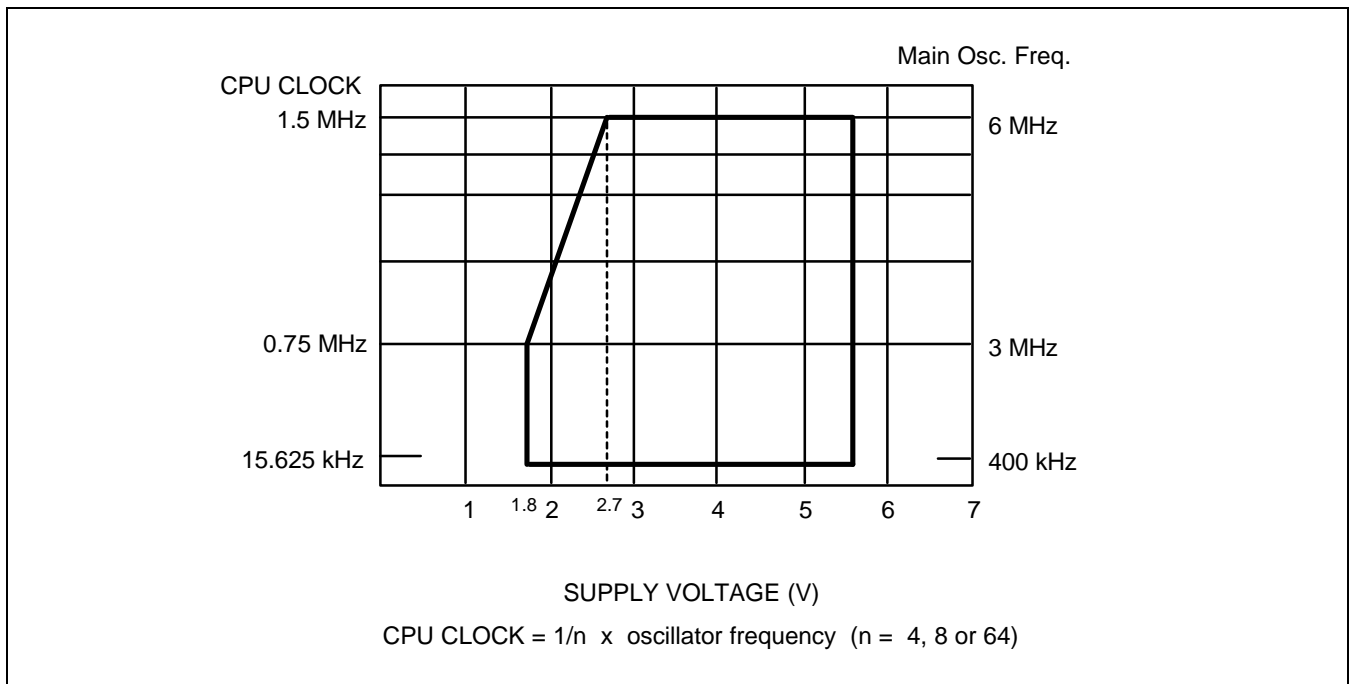
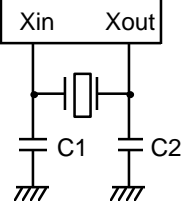
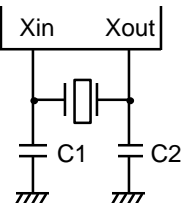
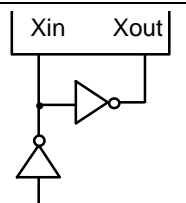
**Figure 16-2. Standard Operating Voltage Range**



Table 16-6. Oscillators Characteristics

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency <sup>(1)</sup>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V <sub>DD</sub> = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time <sup>(2)</sup>	V <sub>DD</sub> = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency <sup>(1)</sup>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V <sub>DD</sub> = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time <sup>(2)</sup>	V <sub>DD</sub> = 3.0 V	–	–	10	ms
External Clock		X <sub>IN</sub> input frequency <sup>(1)</sup>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V <sub>DD</sub> = 1.8 V to 5.5 V	0.4	–	3	
		X <sub>IN</sub> input high and low level width (t <sub>XH</sub> , t <sub>XL</sub> )	–	83.3	–	1250	ns

**NOTES:**

- Oscillation frequency and X<sub>IN</sub> input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 16-7. Input/Output Capacitance

(T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C <sub>IN</sub>	f = 1 MHz; Unmeasured pins are returned to V <sub>SS</sub>	–	–	15	pF
Output Capacitance	C <sub>OUT</sub>				15	pF
I/O Capacitance	C <sub>IO</sub>				15	pF

Table 16-8. Comparator Electrical Characteristics

(T<sub>A</sub> = –40 °C to +85 °C, V<sub>DD</sub> = 3.5 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution	–	–	–	–	8	bits
Absolute Accuracy	–		–3	–	3	LSB
Differential Linearity Error	DLE		–1	–	1	LSB
Setup Time	t <sub>su</sub>		–	–	5	μs
Output Resistance	R <sub>O</sub>		4.5	5	5.5	KΩ

Table 16-9. A.C. Electrical Characteristics

(T<sub>A</sub> = –40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t <sub>CY</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.67	–	64	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.33			
TCL0 Input Frequency	f <sub>TI</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0	–	1.5	MHz
		V <sub>DD</sub> = 1.8 V to 5.5 V			1	MHz
TCL0 Input High, Low Width	t <sub>TIH</sub> , t <sub>TIL</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.48	–	–	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.8			
Interrupt Input High, Low Width	t <sub>INTH</sub> , t <sub>INTL</sub>	INT0, INT1, KS0–KS1	10	–	–	μs
RESET Input Low Width	t <sub>RSL</sub>	Input	–	–	10	μs

**Table 16-10. RAM Data Retention Supply Voltage in Stop Mode** $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{\text{DDDR}}$	–	1.8	–	5.5	V
Data retention supply current	$I_{\text{DDDR}}$	$V_{\text{DDDR}} = 1.8\text{ V}$	–	0.1	10	$\mu\text{A}$
Release signal set time	$t_{\text{SREL}}$	–	0	–	–	$\mu\text{s}$
Oscillator stabilization wait time (1)	$t_{\text{WAIT}}$	Released by RESET	–	$2^{17}/f_x$	–	ms
		Released by interrupt	–	(2)	–	ms

**NOTES:**

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay the execution of CPU instructions during the wait time.